The AI-218 is an 8-channel, fully isolated, high performance analog-to-digital input board. The AI-218 is part of UEI's Guardian series, which consists of I/O boards equipped with on-board diagnostic circuitry.

This application note details the AI-218 self-test functionality and provides an overview of how to configure, perform, and interpret a self-test.

AI-218 self-test description

The AI-218 boards have switches built into the front end allowing a comprehensive self-test of the input stages, even while still connected to the field wiring.

Switches between the input resistor and input programmable gain amplifier (PGA) allow a fixed reference voltage to be connected to the PGA inputs (see S1 and S4 below).
In this configuration, the input signal may have a small effect, but the overall reading should be within 4% of the reference voltage.

Additionally, note that the PGA used on the AI-218 has two input channels (`IN1` and `IN2`). A secondary check of the input system may be conducted by setting the PGA input to read from the second input channel, which is directly connected to the voltage reference. External wiring will have no effect on the PGA secondary input.

AI-218 self-test circuitry block diagram

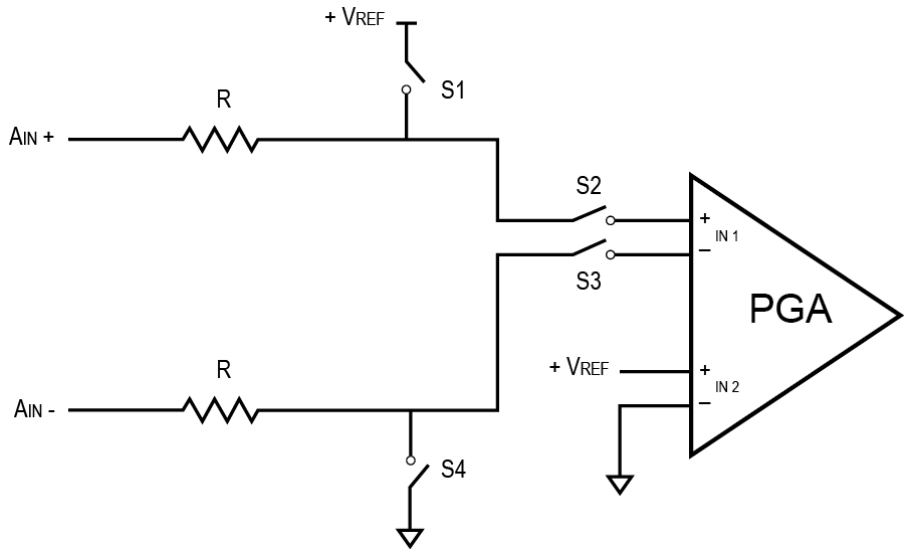

Figure 1 Block Diagram of AI-218 Input and Built-in-Test Circuitry

AI-218 self-test configuration and interpretation

This section provides an overview of configuring the AI-218 built-in test features and interpreting results.

Hardware and software configuration

The AI-218 self-test provides two built-in-test (BIT) options. You can configure a self-test with reference voltage injected between the input resistors and PGA or configure a self-test that only includes the path from the PGA on.

The software configuration steps for implementing the AI-218 self-test are listed below (the low-level API that is used in each step is provided in the parenthesis):

1. Configure mux states to switch in test circuitry (`DqAdv218SetBITMux()`)
2. Configure a channel list (`DqAdv217Read()`)
3. Acquire / monitor the voltage reading (`DqAdv217Read()`)

Result interpretation

The self-test reference voltage is read as approximately 5 volts for the AI-218.

In the mode where the reference voltage is injected between the input resistors and PGA, an input signal on an AI-218 analog input pin may have a small effect on the overall self-test voltage readings by approximately 4% or less.

When interpreting self-test results, the criteria indicating a pass should be a range of voltages instead of an exact value.

AI-218 self-test tutorial

This tutorial provides an overview of how to implement the AI-218 self-test modes using the low-level API.

Please note that only the specific steps for implementing the self-test are provided. Opening communication with the RACK or Cube, handling error codes, and other tasks not specific to self-test are omitted (examples of these tasks can be found in the Sample218 sample code).

Test conditions

- All AI-218 channels (AI0..AI7) are configured and monitored
- Input voltage on even channels is -5.6 V
- Input voltage on odd channels is 3.75 V

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Tutorial

1. **Configure mux states to switch in test circuitry**
   The `DqAdv218SetBITMux()` API controls configuring switches for the self-test mode you want to use.

   The following API configures all channels to switch in $+V_{REF}$ (5 V) to `IN1+` and ground to `IN1-` of the PGA (refer to Figure 1):

```
DqAdv218SetBITMux(hd, DEVN, DQ_AI218_BIT_ALL_CHAN, DQ_AI218_BIT_5V_IN);
```

   BIT options include the following:
   - Normal operation; no BIT (default):
     `DQ_AI218_BIT_OFF` closes S2 and S3 switches and opens S1 and S4.
     The PGA uses the normal input (`IN1`).
   - Self-test that includes reference voltage injected between the input resistors and PGA:
     `DQ_AI218_BIT_5V_IN` closes S1, S2, S3, and S4.
     The PGA uses the normal input (`IN1`) (input voltage has minimal effect).
   - Self-test that tests from PGA on:
     `DQ_AI218_BIT_ALT_5V` causes the PGA to use the alternate `IN2` reference voltage.

2. **Configure the list of channels for self-test**
   The channel list sets up a list of channels to acquire data from and configures what anticipated voltage range (gain) that each channel will support.
   - Set up the channel list array for channel 0..7 (CHANNELS is defined as 8).
   - Use `DQ_LNCL_GAIN` macro to OR in programming a gain of 1 (range of 0 V to maximum supported voltage). We use a gain of 1 for the AI-218 self-test.

```
for (n = 0; n < CHANNELS; n++) {
     cl[n] = n | DQ_LNCL_GAIN(DQ_AI218_GAIN_1); // gain is set in channel list
}

// the first call to DqAdv217Read sets up the channel configuration
DqAdv217Read(hd, DEVN, CHANNELS, cl, NULL, NULL);
```

   The following code ensures that the PGA test current is not enabled:

```
DqAdv217SetCfgLayer(hd, DEVN, DQ_AI217_SETCFG_ALL_CHAN,
                    DQ_AI217_SET_CFG_LAYER_PGA,
                    DQ_AI217_PDWR_PGA_I_SRC_OFF);
```


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3. Acquire / monitor the actual voltage reading

```
printf(" data ");
DqAdv217Read(hd, DEVN, CHANNELS, cl, data, fdata);
for (i = 0; i < CHANNELS; i++) {
        printf("\n cl %2d: %2.6f ", i, fdata[i]);
}
```

Results

In our example, UEI's test adapter differentially drives even channels with -5.6 V and odd channels with +3.7 V.

The following are the output displays for each of the BIT modes on the AI-218 on our test system (refer to Figure 1 for diagram):

- `DQ_AI218_BIT_5V_IN` - Self-test that includes the reference voltage injected between the input resistors and PGA (input voltage has minimal effect).
  PGA uses the normal input (`IN1`) and reference voltage connected at S1/S4:

```
 data
 cl  0: 4.970019
 cl  1: 4.961645
 cl  2: 4.970648
 cl  3: 4.961592
 cl  4: 4.970771
 cl  5: 4.961286
 cl  6: 4.970609
 cl  7: 4.961606
(Received:12)

Press any key to continue
```

- `DQ_AI218_BIT_ALT_5V` - Self-test that tests from PGA on.
  PGA uses the alternate `IN2` reference voltage:

```
 data
 cl  0: 4.999726
 cl  1: 5.000513
 cl  2: 5.000182
 cl  3: 5.000392
 cl  4: 4.999915
 cl  5: 4.999661
 cl  6: 4.999976
 cl  7: 4.999677
(Received:12)

Press any key to continue
```

The actual voltage read for a passing self-test can be within 4% of the expected reference voltage.

For more information:

Please contact UEI support at support@ueidaq.com or call 508.921.4600 with any questions.