



UEI Test Adapters User Manual

Test Adapters for PowerDNx Boards

July 2021

PN Man-Test-Adapters

© Copyright 1998-2021 United Electronic Industries, Inc. All rights reserved.

No part of this publication may be reproduced, stored in a retrieval system, or transmitted, in any form by any means, electronic, mechanical, by photocopying, recording, or otherwise without prior written permission.

Information furnished in this manual is believed to be accurate and reliable. However, no responsibility is assumed for its use, or for any infringement of patents or other rights of third parties that may result from its use.

All product names listed are trademarks or trade names of their respective companies.

See the UEI website for complete terms and conditions of sale:

<http://www.ueidaq.com/cms/terms-and-conditions>



Contacting United Electronic Industries:

Mailing Address:

249 Vanderbilt Avenue
Norwood, MA 02062
U.S.A.

Shipping Address:

24 Morgan Drive
Norwood, MA 02062
U.S.A.

For a list of our distributors and partners in the US and around the world, please contact a member of our support team:

Support:

Telephone: (508) 921-4600
Fax: (508) 668-2350

Also see the FAQs and online "Live Help" feature on our web site.

Internet Support:

Support: support@ueidaq.com
Website: www.ueidaq.com
FTP Site: <ftp://ftp.ueidaq.com>

Product Disclaimer:

WARNING!

DO NOT USE PRODUCTS SOLD BY UNITED ELECTRONIC INDUSTRIES, INC. AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

Products sold by United Electronic Industries, Inc. are not authorized for use as critical components in life support devices or systems. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness. Any attempt to purchase any United Electronic Industries, Inc. product for that purpose is null and void and United Electronic Industries Inc. accepts no liability whatsoever in contract, tort, or otherwise whether or not resulting from our or our employees' negligence or failure to detect an improper purchase.

Specifications in this document are subject to change without notice. Check with UEI for current status.

Table of Contents

Introduction	1
1.1 Overview	1
1.2 Organization of this Manual	1
1.3 Manual Conventions	1
1.4 Before You Begin	1
1.5 Related Resources	2
101 Test Adapter	3
2.1 General Description	3
2.2 Analog I/O Loopback	4
2.3 Industrial Digital I/O Loopback	5
2.4 TTL Digital I/O Loopback	6
2.5 Serial Loopback	6
2.6 I2C Port Testing	6
2.6.1 Temperature Data Format	7
2.7 Pinout	8
2.8 Using the 101 Test Adapter	8
2.9 Specifications	9
201 Test Adapter	10
3.1 General Description	10
3.2 Device Architecture	11
3.3 Using the 201 Test Adapter	12
3.4 Specifications	13
201-to-308 Test Adapter	14
4.1 Features	14
4.2 General Description	15
4.3 Device Architecture	16
4.4 Using the 201-to-308 Test Adapter	18
4.5 Specifications	19
202 Test Adapter	20
5.1 General Description	20
5.2 Device Architecture	21
5.3 Using the 202 Test Adapter	22
5.4 Specifications	23
205 Test Adapter	24



6.1	General Description	24
6.2	Device Architecture	24
6.3	Using the 205 Test Adapter	25
6.4	Specifications	26
207/217 Test Adapter		27
7.1	General Description	27
7.2	Device Architecture	28
7.3	Using the 207/217 Test Adapter	29
7.4	Specifications	30
207-to-332 Test Adapter		31
8.1	Features	31
8.2	General Description	31
8.3	Device Architecture	33
8.4	Using the 207-to-332 Test Adapter	34
8.5	Specifications	35
208 Test Adapter		36
9.1	General Description	36
9.2	Device Architecture	37
9.3	Using the 208 Test Adapter	38
9.4	Specifications	39
211 Test Adapter		40
10.1	Features	40
10.2	General Description	40
10.3	Device Architecture	41
10.4	Using the 211 Test Adapter	42
10.5	Specifications	43
225 Test Adapter		44
11.1	General Description	44
11.2	Device Architecture	45
11.3	Using the 225 Test Adapter	46
11.4	Specifications	47
254 Test Adapter		48
12.1	Features	48
12.2	General Description	48
12.3	Device Architecture	49



12.4	Using the 254 Test Adapter	50
12.5	Specifications	51
255/256 Test Adapter		52
13.1	Features	52
13.2	General Description	52
13.3	Device Architecture	53
13.4	Using the 255/256 Test Adapter	54
13.5	Specifications	55
401-to-402 Test Adapter		56
14.1	General Description	56
14.2	Device Architecture	57
14.3	Using the 401-to-402 Test Adapter	58
14.4	Specifications	59
403 Test Adapter		60
15.1	General Description	60
15.2	Device Architecture	61
15.3	Using the 403 Test Adapter	62
15.4	Specifications	63
404/405/406 Test Adapter		64
16.1	General Description	64
16.2	Device Architecture	65
16.3	Using the 404/405/406 Test Adapter	66
16.4	Specifications	67
429-566 Test Adapter		68
17.1	General Description	68
17.2	Pinout	71
17.3	Using the 429-566 Test Adapter	71
17.4	Specifications	72
432/433 Test Adapter		73
18.1	General Description	73
18.2	Device Architecture	74
18.3	Using the 432/433 Test Adapter	75
18.4	Specifications	76
448/449 Test Adapter		77
19.1	General Description	77



19.2	Using the 448/449 Test Adapter	79
19.3	Specifications	80
501 Test Adapter		81
20.1	General Description	81
20.2	Device Architecture	82
20.3	Using the 501 Test Adapter	83
20.4	Specifications	84
503 Test Adapter		85
21.1	General Description	85
21.2	Using the 503 Test Adapter	86
21.3	Specifications	87
508 Test Adapter		88
22.1	General Description	88
22.2	Device Architecture	89
22.3	Using the 508 Test Adapter	90
22.4	Specifications	91
601 Test Adapter		92
23.1	General Description	92
23.2	Device Architecture	93
23.3	Using the 601 Test Adapter	95
23.4	Specifications	95
604 Test Adapter		96
24.1	General Description	96
24.2	Device Architecture	97
24.3	Using the 604 Test Adapter	99
24.4	Specifications	99
1553 Test Adapter		100
25.1	General Description	100
25.2	Using the 1553 Test Adapter	102
25.3	Specifications	103



List of Figures

	Introduction	1
	101 Test Adapter	3
2-1	Photo of 101 Test Adapter	3
2-2	Schematic of Analog Loopback Channel	4
2-3	Industrial Digital I/O Channel Configuration	5
2-4	External Power Supply Connector	5
2-5	TTL Digital I/O Channel Configuration	6
2-6	Schematic of Serial Port Loopback Circuit	6
2-7	Schematic of I2C Port Test Circuit	7
2-8	Example Data from ADT7420	7
2-9	Pinout of DNx-TADP-101 and MF-101	8
	201 Test Adapter	10
3-1	Photo of 201 Test Adapter	10
3-2	Block Diagram of 201 Test Adapter	11
3-3	Schematic of 201 Test Adapter	12
	201-to-308 Test Adapter	14
4-1	Photo of 201-to-308 Test Adapter	15
4-2	Block Diagram of 201-to-308 Test Adapter	16
4-3	Schematic of 201-to-308 Test Adapter	17
	202 Test Adapter	20
5-1	Photo of 202 Test Adapter	20
5-2	Block Diagram of 202 Test Adapter	21
5-3	Schematic and Pinout of 202 Test Adapter	22
	205 Test Adapter	24
6-1	Block Diagram of 205 Test Adapter	24
6-2	Schematic and Pinout of 205 Test Adapter	25
	207/217 Test Adapter	27
7-1	Photo of 207/217 Test Adapter	27
7-2	Block Diagram of 207/217 Test Adapter	28
7-3	Schematic of 207/217 Test Adapter	29
	207-to-332 Test Adapter	31
8-1	Photo of 207-to-332 Test Adapter	31
8-2	Block Diagram of 207-to-332 Test Adapter	33
8-3	Schematic and Pinout of 207-to-332 Test Adapter	34
	208 Test Adapter	36
9-1	Photo of 208 Test Adapter	36
9-2	Block Diagram of 208 Test Adapter	37
9-3	Schematic and Pinout of 208 Test Adapter	38
	211 Test Adapter	40
10-1	Photo of 211 Test Adapter	40
10-2	Block Diagram of 211 Test Adapter	41
10-3	Schematic and Pinout of 211 Test Adapter	42
	225 Test Adapter	44
11-1	Photo of 225 Test Adapter	44
11-2	Schematic and Pinout of 225 Test Adapter	45



	254 Test Adapter	48
12-1	Photo of 254 Test Adapter	48
12-2	Channel Configuration of 254 Test Adapter	49
12-3	Schematic and Pinout of 254 Test Adapter	50
	255/256 Test Adapter	52
13-1	Photo of 255/256 Test Adapter	52
13-2	Channel Configuration of 255/256 Test Adapter	53
13-3	Schematic and Pinout of 255/256 Test Adapter	54
	401-to-402 Test Adapter	56
14-1	Photo of 401-to-402 Test Adapter	56
14-2	Block Diagram of 401-to-402 Test Adapter	57
14-3	Schematic and Pinout of 401-to-402 Test Adapter	58
	403 Test Adapter	60
15-1	Photo of 403 Test Adapter	60
15-2	Block Diagram of 403 Test Adapter	61
15-3	Schematic and Pinout of 403 Test Adapter	62
	404/405/406 Test Adapter	64
16-1	Photo of 404/405/406 Test Adapter	64
16-2	Block Diagram of 404/405/406 Test Adapter	65
16-3	Schematic and Pinout of 404/405/406 Test Adapter	66
	429-566 Test Adapter	68
17-1	Photo of 429-566 Test Adapter	68
17-2	Block Diagram of 429-566 Test Adapter	69
17-3	Schematic of the 429-566 Test Adapter	70
17-4	Pinout of 429-566 Test Adapter	71
	432/433 Test Adapter	73
18-1	Photo of 432/433 Test Adapter	73
18-2	Output Circuit Diagram of DIO-432	74
18-3	Output Circuit Diagram of DIO-433	74
18-4	Schematic and Pinout of 432/433 Test Adapter	75
	448/449 Test Adapter	77
19-1	Photo of 448/449 Test Adapter	77
19-2	Schematic and Pinout of 448/449 Test Adapter	78
19-3	Divider Circuit on Odd Channels	78
	501 Test Adapter	81
20-1	Photo of 501 Test Adapter	81
20-2	Block Diagram of 501 Test Adapter	82
20-3	Schematic of 501 Test Adapter	83
	503 Test Adapter	85
21-1	Photo of 503 Test Adapter	85
21-2	Block Diagram of 503 Test Adapter	85
21-3	Schematic of 503 Test Adapter	86
	508 Test Adapter	88
22-1	Photo of 508 Test Adapter	88
22-2	Block Diagram of 508 Test Adapter	89
22-3	Schematic of 508 Test Adapter	90
	601 Test Adapter	92



23-1	Photo of 601 Test Adapter	92
23-2	Connection Diagram of CT-601 Board and 601 Test Adapter	93
23-3	Schematic of 601 Test Adapter	94
	604 Test Adapter	96
24-1	Photo of 604 Test Adapter	96
24-2	Connection Diagram of QUAD-604 and 604 Test Adapter	97
24-3	Schematic of 604 Test Adapter	98
	1553 Test Adapter	100
25-1	Photo of 1553 Test Adapter	100
25-2	Block Diagram of 1553 Test Adapter	101
25-3	Schematic of 1553 Test Adapter	102



List of Tables

	Introduction	1
	101 Test Adapter	3
2-1	Analog Channel Configuration	4
2-2	Technical Specifications for the DNx-TADP-101	9
	201 Test Adapter	10
3-1	Technical Specifications for the DNx-TADP-201	13
	201-to-308 Test Adapter	14
4-1	Technical Specifications	19
	202 Test Adapter	20
5-1	Technical Specifications for the 202 Test Adapter	23
	205 Test Adapter	24
6-1	Technical Specifications for the 205 Test Adapter	26
	207/217 Test Adapter	27
7-1	Technical Specifications for the 207/217 Test Adapter	30
	207-to-332 Test Adapter	31
8-1	Technical Specifications	35
	208 Test Adapter	36
9-1	Technical Specifications for the 208 Test Adapter	39
	211 Test Adapter	40
10-1	Technical Specifications for the 211 Test Adapter	43
	225 Test Adapter	44
11-1	Technical Specifications for the 225 Test Adapter	47
	254 Test Adapter	48
12-1	Technical Specifications (when used with the AI-254)	51
	255/256 Test Adapter	52
13-1	Technical Specifications	55
	401-to-402 Test Adapter	56
14-1	Technical Specifications for the 401-to-402 Test Adapter	59
	403 Test Adapter	60
15-1	Technical Specifications for the 403 Test Adapter	63
	404/405/406 Test Adapter	64
16-1	Technical Specifications for the 404/405/406 Test Adapter	67
	429-566 Test Adapter	68
17-1	Technical Specifications for the 429-566 Test Adapter	72
	432/433 Test Adapter	73
18-1	Technical Specifications for the 432/433 Test Adapter	76
	448/449 Test Adapter	77
19-1	Technical Specifications for the 448/449 Test Adapter	80
	501 Test Adapter	81
20-1	Technical Specifications for the 501 Test Adapter	84
	503 Test Adapter	85



21-1	Technical Specifications for the 503 Test Adapter	87
	508 Test Adapter	88
22-1	Technical Specifications for the 508 Test Adapter	91
	601 Test Adapter	92
23-1	Source and Destination of Channel Signals	94
23-2	Technical Specifications for the 601 Test Adapter	95
	604 Test Adapter	96
24-1	Source and Destination of Channel Signals	98
24-2	Technical Specifications for the 604 Test Adapter	99
	1553 Test Adapter	100
25-1	Technical Specifications for the 1553 Test Adapter	103



Introduction

1.1 Overview

This manual describes the design and functional operation of UEI's test adapters. Test adapters are used for preliminary testing and troubleshooting of UEI I/O boards.

A quick reference guide for the test adapters may be downloaded from UEI's website at <https://www.ueidaq.com/products/uei-test-adapters>.

1.2 Organization of this Manual

Each chapter is dedicated to a specific test adapter and titled with the name(s) of the associated I/O board(s). Chapters are arranged in the manual according to I/O board number.

1.3 Manual Conventions

The following conventions are used throughout this manual:



Tips are designed to highlight quick ways to get the job done or to reveal good ideas you might not discover on your own.



CAUTION! *advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

NOTE: Notes alert you to important information.

Typeface	Description	Example
bold	field or button names	Click Scan Network
»	hierarchy to get to a specific menu item	File » New
<code>fixed</code>	source code to be entered verbatim	<code>session.CleanUp()</code>
<code><brackets></code>	placeholder for user-defined text	<code>pdna://<IP address></code>
<i>italics</i>	path to a file or directory	<i>C:/Program Files</i>

1.4 Before You Begin



No Hot Swapping!

Before plugging any I/O connector into the Cube or Rack, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.



Check Your Firmware



Ensure that the firmware installed on the Cube or Rack CPU matches the UEI software version installed on your PC. The IOM is shipped with pre-installed firmware and a matching software installation. If you upgrade your software installation, you must also update the firmware on your Cube or Rack CPU. Instructions for updating firmware are provided in the UEI chassis user manuals.

1.5 Related Resources

For information about the I/O board associated with each test adapter, please refer to the website or the documentation folder included with the software installation. On Windows, these resources can be found from the desktop by clicking **Start » All Program » UEI**.

UEI's website includes other user resources such as application notes, FAQs, tutorials, and videos. In particular, the glossary of terms may be helpful when reading through this manual: <https://www.ueidaq.com/glossary>

Additional questions? Please email UEI Support at support@ueidaq.com or call 508-921-4600.



101 Test Adapter

The 101 Test Adapter (p/n DNx-TADP-101) is an accessory designed for testing UEI's DNx-MF-101 Multifunction I/O Board.

2.1 General Description

Under software control, the 101 Test Adapter facilitates testing of all channels on a DNx-MF-101 Multifunction I/O Board:

- 16 single-ended or 8 fully differential analog inputs
- 2 analog outputs
- 16 industrial digital I/O bits
- 6 TTL digital bits (4 I/O, 1 input, 1 output)
- 1 RS-232/422/485 serial port
- 1 I²C port (master and slave)

Loopback tests can be performed between analog inputs and outputs, industrial digital inputs and outputs, TTL inputs and outputs, and serial receiver and transmitter. A built-in ADT7420 temperature sensor is used to verify I²C port functionality.

Industrial digital outputs draw power from a user-supplied 0-55V source. If the external supply is disconnected, +VIn is pulled up to an internal +60 V supply by a 2 MΩ resistor. An on-board LED indicates the status of VIn

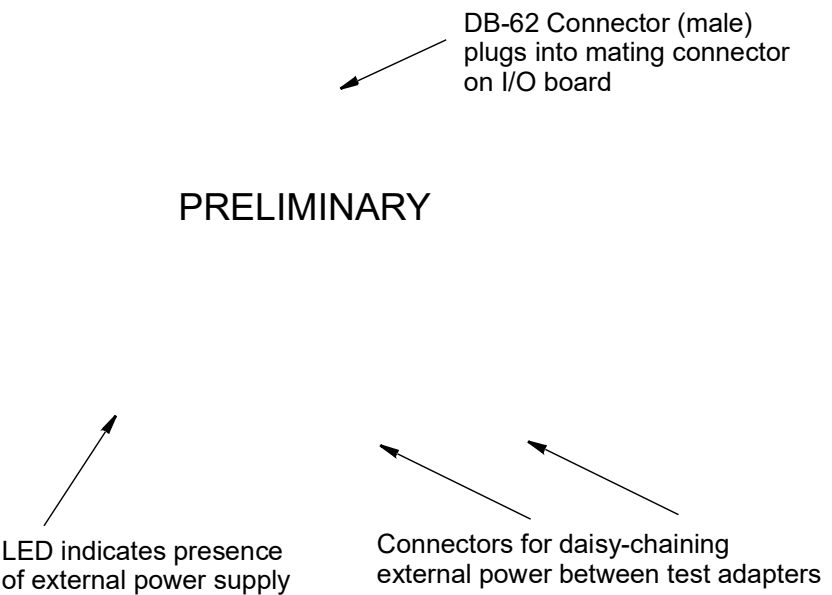


Figure 2-1 Photo of 101 Test Adapter

2.2 Analog I/O Loopback

The 101 Test Adapter connects two analog output channels to analog input channels as shown in **Table 2-1**.

Table 2-1 Analog Channel Configuration

Single-Ended Input	Differential Input	Analog Output
AI0	AI0+	AOut0
AI1	AI0-	AOut1
AI2	AI1+	AOut1
AI3	AI1-	AOut0
AI4	AI2+	AOut0
AI5	AI2-	AOut1
AI6	AI3+	AOut1
AI7	AI3-	AOut0
AI8	AI4+	AOut0
AI9	AI4-	AOut1
AI10	AI5+	AOut1
AI11	AI5-	AOut0
AI12	AI6+	AOut0
AI13	AI6-	AOut1
AI14	AI7+	AOut1
AI15	AI7-	AOut0

Analog outputs can be tested in both voltage and current output mode. In voltage output mode, differential input measurements take the difference of AOut1 and AOut0. For example, setting AOut1 to -5V and AOut0 to +2V should return +7V on AI6+/- and -7V on AI7+/-.

Use single-ended analog inputs to test current output mode. Since each analog pin is tied to ground via a 2.2kΩ resistor (**Figure 2-2**), the output current I encounters a total resistance of 1.1kΩ, creating a voltage of $I \cdot 1.1k\Omega$.

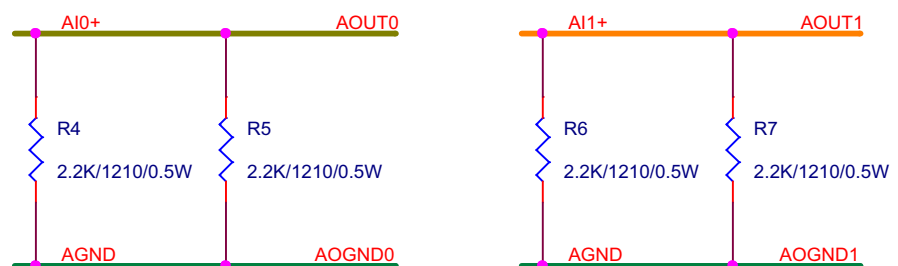


Figure 2-2 Schematic of Analog Loopback Channel



2.3 Industrial Digital I/O Loopback

The 101 Test Adapter connects FET-based digital I/O channels 0-7 to channels 8-15 as shown in **Figure 2-3**.

Industrial digital outputs are designed to draw power from an external supply, which is protected by a resettable fuse (**Figure 2-4**). Two power connectors are provided, allowing daisy-chaining of external power to other test adapters. When using the test adapter, all 4 blocks of DIO channels (16 channels total) are connected to the same power supply.

If +VIN is disconnected, the MF-101 automatically pulls up the positive rail to an internal +60 V supply using a 2 MΩ resistor. The internal supply is only meant to be used for very basic testing and to prevent accidental floating inputs on the MF-101. A disconnected +VIN may cause unexpected digital input readings as the outputs switch ON/OFF.

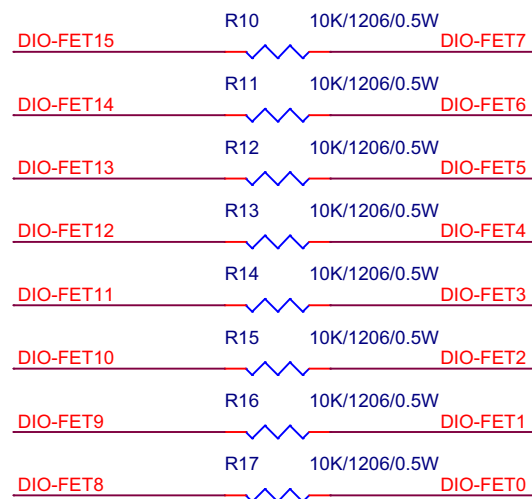


Figure 2-3 Industrial Digital I/O Channel Configuration

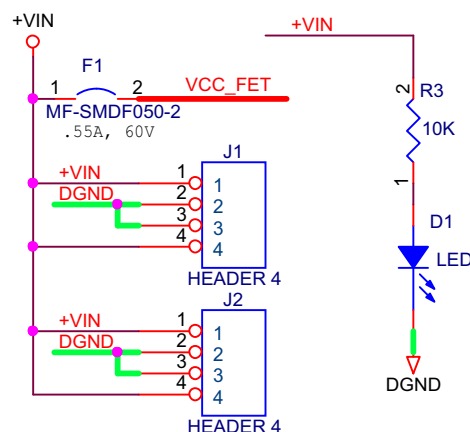


Figure 2-4 External Power Supply Connector



2.4 TTL Digital I/O Loopback

TTL digital I/O channels 0-1 are tied to channels 2-3 as shown in **Figure 2-5**. TRIGIN reads the TRIGOUT signal.

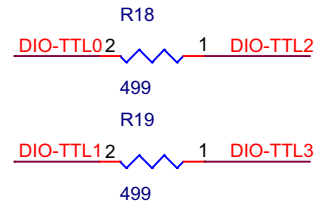


Figure 2-5 TTL Digital I/O Channel Configuration

2.5 Serial Loopback

The serial port can be tested in either RS-232 or RS-485 mode. As shown in **Figure 2-6**, TRIGOUT controls the relay that switches between the two modes. Set TRIGOUT=1 to use the port in RS-232 mode, and set TRIGOUT=0 to use RS-422/485 mode. Remember to disable the internal loopback software setting if you want to make use of this external loopback test circuit.

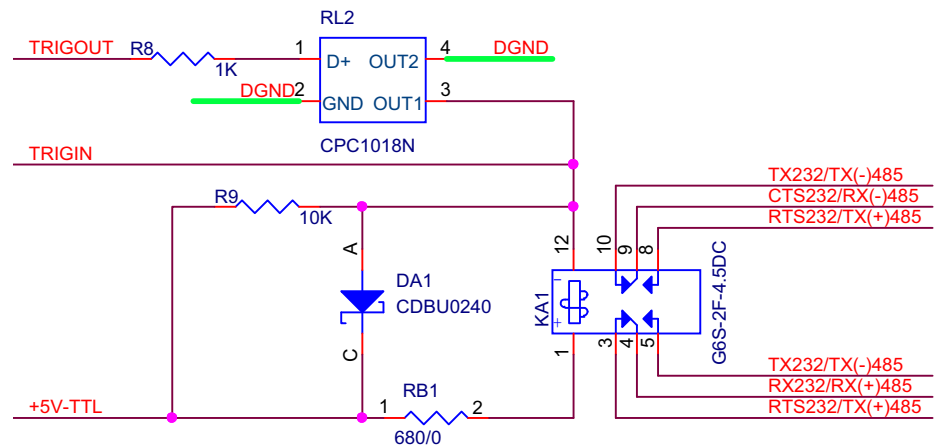


Figure 2-6 Schematic of Serial Port Loopback Circuit

2.6 I2C Port Testing

The 101 Test Adapter includes an ADT7420 temperature sensor wired to the I²C bus as shown in **Figure 2-7**. You can use the sensor to test both the MF-101 master module and Bus Monitor slave module. Example programs for reading the temperature sensor are provided in the “Sample101” (low-level C code) and “I2CReadSensor” (high-level C++ code) folders. Note that the I²C address of the ADT7420 is set to 0x48.



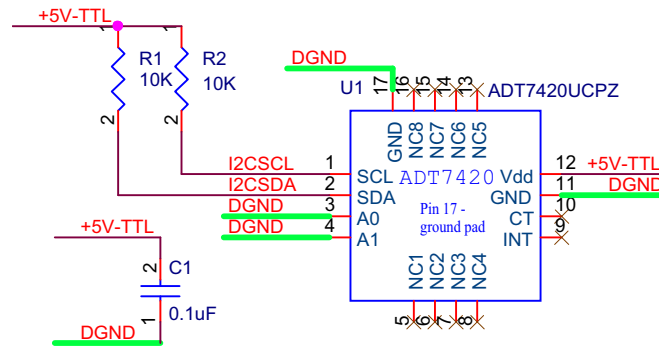


Figure 2-7 Schematic of I²C Port Test Circuit

2.6.1 Temperature Data Format

By default, the ADT7420 encodes the temperature in a 13-bit number. Therefore, the MF-101 master should be programmed to read two bytes from the sensor and discard the three LSBs.

An example is illustrated in **Figure 2-8**. If the master receives `rx_data[0]=0xf` and `rx_data[1]=0x178`, then the raw temperature data equals 0x1ef (binary: 0 0001 1110 1111, decimal: 495). Data bit 13 indicates whether the temperature is positive or negative. If the temperature is positive, divide the raw temperature data number by 16 to obtain the temperature in °C. In this example, temperature = 495/16 = 30.9 °C. If the sign bit is 1, subtract 8192 from the raw temperature data number before dividing by 16. Refer to the ADT7420 datasheet for additional details on this conversion.

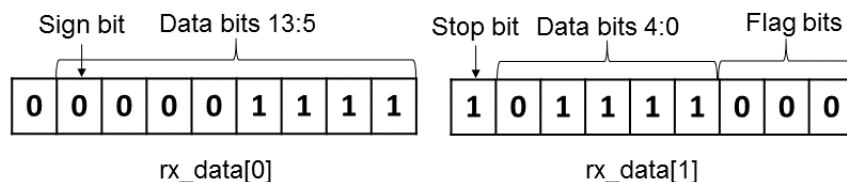


Figure 2-8 Example Data from ADT7420



2.7 Pinout

The 101 Test Adapter plugs directly into the DB-62 mating connector of the MF-101. The pinout for the 101 Test Adapter is shown below in **Figure 2-9**.

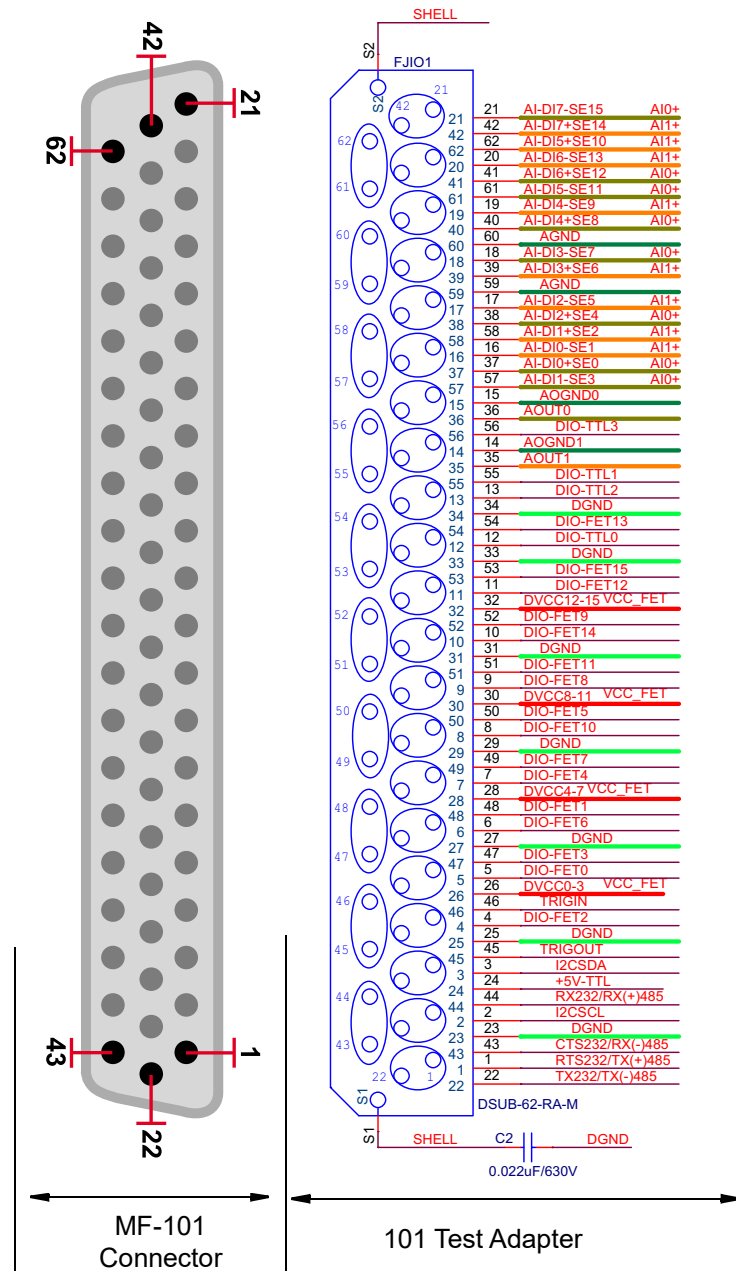


Figure 2-9 Pinout of DNX-TADP-101 and MF-101

2.8 Using the 101 Test Adapter

Testing the DNX-MF-101 Multifunction I/O Board with the DNX-TADP-101 requires you to develop a simple program to acquire data and display the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNX-MF-101 User Manual for information about programming the MF-101.



2.9 Specifications

Technical specifications for the 101 Test Adapter are listed in **Table 2-2** below.

Table 2-2 Technical Specifications for the DNx-TADP-101

Channel Configurations	
Analog IO	2 outputs connected to 16 inputs
Analog Output Modes	Voltage or current
Industrial DIO	DIO15:8 paired with DIO7:0
TTL DIO	TTL0:1 paired to TTL2:3 TRIGIN connected to TRIGOUT
Serial Port	Receiver loops back to Transmitter
Serial Interface Modes	RS-232 or RS-422/485
I2C Port	Bus connected to ADT7420 slave device
Power Supply Specifications	
Power Source	Supplied by user
Input Range	0-55 VDC
Protection	0.55 Amp, 60V resettable fuse
General Specifications	
Connectors	DB-62 male, two 4-pin Molex RA
Overvoltage Protection	-40V to +55V
ESD Protection	15 kV
Power Consumption	Less than 1 W
Operating Temperature	-40°C to +85°C
Operating Humidity	90%, non-condensing



201 Test Adapter

The 201 Test Adapter (p/n DNx-TADP-201) is an accessory designed for testing UEI's DNx-AI-201-100 Analog Input Board.

3.1 General Description

Under software control, the 201 Test Adapter facilitates DC tests on all 24 single-ended or 12 differential channels of a DNx-AI-201-100 Analog Input Board. The AI-201 is designed to accept differential analog voltage inputs within a $\pm 15V$ range at sampling rates up to 100kS/s per channel at a resolution of 16 bits.

The 201 Test Adapter receives a $\pm 18VDC$ reference voltage from the AI-201 and converts it to +2.5V, -2.5V, +5V, and -5V voltages. These voltages are fed back as analog inputs to the AINn terminals of the AI-201 board.

The LED indicates the presence of the +18 VDC output from the AI-201.

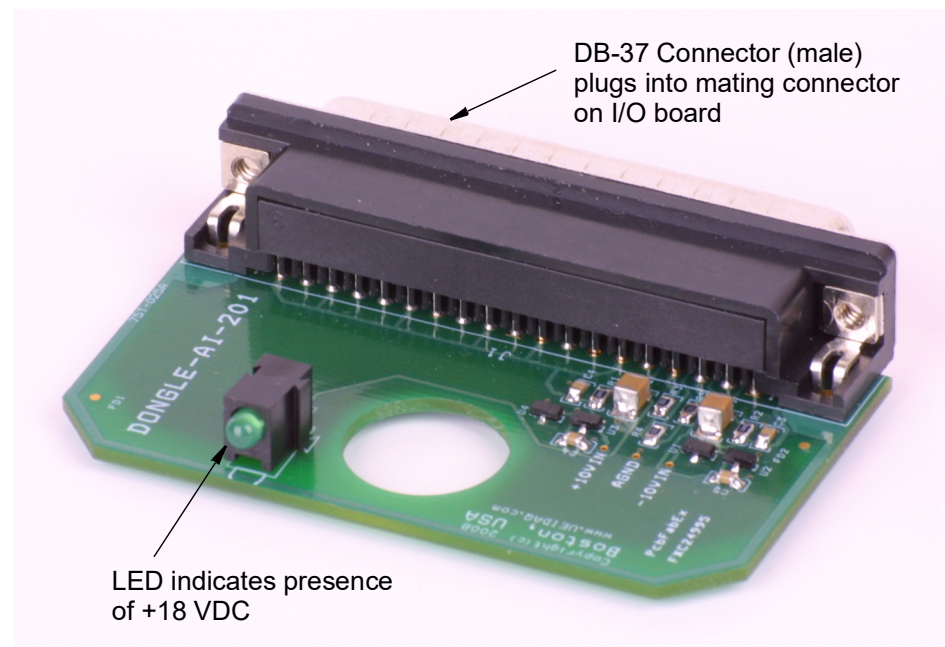


Figure 3-1 Photo of 201 Test Adapter



3.2 Device Architecture

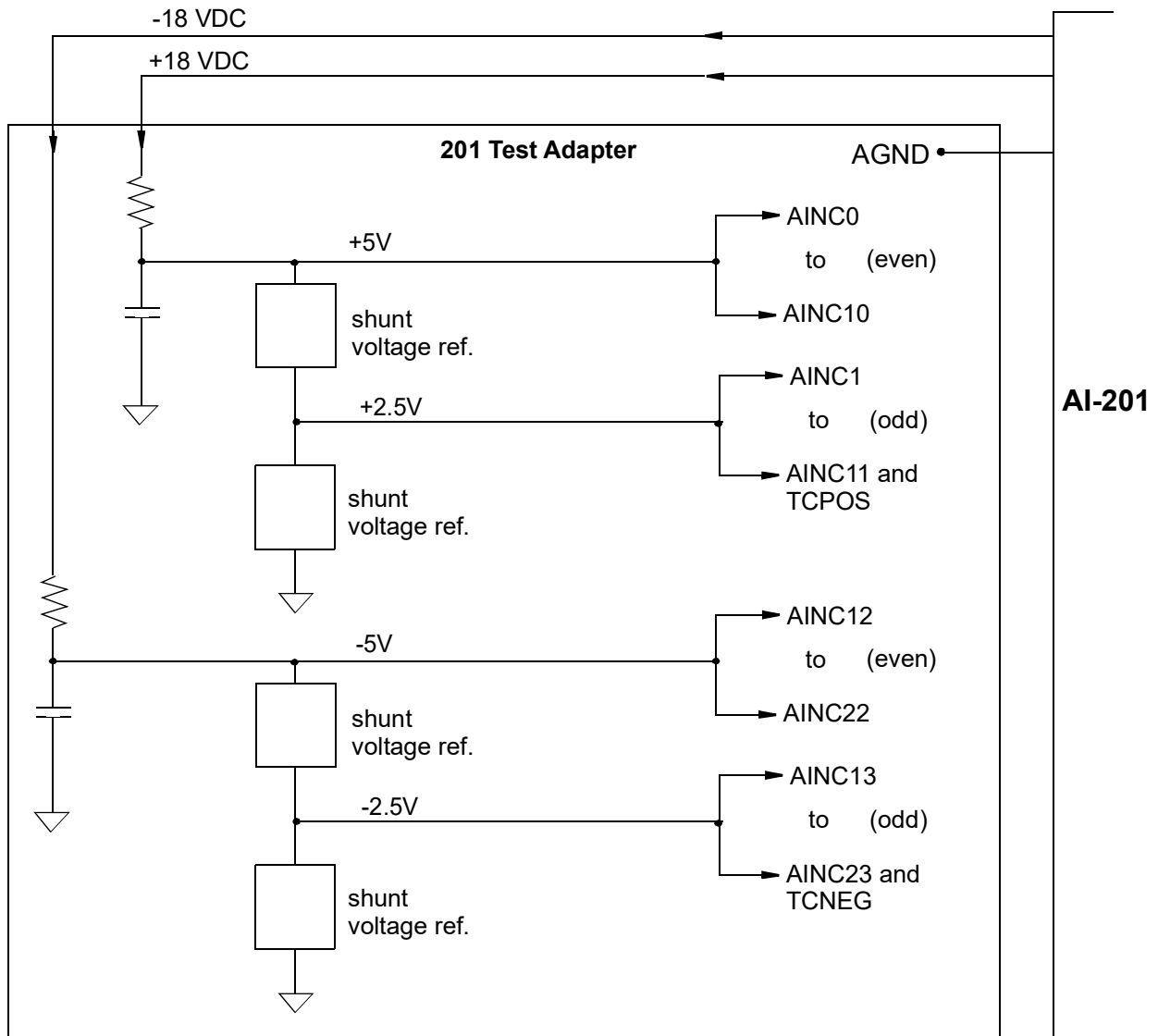


Figure 3-2 Block Diagram of 201 Test Adapter

As shown in **Figure 3-2** above, the AI-201 outputs two DC voltages (+18V and -18V) to the 201 Test Adapter on terminals 21 and 20, respectively. The +18V is dropped to +5V and distributed to inputs AINC0, 2, 4, 6, 8, and 10. The -18V is dropped to -5V and distributed to inputs AINC12, 14, 16, 18, and 20. The +5V is dropped to +2.5V and distributed to analog inputs AINC1, 3, 5, 7, 9, 11 and TCPOS. The -5V is dropped to -2.5V and distributed to inputs AINC13, 15, 17, 19, 21, 23, and TCNEG.

The 201 Test Adapter plugs directly into the DB-37 mating connector of the AI-201. The pinout for the 201 Test Adapter and AI-201 is shown below in **Figure 3-3** alongside the test adapter's schematic.



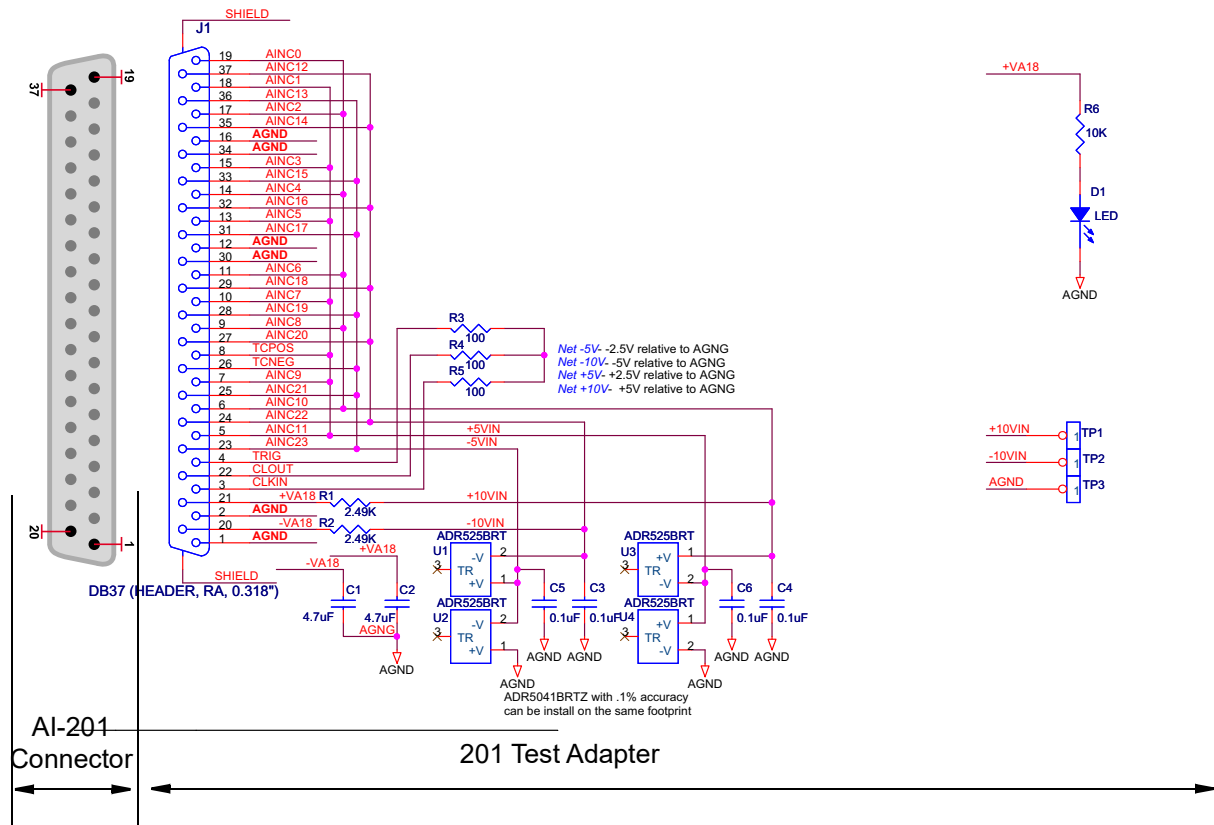


Figure 3-3 Schematic of 201 Test Adapter

3.3 Using the 201 Test Adapter

Testing the DNx-AI-201-100 Analog Input Board with the DNx-TADP-201 requires you to develop a simple program for performing DC tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-AI-201 User Manual for information about programming the AI-201.



3.4 Specifications

Technical specifications for the 201 Test Adapter are listed in **Table 3-1** below.

Table 3-1 Technical Specifications for the DNx-TADP-201

Channel Configurations	
Number of channels	12 differential ($\pm 15V$) 24 single-ended
Input Specifications	
Inputs to AI-201	DC Analog Voltage derived from AI-201 $\pm 18VDC$
Resolution	16 bits
Power Input to Test Adapter	$\pm 18VDC$ from AI-201
General Specifications	
Connector to AI-201	DB-37 male
Overvoltage Protection	-40V to +55V
ESD Protection	15 kV
Power Consumption	Less than 1 W
Operating Temperature	-40°C to +85°C
Operating Humidity	90%, non-condensing



201-to-308 Test Adapter

The 201-to-308 Test Adapter (p/n B-D-A-201-308-x and B-D-R-201-308-x) is an accessory designed for combination testing of UEI's DNx-AI-201-100 Analog Input Board and DNx-AO-308 Analog Output Boards of various types. The test adapter requires that the I/O boards be mounted in adjacent slots of a PowerDNA Cube or in adjacent positions of a DNR rack for testing to be performed.

4.1 Features

The key features of the 201-to-308 Test Adapter are:

- Facilitates basic testing of DNx-AI-201-100 Analog Input Board and DNx-AO-308 Analog Output Boards mounted in adjacent slots of a Cube or Rack
- Available in different versions for testing AI-201 in combination with AO-308, AO-308-350, AO-308-353, or AO-308-420
- Simulates analog voltage Inputs to all channels of an AI-201
- LED indicates presence of +15 VDC voltage source from AO-308
- Accepts ± 45 VDC daisy-chained external power source when configured as 201-308-353 Version
- Provides analog output sensing for 201-308-350 version

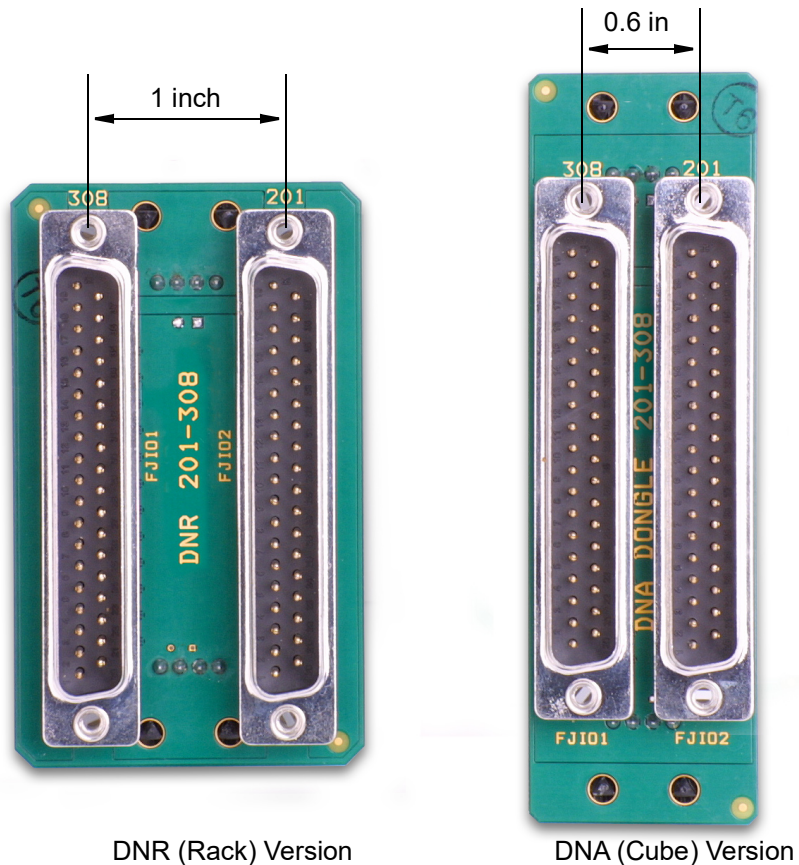


Figure 4-1 Photo of 201-to-308 Test Adapter

4.2 General Description

Under software control, the 201-to-308 Test Adapter facilitates tests between DNx-AI-201-100 Analog Input Board and DNx-AO-308 Analog Output Boards. The AI-201-100 is designed to accept 24 single-ended or 12 differential analog voltage inputs within a $\pm 15\text{V}$ range at sampling rates up to 100kS/s per channel at a resolution of 16 bits.

The 201-to-308 Test Adapter is offered in several different configurations, depending upon which IO boards are to be tested. First, all versions of the test adapters are offered in either a DNA (Cube) or DNR (Rack) model. Although functionally identical, they differ in the spacing between connectors — the DNA model connectors match the slot spacing of a PowerDNA Cube (0.6 in.); the DNR model connectors match the spacing of modules in a RACKtangle or HalfRACK housing (1.0 in.). The other variations between models relate to the type of AO-308 to be tested.

All versions receive +15VDC and -15VDC power from the AO-308 and +18VDC and -18VDC from the AI-201. The AO-308-353 version also receives $\pm 45\text{VDC}$ power from an external source via a daisy chain cable with resettable fuses in the +VEXT and -VEXT lines. This version is also populated with components required for the $\pm 40\text{VDC}$ output voltage range. An LED indicates the presence of the +V15 voltage.

The version for the basic AO-308 is populated with components with an output range of $\pm 10\text{VDC}$ and is powered from the AO-308. The version for the AO-308-350 is also designed for a high current analog voltage output range of $\pm 10\text{VDC}$, powered from the AO-308, but which also provides sense lines for more accurate measurement of output voltage on each 308 channel.

The version for the AO-308-353 is populated with components with an output range of $\pm 40\text{VDC}$ and is powered from an external source as noted above.

The version for the AO-308-420 is populated with resistors matched to the higher current ratings of the -420.

The 201 section of the adapter accepts analog voltage inputs from the eight analog outputs of the AO-308 board under test and senses them as analog voltage inputs on the AI-201. It also accepts as analog inputs the +V15, -V15 from the AO-308 board and the +V18, and -V18 from the AI-201 board.

The TRIG-IN, CLKIN, and CLKOUT of the 201 are connected to DIO1, DIO2, and DIO3 of the AO-308.

The LED indicates the presence of the +15 VDC output from the AO-308.



4.3 Device Architecture

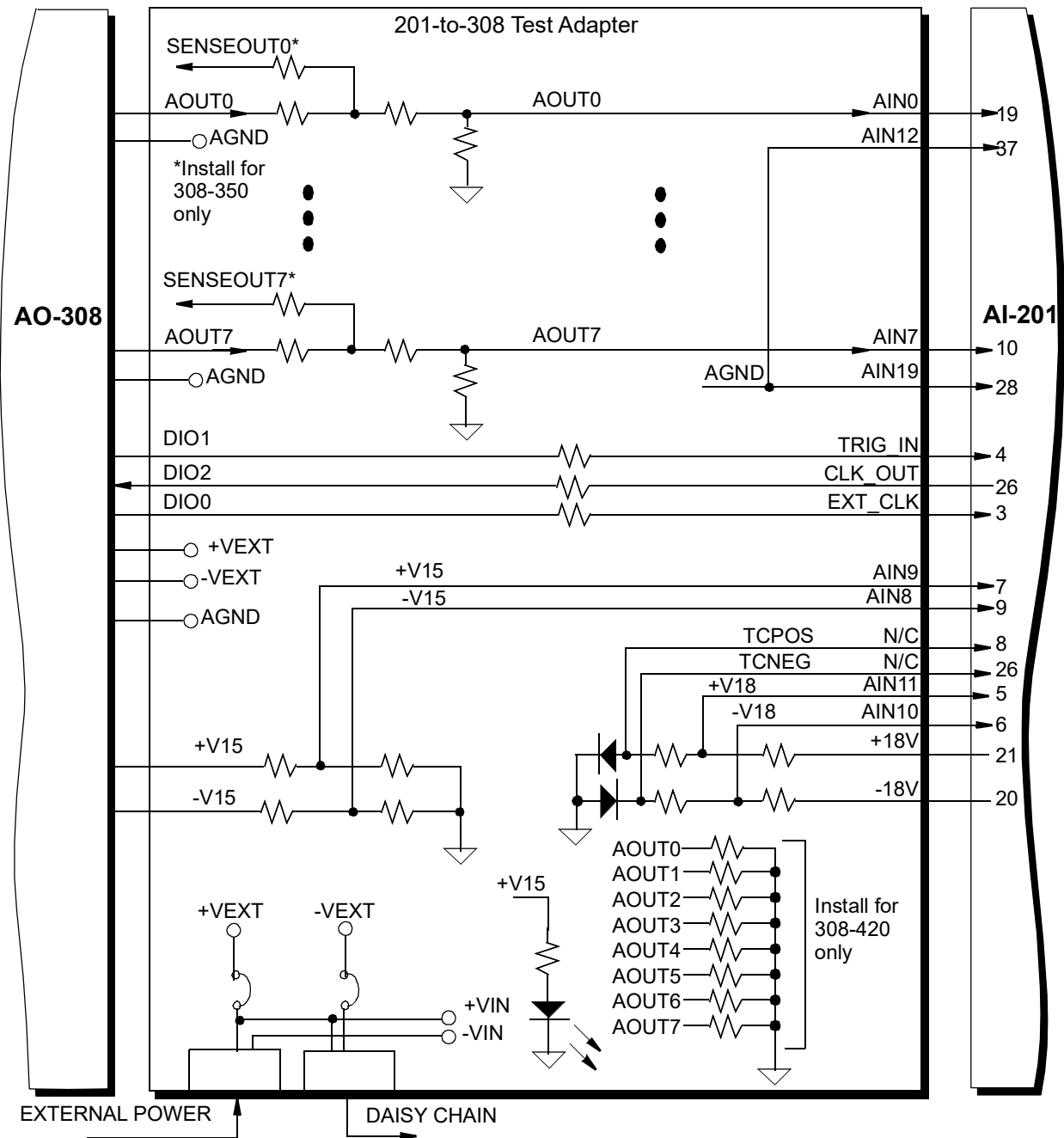


Figure 4-2 Block Diagram of 201-to-308 Test Adapter

As shown in **Figure 4-2** above, an AO-308-350 outputs -10 to +10 VDC analog voltages that are passed to the AI-201 as analog voltage inputs. The 308-350 version of the test adapter feeds back the actual voltage outputs via sense lines for each output.

In all versions of the 201-to-308 Test Adapter, the DIO1 output of the 308 is fed to the 201 as a TRIG input. DIO0 is also used as the AI-201 CLKIN input. The AI-201 CLKOUT signal is passed to the 308 on DIO2.

In the 308-353 version of the test adapter, resistors of values appropriate for a $\pm 40\text{VDC}$ range are used. Connectors are provided on the board to accept a $\pm 45\text{VDC}$ power from an external source and to accommodate a daisy chain to other devices. The external power circuit is protected by resettable fuses.

In the 308-420 version of the test adapter, resistors of values appropriate for the 4-20 mA current input signals are used for generating analog voltage inputs to the AI-201.

In all versions of the test adapter, the +VA18 and -VA18 voltages from the AI-201 are fed back as analog voltage inputs to the AI-201 on AINC10 and AINC11, and lower values to TCPOS and TCNEG. The +V15 and -V15 voltages from the AO-308 are input to the AI-201 as AINC9 and AINC8.

The pinouts of the AO-308, the AI-201, and the 201-to-308 Test Adapter are shown in **Figure 4-3**, along with a schematic of the test adapter circuit.

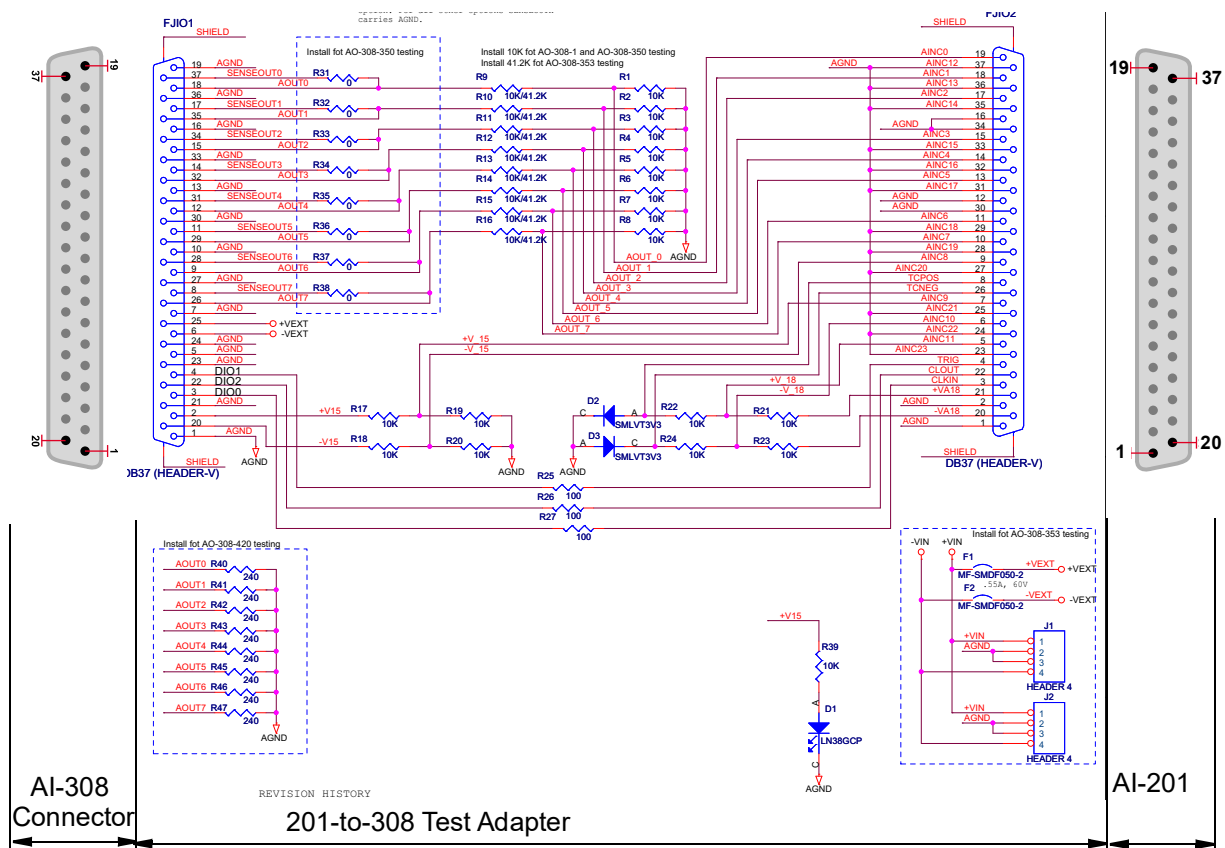


Figure 4-3 Schematic of 201-to-308 Test Adapter



- 4.4 Using the 201-to-308 Test Adapter** Testing the DNx-AI-201-100 Analog Input Board and DNx-AO-308 Analog Output Boards with the 201-to-308 Test Adapter requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. In particular, UEI Framework contains examples in the Analog Input folders and Analog Output folders that can be used to operate the AI-201 and AO-308 boards together. Please refer to the DNx-AI-201 and AO-308 User Manuals for information about programming the AI-201 and AO-308.



4.5 Specifications Technical specifications for the 201-to-308 Test Adapter are listed in **Table 4-1** below.

Table 4-1 Technical Specifications

Channel Configurations	
No. of channels	8 in, 12 out
Isolation	350 Vrms (chan-to-chan and chan-to-chassis)
Input/Output Specifications	
Inputs	8 analog voltage from AO-308, 3 DIO from AO-308 and AI-201
Outputs	8 analog voltage sense (± 10 VDC) for 308-350, Two ± 18 VDC, Two ± 15 VDC
Resolution	16 bits
Power Input	+45 VDC from external source for AO-308-353 only, (daisy-chained)
Power Output	+V15, -V15 to AI-201
General Specifications	
Connector	Two DB-37 male
Overvoltage protection	-40V to +55V
ESD Protection	2000 V ESD
Power Consumption	Less than 1 W
Operating Temperature	-40°C to +85°C
Operating Humidity	0 to 95%, non-condensing



202 Test Adapter

The 202 Test Adapter (p/n DNx-TADP-202) is an accessory designed for testing UEI's DNx-AI-202 Analog Current Input Board.

5.1 General Description

Under software control, the 202 Test Adapter facilitates tests on all 12 differential input channels of a DNx-AI-202 Analog Current Input Board. The AI-202 is designed to accept differential analog current inputs within any of three ranges ($\pm 1.5\text{mA}$, $\pm 15\text{mA}$, or $\pm 150\text{mA}$) at sampling rates up to 16 kS/s aggregate.

The 202 Test Adapter receives a +18V reference voltage from the AI-202 and converts it to a +10VDC voltage, which drives a current through the resistors connected across the terminals of the differential inputs of the AI-202 board. The current through the resistors, which are all connected in series by the test adapter, produces voltage drops that, in turn, are measured as analog voltage inputs to the AI-202. An opto-relay in the test adapter switches resistance values to give two current values through the input shunt resistors.

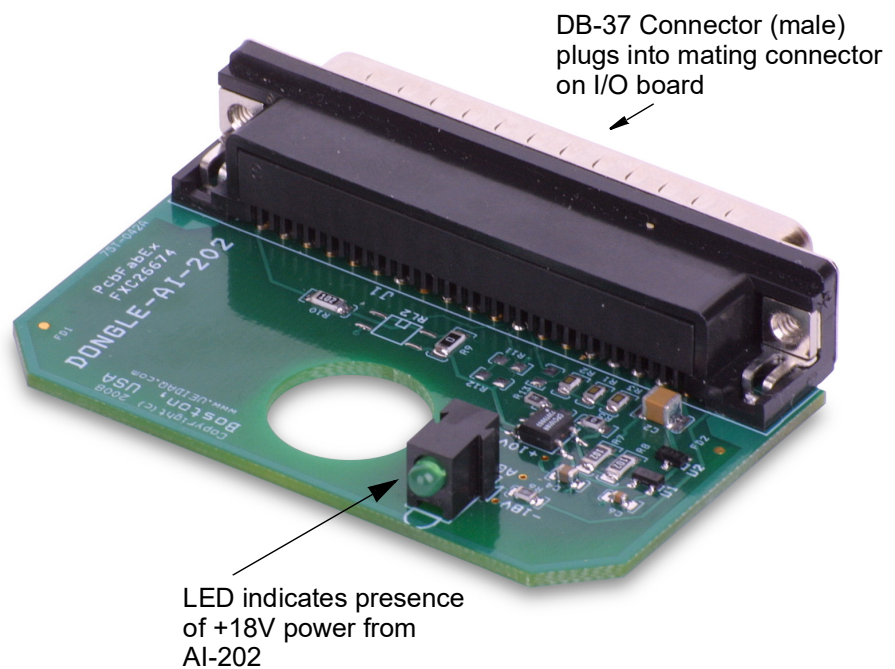


Figure 5-1 Photo of 202 Test Adapter



5.2 Device Architecture

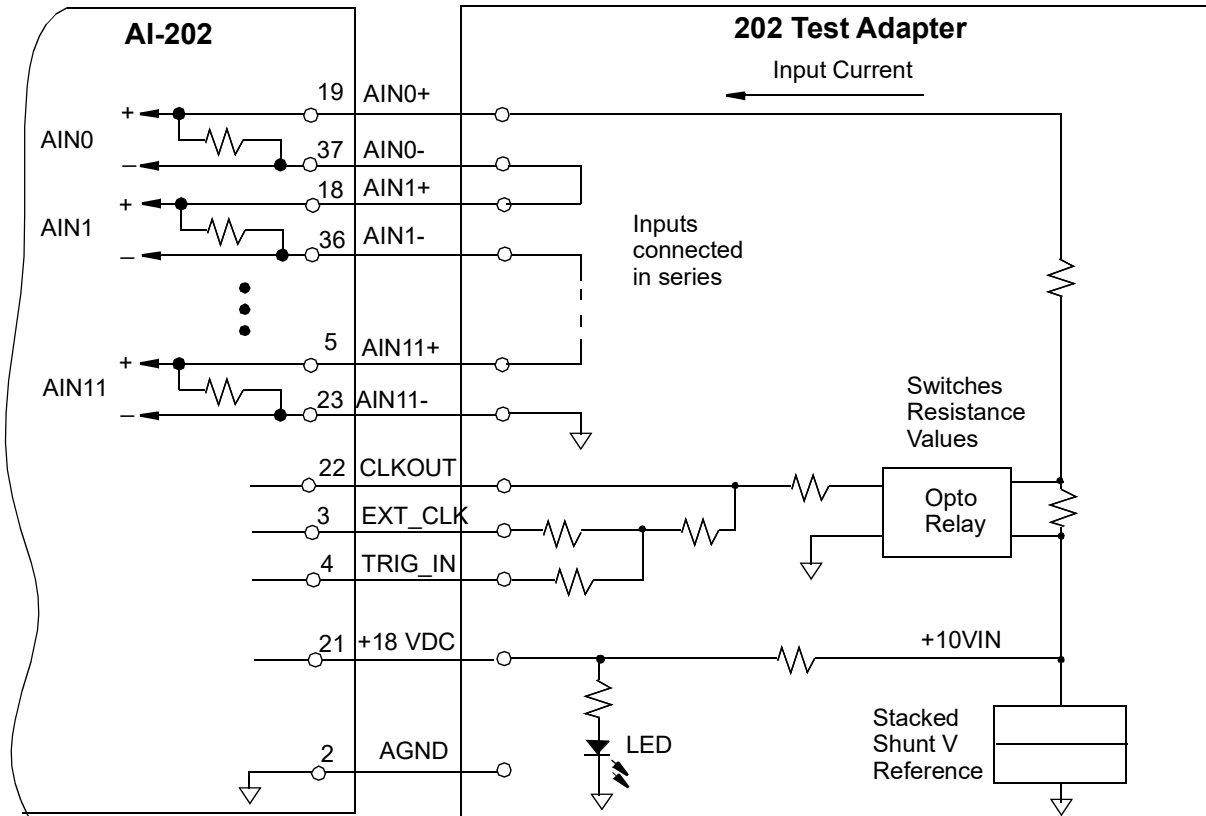


Figure 5-2 Block Diagram of 202 Test Adapter

As shown in **Figure 5-2** above, the AI-202 outputs a DC voltage (+18V) to the Test Adapter. This voltage is regulated by a shunt voltage reference to +10VDC (+VIN), which is then fed through all AI-202 input shunt resistors in series to ground. The voltage drops through the series of input shunt resistors produce voltages on each that are sensed as input signals for the AI-202. These measured values are then compared to known reference values for testing performance of the AI-202.

An opto-relay changes the value of a resistor in the series circuit for all of the AI-202 input shunt resistors, thus making it possible to sense all inputs at two different values of current.

A circuit is also included for testing the TC POS and NEG leads, a feature not currently implemented in the AI-202.

An LED on the Test Adapter indicates presence of the +18V supplied by the AI-202.

The pinouts of the AI-202 and the 202 Test Adapter are shown in **Figure 5-3**, along with a schematic of the Test Adapter circuit.



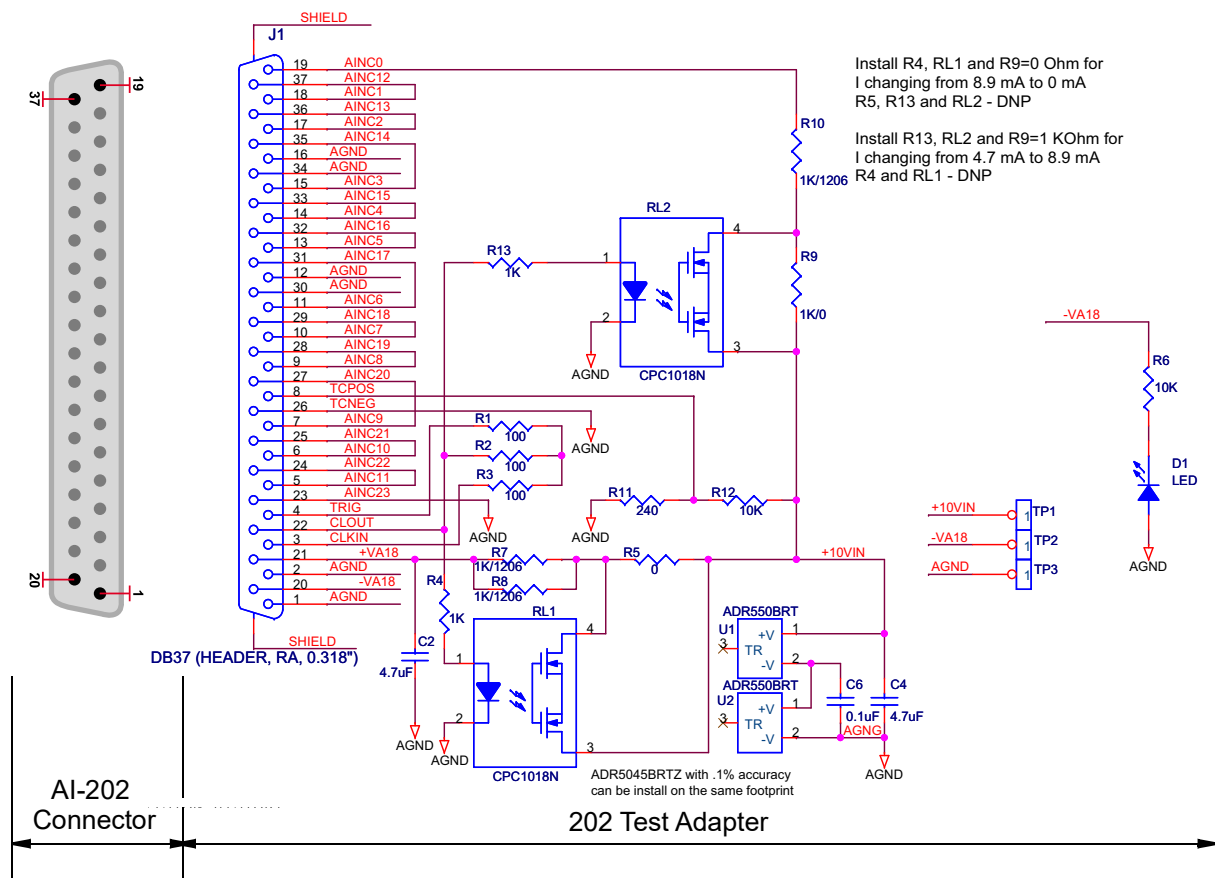


Figure 5-3 Schematic and Pinout of 202 Test Adapter

5.3 Using the 202 Test Adapter

Testing the DNx-AI-202 Analog Current Input Board with the DNx-TADP-202 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-AI-202 User Manual for information about programming the AI-202.



5.4 Specifications Technical specifications for the 202 Test Adapter are listed in **Table 5-1** below.

Table 5-1 Technical Specifications for the 202 Test Adapter

Channel Configurations	
Number of channels	12 differential current inputs to AI-202
Input Ranges to AI-202	$\pm 1.5\text{mA}$, $\pm 15\text{mA}$, $\pm 150\text{mA}$
Shunt Resistance (across AI-202 Inputs)	10-ohm, 0.1%
Isolation	1500 Vrms
Power Input to Test Adapter	+18VDC from AI-202
General Specifications	
Connector	DB-37 male
Overvoltage protection	-40V
ESD Protection	2000V
Power Consumption	Less than 1 W
Operating Temperature	-40°C to +85°C
Operating Humidity	95%, non-condensing



As shown in the diagram, the incoming power voltage is regulated down to +5V for input to two analog voltage inputs (CH1 and CH3) on the AI-205 and to +10V for the two others (CH0 and CH2).

The +5V and AGND are also used for the DIO channels on the AI-205. Since the DIO channels are bidirectional and cross-connected (Ch 0 and Ch1, Ch 2 and Ch3), the test program can be designed to simulate digital inputs and outputs on all four channels in either direction.

The pinouts of the AI-205 and the 205 Test Adapter are shown in **Figure 6-2**, along with a schematic of the Test Adapter circuit.

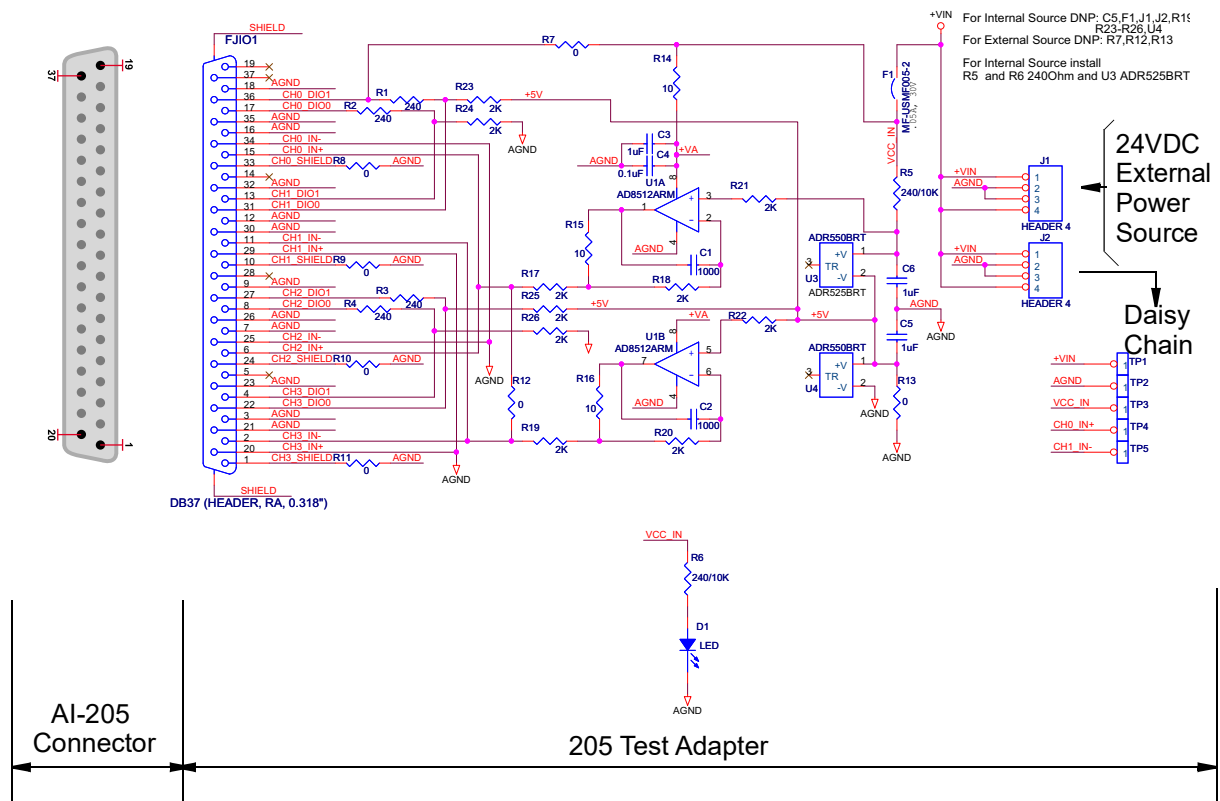


Figure 6-2 Schematic and Pinout of 205 Test Adapter

6.3 Using the 205 Test Adapter

Testing the DNx-AI-205 Analog Input Board with the DNx-TADP-205 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-AI-205 User Manual for information about programming the AI-205.



6.4 Specifications Technical specifications for the 205 Test Adapter are listed in **Table 6-1** below.

Table 6-1 Technical Specifications for the 205 Test Adapter

Channel Configurations	
Number of channels	4 differential voltage inputs to AI-205
Input Impedance	2 Mohm (to ground), 4 Mohm (differential)
Input Ranges to AI-205	$\pm 100V$, $\pm 10V$, $\pm 1V$, $\pm 0.1V$
Power Input to Test Adapter	+24VDC from external source
General Specifications	
Connector	DB-37 male
Overvoltage protection	$\pm 150V$ (powered or unpowered)
ESD Protection	2000V
Power Consumption	Less than 1 W.
Operating Temperature	-40°C to +85°C
Operating Humidity	0 to 95%, non-condensing



207/217 Test Adapter

The 207/217 Test Adapter (p/n DNx-TADP-207-17) is an accessory designed for testing UEI's DNx-AI-207 and DNx-AI-217 Analog Input Boards.

7.1 General Description

Under software control, the 207/217 Test Adapter facilitates tests on all 17 channels (16 analog voltage differential inputs plus one single ended CJC voltage) of a DNx-AI-207 or DNx-AI-217 Analog Input Board.

The 207/217 Test Adapter receives a +13V reference voltage from the AI-207/217 and converts it to +7.5V, +5V, and -2.5V voltages, which are looped back as analog inputs to the I/O board. The voltages are connected as follows:

- 7.5VDC to inputs AIN0+, AIN2+, AIN4+, AIN6+, AIN8+, AIN10+, AIN12+, and AIN14+
- 5VDC to AIN1-, AIN3-, AIN5-, AIN7-, AIN9-, AIN11-, AIN13-, AIN15-
- -2.5VDC to AIN1+, AIN3+, AIN5+, AIN7+, AIN9+, AIN11+, AIN13+, AIN15+
- 0VDC (GND) to AIN0-, AIN2-, AIN4-, AIN6-, AIN8-, AIN10-, AIN12-, and AIN14-
- The XTRIG signal from the AI-207/217 switch U1, if installed, turns the +13V power on and off.

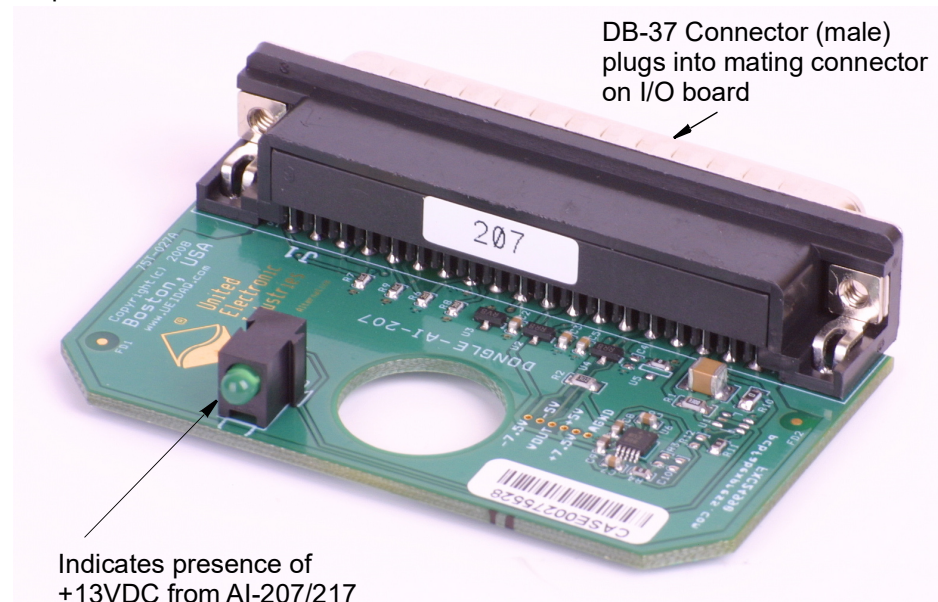


Figure 7-1 Photo of 207/217 Test Adapter



7.2 Device Architecture

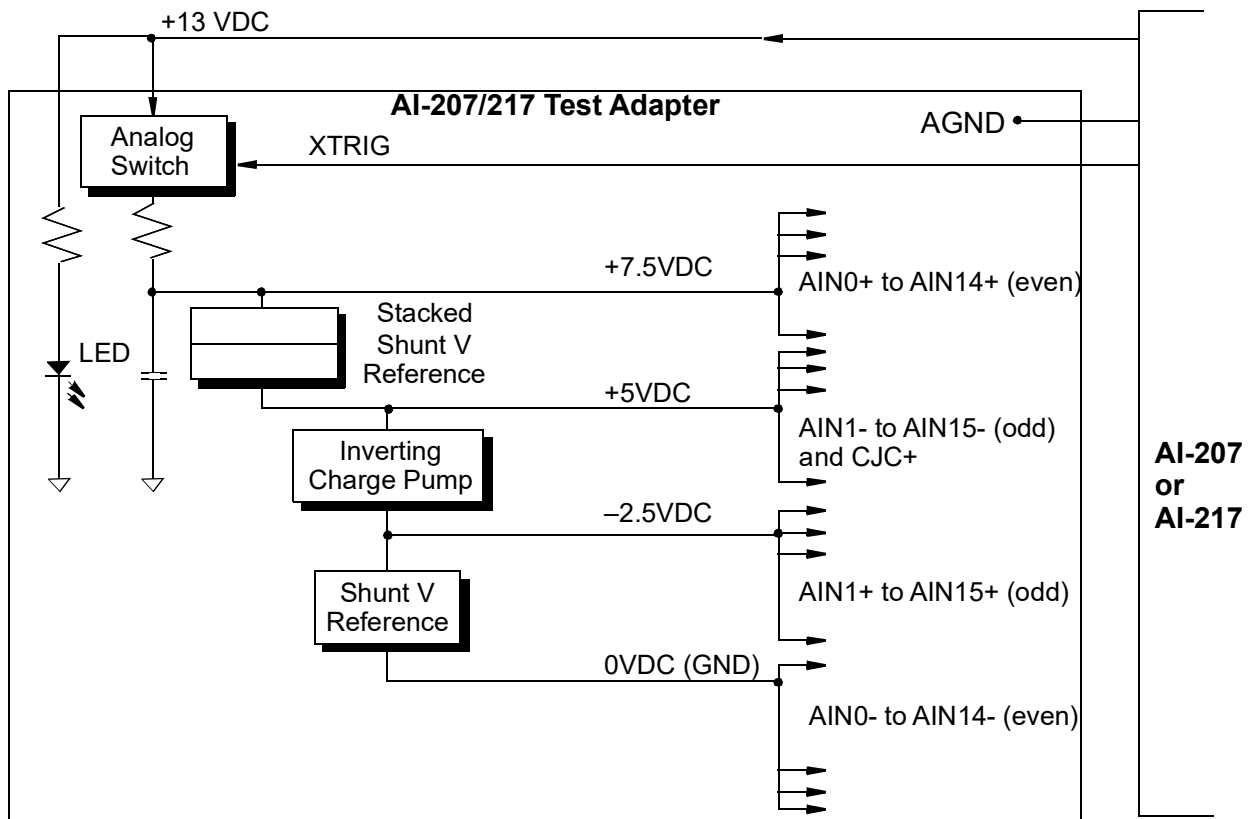


Figure 7-2 Block Diagram of 207/217 Test Adapter

As shown in **Figure 7-2** above, the AI-207/217 outputs a 13VDC voltage to the Test Adapter. This voltage is fed through an analog switch controlled via a trigger from the AI-207/217. The current through the switch passes through a resistor and two shunt voltage references to ground, which drops the voltage to 7.5V and +5 VDC. The +5 V is then passed to an inverting charge pump that outputs -10 VDC. The -10 V is fed through a shunt voltage reference to produce a -2.5 V signal. These three reference voltages and GND are connected as inputs to the terminals of the AI-207/217 Analog Input Board.

Differential measurements should therefore result in +7.5V on even channels and -7.5V on odd channels. On the AI-207, the CJC buffer will produce an expected CJC reading of +2.5V. The CJC channel is not recommended for use on the AI-217.

The pinouts of the AI-207/217 and the 207/217 Test Adapter are shown in **Figure 7-3**, along with a schematic of the Test Adapter circuit.



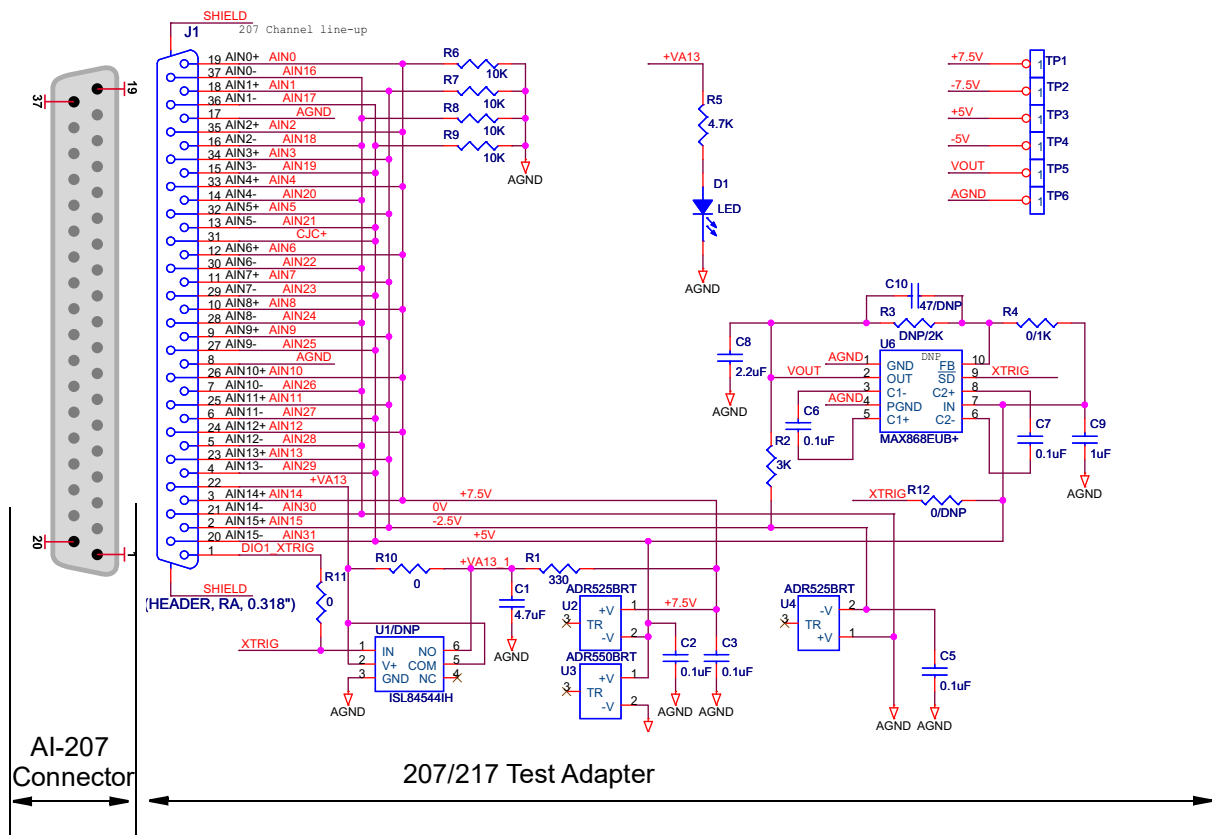


Figure 7-3 Schematic of 207/217 Test Adapter

7.3 Using the 207/217 Test Adapter

Testing the DNx-AI-207 and DNx-AI-217 Analog Input Boards with the DNx-TADP-207-17 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-AI-207/217 User Manual for information about programming the AI-207/217.



7.4 Specifications Technical specifications for the 207/217 Test Adapter are listed in **Table 7-1** below.

Table 7-1 Technical Specifications for the 207/217 Test Adapter

Channel Configurations	
Number of channels	16 differential (8 at +7.5V, 8 at -7.5V), 1 single-ended CJC channel
Programmable DIO line	One (external trigger) for switching +13V on and off. Controlled from AI-207/217.
Input Specifications	
Inputs to AI-207/217	DC Analog Voltage (+7.5V, -2.5V, +5V, 0V)
Power Input to Test Adapter	+13VDC from AI-207/217
General Specifications	
Connector	DB-37 male
Overvoltage protection	-40V to +55V
ESD Protection	15 kV
Power Consumption	Less than 1 W
Operating Temperature	-40°C to +85°C



207-to-332 Test Adapter

The 207-to-332 Test Adapter (p/n B-D-DNA-207-332 and B-D-DNR-207-332) is an accessory designed for combination testing of UEI's DNx-AI-207/217 Analog Input Board and DNx-AO-332 Analog Output Board. The test adapter requires that the I/O boards be mounted in adjacent slots of a PowerDNA Cube or in adjacent positions of a DNR rack for testing to be performed.

8.1 Features

The key features of the 207-to-332 Test Adapter are:

- Facilitates basic testing of DNx-AI-207/217 Analog Input Board and DNx-AO-332 Analog Output Board mounted in adjacent slots of a Cube or Rack
- On-board jumper selector permits testing AI-207 or AI-217 in combination with either AO-332 or AO-332-828
- AO-332 simulates analog voltage inputs to all channels of an AI-207/217 I/O Board
- LED indicates presence of +12 VDC voltage source from AI-207/217

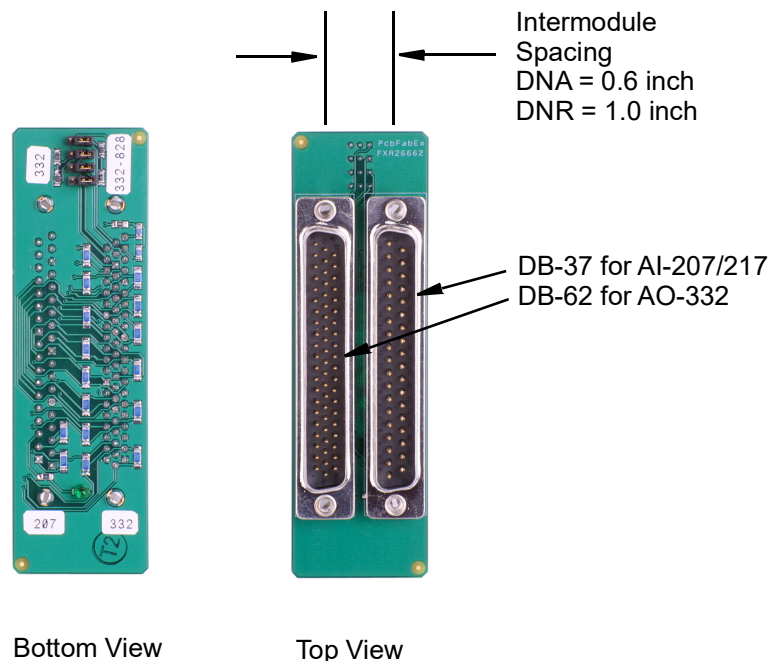


Figure 8-1 Photo of 207-to-332 Test Adapter

8.2 General Description

Under software control, the 207-to-332 Test Adapter facilitates tests on all 16 differential input channels of a DNx-AI-207 or DNx-AI-217 Analog Input Board or all 32 channels of the AO-332 Analog Output Board. Since the AI-207/217 accepts only 16 differential analog voltages, the Test Adapter combines pairs of single-ended analog outputs of the AO-332 into 16 differential voltage inputs to the AI-207/217.



The 207-to-332 Test Adapter is offered in two different versions, depending upon which I/O boards are to be tested. The Test Adapter is offered in either a DNA (Cube) or DNR (Rack) model. Although functionally identical, they differ in the spacing between connectors — the DNA model connectors match the slot spacing of a PowerDNA Cube; the DNR model connectors match the spacing of modules in a RACKtangle or HalfRACK housing. Both versions have an on-board jumper selector that permits testing of either a standard AO-332 or an AO-332-828.

The AI-207/217 also has a bidirectional DIO line connected through resistors with DIN and DOUT lines on the AO-332.

When the Test Adapter jumpers are set to test a standard AO-332, the jumpers are placed into the 1-2 position. This connects AOUT28 and AOUT29 directly to inputs AIN14+ and AIN14- on the AI-207/217, (Analog Input Channel 14). In this mode, AOUT30 and AOUT31 output a constant +12V and -12V, respectively. These voltages are connected directly to inputs AIN15+ and AIN15- (AI-207/217 input Channel 15).

When the Test Adapter jumpers are set to the AO-332-828 position (position 2-3), AOUT 27 and AOUT28 are connected to AGND-CH. In this mode, AOUT30 and AOUT31, which carry +12V and 12V from the 332, are connected through a voltage divider circuit (which drops the voltage to about 8V) to AIN15+ and AIN15- (Channel 15) on the AI-207/217.

An LED indicates the presence of the +12 VDC output from the AI-207/217.

AO-333 Compatibility



While you can use the 207-to-332 Test Adapter with the AO-333, it is more convenient to test the AO-333 directly using its Guardian Readback feature.



8.3 Device Architecture

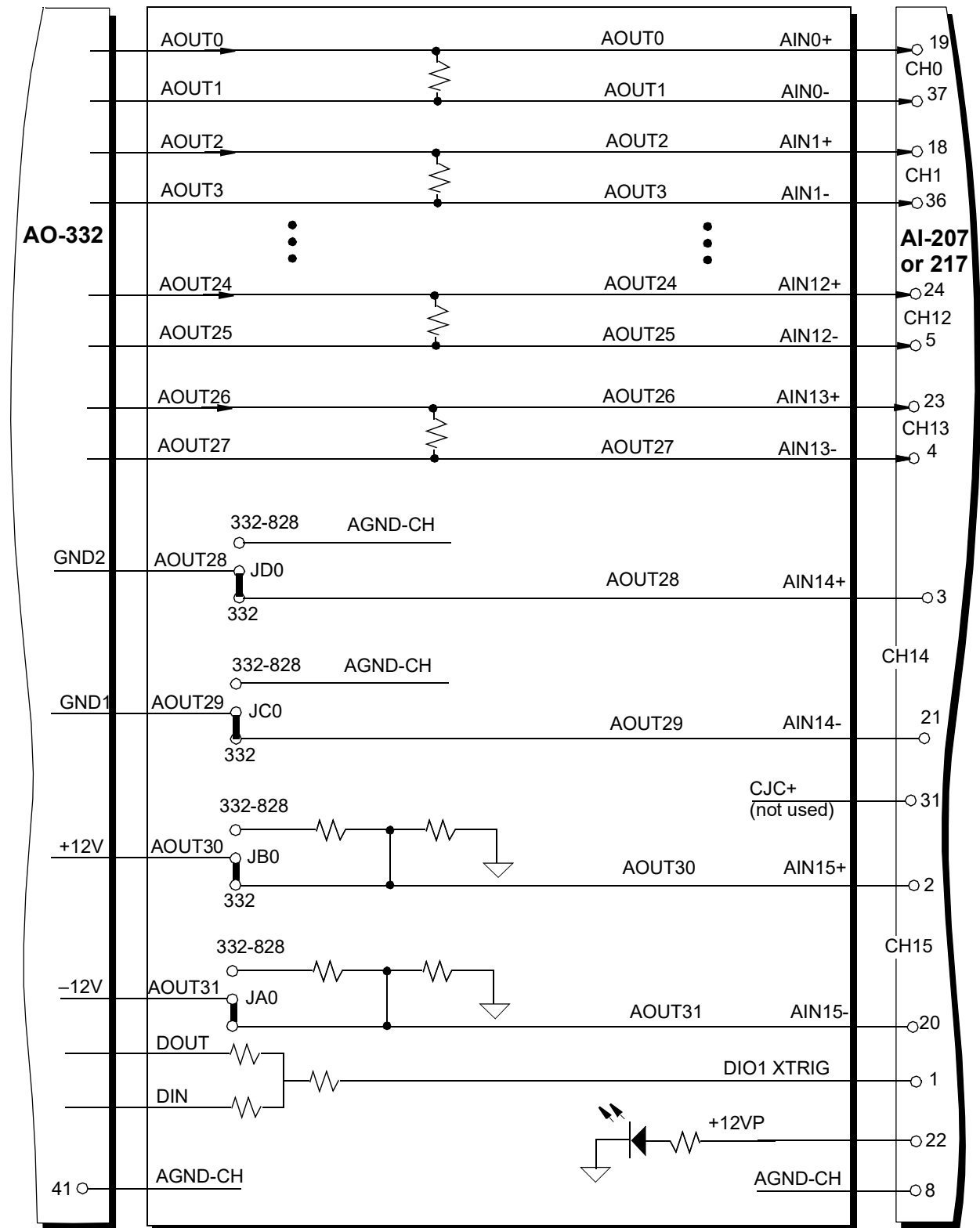


Figure 8-2 Block Diagram of 207-to-332 Test Adapter



8.5 Specifications Technical specifications for the 207-to-332 Test Adapter are listed in **Table 8-1** below.

Table 8-1 Technical Specifications

Channel Configurations	
No. of channels	32 analog inputs, 16 analog outputs, 1 DIO
Channel configurations	AO-332 even channel <-> AI-207 +channel AO-332 odd channel <-> AI-207 -channel (e.g., AOut0 <-> AIN0+ and AOut1 <-> AIN0-) AO-332 DIO <-> AI-207/217 XTrig
General Specifications	
Connector	One DB-37 male to AI-207/217 One DB-62 male to AO-332
Overvoltage protection	-40V to +55V
ESD Protection	2000 V ESD
Power Consumption	3W (AO-332)
Operating Temperature	-40°C to +85°C
Operating Humidity	0 to 95%, non-condensing



208 Test Adapter

The 208 Test Adapter (p/n DNx-TADP-208) is an accessory designed for testing UEI's DNx-AI-208 Strain/Bridge Analog Input Board.

9.1 General Description

Under software control, the 208 Test Adapter facilitates tests on all 8 channels of a DNx-AI-208 Analog Input Board. The AI-208 is designed to accept analog voltage inputs from full, half, and quarter-bridge strain gauges. The 208 Test Adapter connects a full Wheatstone bridge to each of the eight input channels of the AI-208.

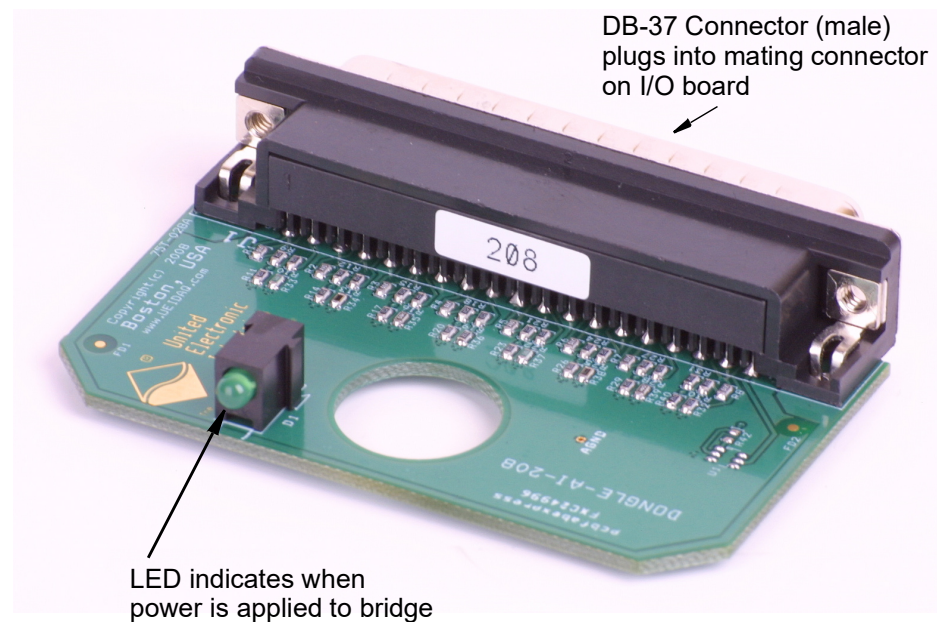


Figure 9-1 Photo of 208 Test Adapter

9.2 Device Architecture

As shown in **Figure 9-2**, the 208 Test Adapter connects a fixed-resistor bridge circuit to each AI-208 channel. Channel 0 and 4 have a 2% unbalance, Ch1 and Ch5 have 5%, Ch2 and Ch6 have 7%, Ch3 and Ch7 have 10%.

The LED is ON when P1+ is present to indicate that power is applied to the bridge.

The XTRIG signal is not currently used.

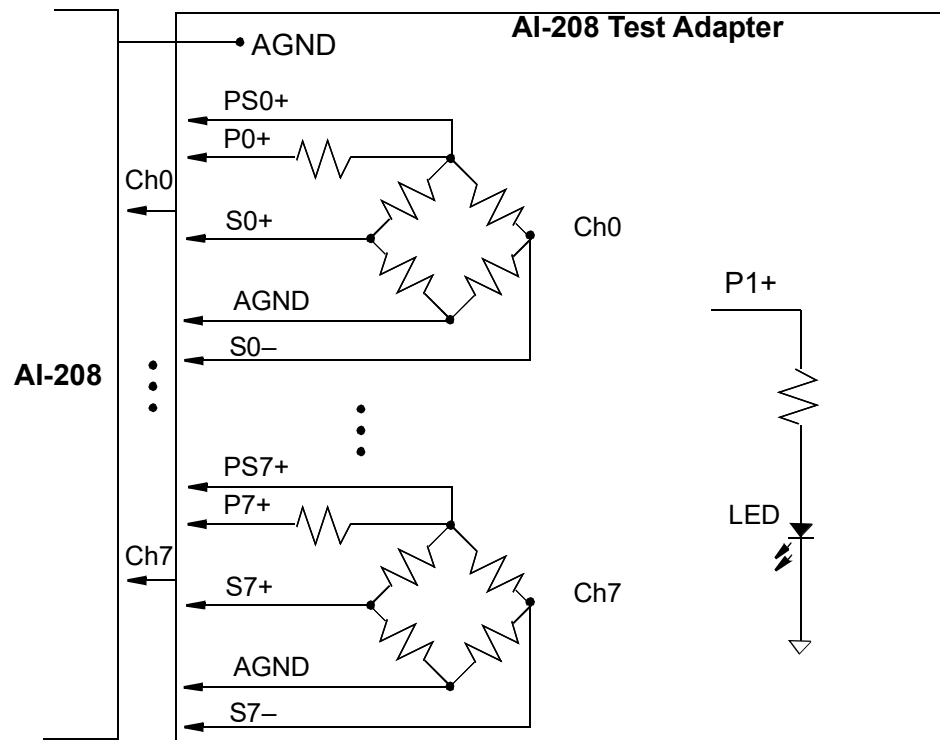


Figure 9-2 Block Diagram of 208 Test Adapter

The pinouts of the AI-208 and the 208 Test Adapter are shown in **Figure 9-3**, along with a schematic of the Test Adapter circuit.

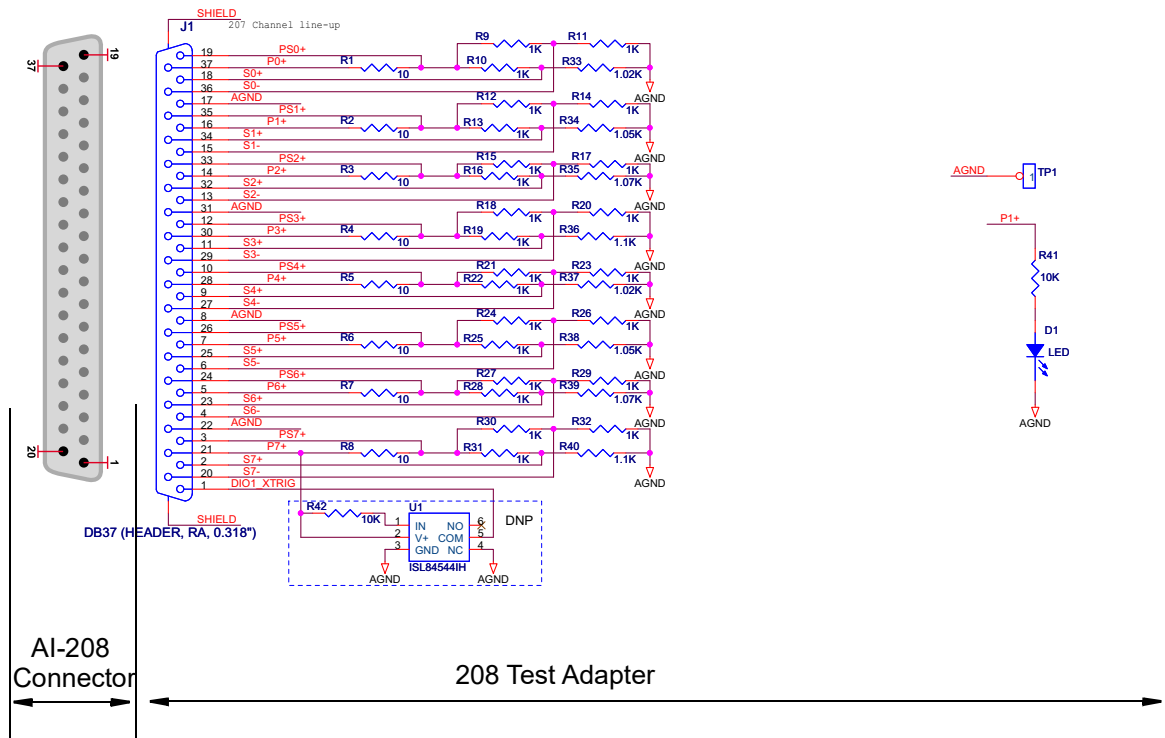


Figure 9-3 Schematic and Pinout of 208 Test Adapter

9.3 Using the 208 Test Adapter

Testing the DNx-AI-208 Strain/Bridge Analog Input Board with the DNx-TADP-208 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-AI-208 User Manual for information about programming the AI-208.



9.4 Specifications

Technical specifications for the 208 Test Adapter are listed in **Table 9-1** below.

Table 9-1 Technical Specifications for the 208 Test Adapter

Channel Configurations	
Number of channels	8 full-bridge strain gauge inputs
Indicating LED	One LED indicates Power On when voltage is applied to Ch 1 bridge.
Input Specifications	
Inputs to AI-208	Fixed-resistor Wheatstone bridge with one resistor specified to give a specific unbalance.
General Specifications	
Connector	DB-37 male
Overvoltage protection	-40V to +55V
ESD Protection	15 kV
Power Consumption	Less than 1 W
Operating Temperature	-40°C to +85°C



211 Test Adapter

The 211 Test Adapter (p/n DNx-TADP-211) is an accessory designed for testing UEI's DNx-AI-211 Vibration Interface Board.

10.1 Features

The key features of the 211 Test Adapter are:

- Facilitates basic DC testing of DNx-AI-211 Boards
- Performs loopback tests to verify operation of DC bias current output through 3.6K resistor using analog input voltage
- Allows testing of open circuit and short circuit trip points
- 4 Independent channels with 2-color (Red/Green) indicating LEDs on each for visual verification of bias current operating point
- Allows testing of AC and DC coupling

10.2 General Description

Under software control, the 211 Test Adapter facilitates loopback tests on all four channels of a DNx-AI-211 IEPE/ICP Vibration Sensor Interface Board. The AI-211, which is designed to interface directly with industry standard IEPE/ICP vibration sensors, outputs a DAC-controlled 0-8 mA DC current on each of four channels. This current is typically used to bias an IEPE/ICP vibration sensor, one per channel. The output of a sensor is an AC signal superimposed on a DC voltage. Vibration measurements look only at the AC component and usually use AC coupling to remove the DC component. The AC component is then filtered, amplified, and fed to a 24-bit ADC.

For this test, however, no AC component is present. The 211 Test Adapter, therefore, tests operation and accuracy of the bias current circuit (DAC, V/I converter/monitor, Secondary ADC, PGA, and 24-bit ADC) on each of the four channels. It does not, however, test AC performance of AI-211 or the vibration sensor itself.

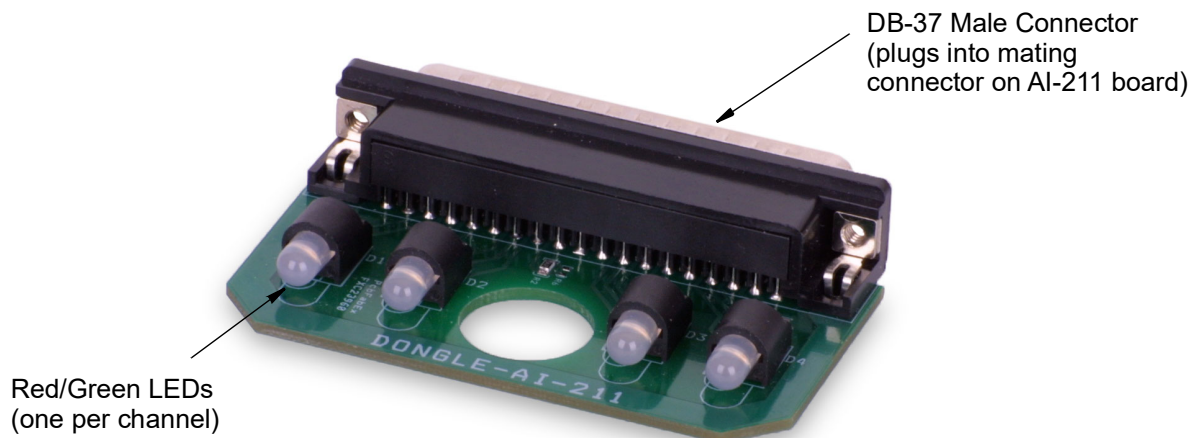


Figure 10-1 Photo of 211 Test Adapter



10.3 Device Architecture

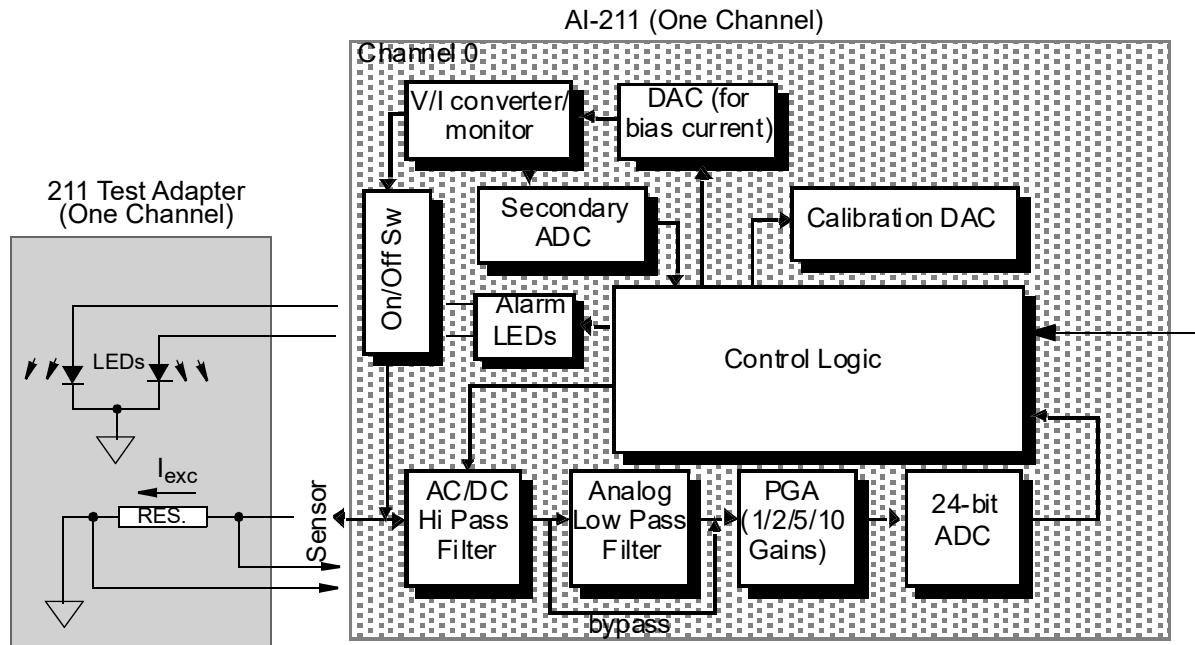


Figure 10-2 Block Diagram of 211 Test Adapter

As shown in **Figure 10-2** above, the AI-211 outputs a bias current to a 3.6K resistor on the 211 Test Adapter. The magnitude of the current is set by a DAC, which outputs a voltage to a V-to-I converter. The V-to-I module also monitors the current and feeds back a measurement signal to a secondary 12-bit ADC.

The voltage across the 3.6K resistor is fed back to the AI-211 as an analog input. The signal is then processed by the AI-211 as a normal voltage measurement input.

The test program thus exercises and verifies DC performance of the PGA and 24-bit ADC at various levels of bias current. Test results can be displayed, stored, or exported as needed by your application.

The pinouts of the AI-211 and the 211 Test Adapter are shown in **Figure 10-3**, along with a schematic of the Test Adapter circuit.

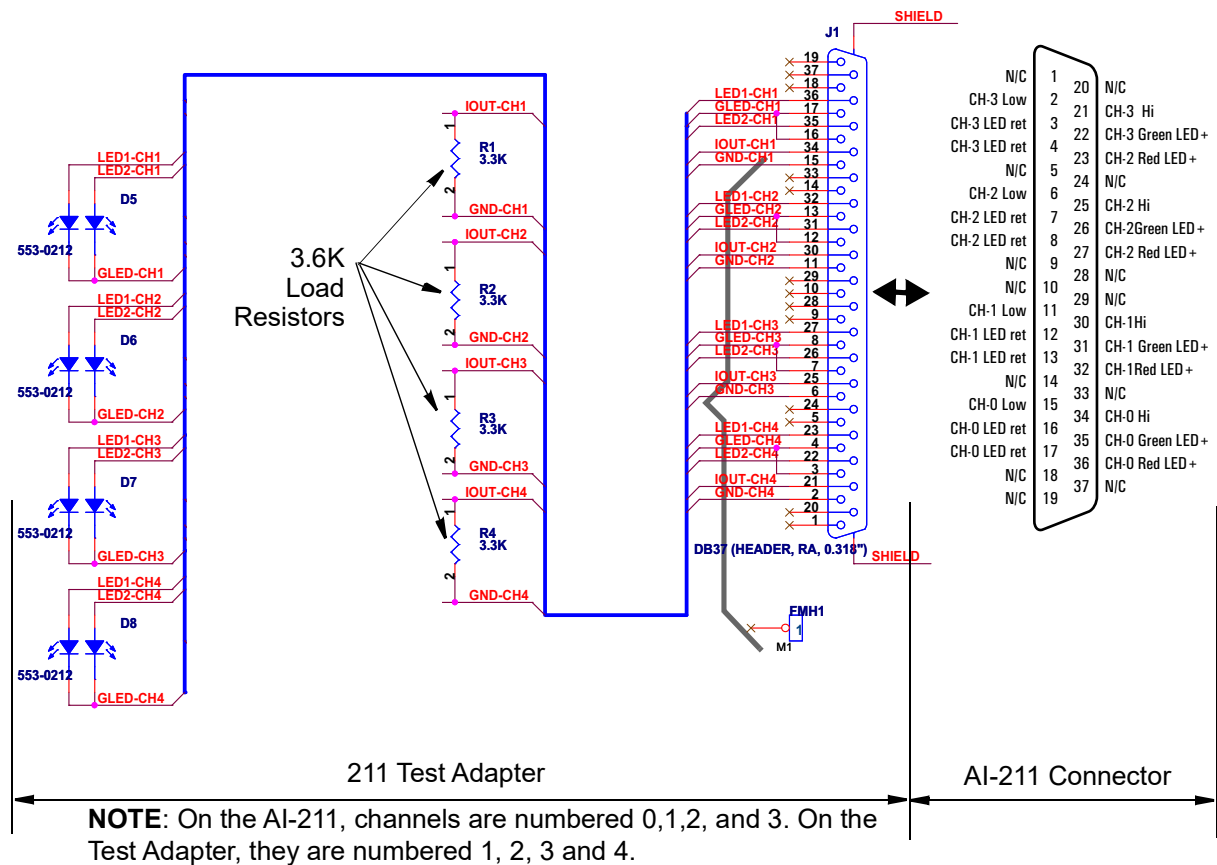


Figure 10-3 Schematic and Pinout of 211 Test Adapter

10.4 Using the 211 Test Adapter

Testing the DNx-AI-211 Vibration Interface Board with the DNx-TADP-211 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-AI-211 User Manual for information about programming the AI-211.



10.5 Specifications Technical specifications for the 211 Test Adapter are listed in **Table 10-1** below.

Table 10-1 Technical Specifications for the 211 Test Adapter

Channel Configurations	
Number of channels	4
Input Specifications	
Input Types	One bias current analog input per channel and two on/off voltage inputs per channel for red/green alarm LEDs (2 per channel)
Load Resistor	3.6 k ohm per channel
Current Range	0.0 to 8 mA
Resolution	12-bits
Accuracy	±1%
Short Circuit Protection	Continuous short will not cause damage.
Maximum Output Voltage	25 VDC minimum
Open/short detection	Automatic alarms for both high and low current at user-selectable trigger points (provided by AI-211 board)
Open/Short Annunciators	Two LEDs per channel
General Specifications	
Connector	DB-37 male
ESD Protection	15 kV
Power Consumption	Less than 1 W
Operating Temperature	-40°C to +85°C



225 Test Adapter

The 225 Test Adapter (p/n DNx-TADP-225) is an accessory designed for testing UEI's DNx-AI-225 Analog Input Board.

11.1 General Description

Under software control, the 225 Test Adapter facilitates analog input testing on all 25 channels of a DNx-AI-225 Analog Input Board. The AI-225, which is designed to accept analog voltage inputs in the range of ± 1.25 VDC, also outputs a 9 VDC voltage for use with the STP-AI-U accessory board and CJC.

The 225 Test Adapter performs simulated analog input tests on all channels using the AI-225 internal voltage source. The test program exercises and verifies DC performance of the PGA and 24-bit ADCs on each channel. Test results can be displayed, stored, or exported as needed by your application.

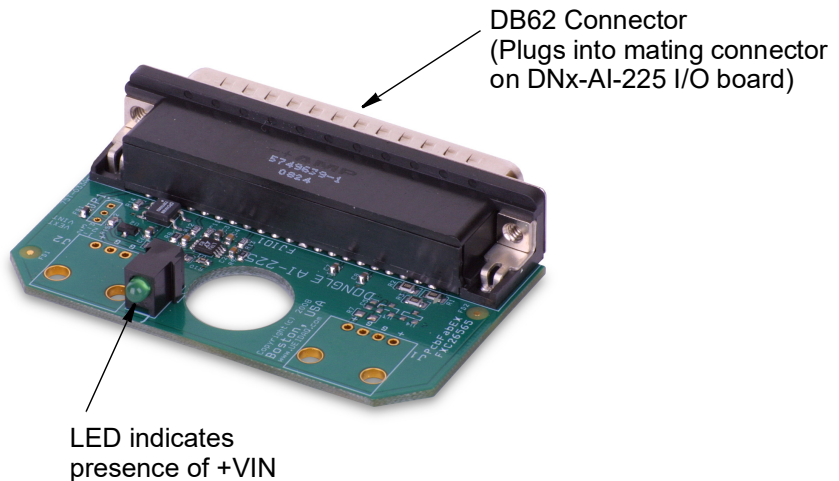


Figure 11-1 Photo of 225 Test Adapter



11.2 Device Architecture

In the 225 Test Adapter, the +9 VDC is dropped to +2.5 VDC (U1A input) by a shunt voltage reference. The +2.5 VDC is then divided to +1.5 VDC at the U1B input. The output of U1A connects with VIN+ and the output of U1B connects with VIN-. RL1, if installed and under DIO control, can connect both outputs of U1 to analog ground. An LED indicates when VIN+ is present.

Even-numbered INPx and odd-numbered INNx inputs are connected to VIN-, while even-numbered INNx and odd-numbered INPx are connected to VIN+. This channel configuration allows short circuit detection between adjacent channels. Even channels should read -1.0 VDC and odd channels should read +1.0 VDC.

The pinouts of the AI-225 and the 225 Test Adapter are shown in **Figure 11-2**, along with a schematic of the Test Adapter circuit.

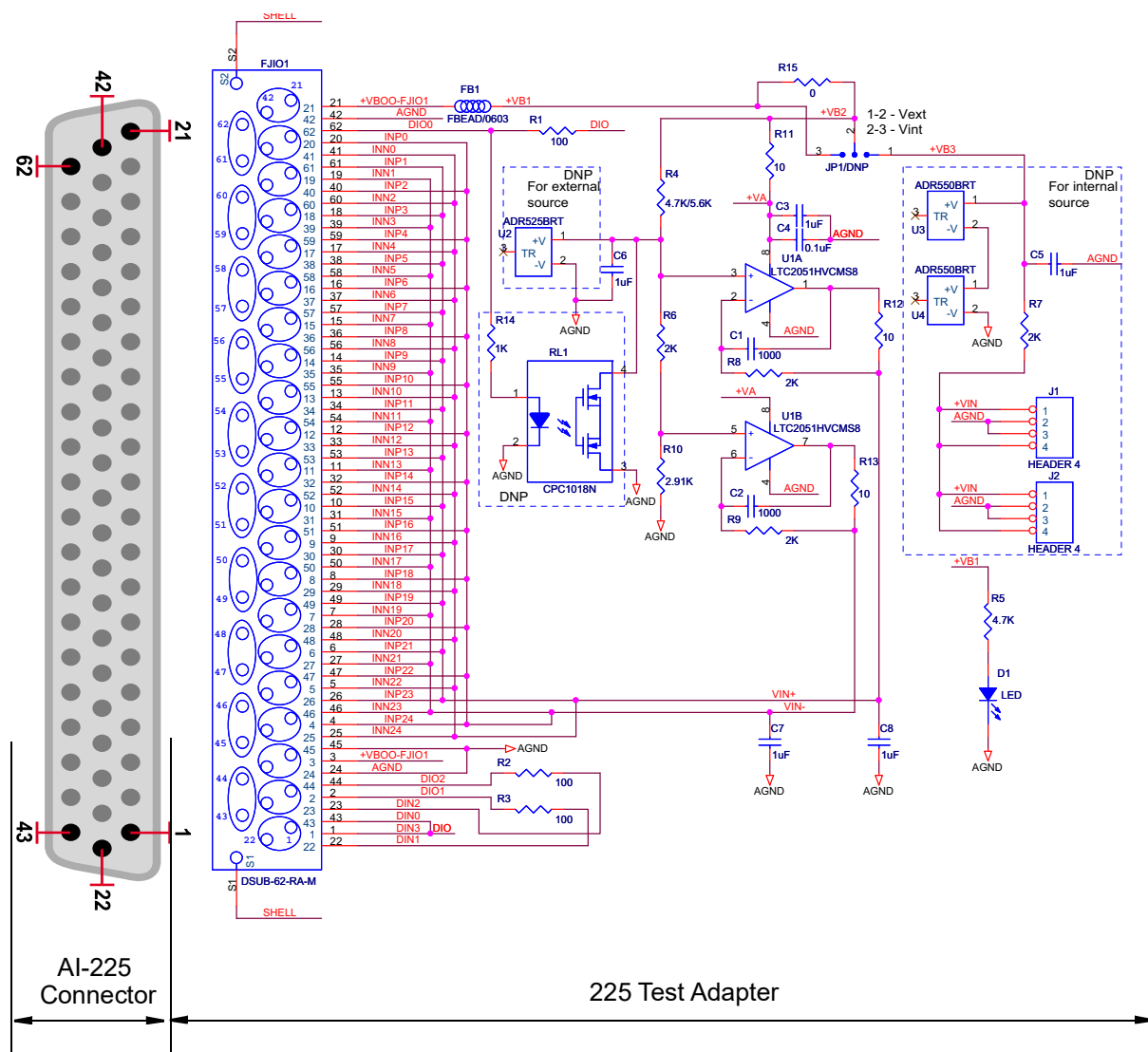


Figure 11-2 Schematic and Pinout of 225 Test Adapter



11.3 Using the 225 Test Adapter

Testing the DNx-AI-225 Analog Input Board with the DNx-TADP-225 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-AI-225 User Manual for information about programming the AI-225.



11.4 Specifications Technical specifications for the 225 Test Adapter are listed in **Table 11-1** below.

Table 11-1 Technical Specifications for the 225 Test Adapter

Channel Configurations	
Number of channels	25 analog voltage, 3 DIO
Power Supply	AI-225 internal source (+9 VDC)
Inputs to AI-225	Even channels: -1.0 VDC Odd channels: +1.0 VDC
Input Protection	2 kV ESD, ± 15 V over/under voltage
General Specifications	
Connector	DB-62 male
ESD Protection	15 kV
Power Consumption	Less than 1 W
Operating Temperature	-40°C to +85°C



254 Test Adapter

The 254 Test Adapter (p/n DNx-TADP-254) is an accessory designed for testing UEI's DNx-AI-254 LVDT/RVDT Interface Board.

12.1 Features

The key features of the 254 Test Adapter are:

- Facilitates loopback testing of DNx-AI-254 Boards in all operating modes
- Compatible with all standard LVDT/RVDT wiring configurations
- Tests easily defined and modified via software
- Red/Green LEDs on each channel are provided for future testing of digital I/O (not currently supported)

12.2 General Description

Under software control, the 254 Test Adapter facilitates loopback tests on all four channels of a DNx-AI-254 LVDT/RVDT Interface Board. The AI-254 itself is designed to interface directly with industry standard LVDT/RVDT sensors in any of the standard operating modes (4-, 5-, and 6-wire connections).

Since each of the four channels may be configured either as an LVDT/RVDT input interface with either internal or external excitation or as an LVDT/RVDT simulator output with external excitation, the 254 Test Adapter cross-connects Channels 0 and 1 and Channels 2 and 3 so that in testing mode an excitation output from one channel can be used as the external excitation input for the other channel in the pair.

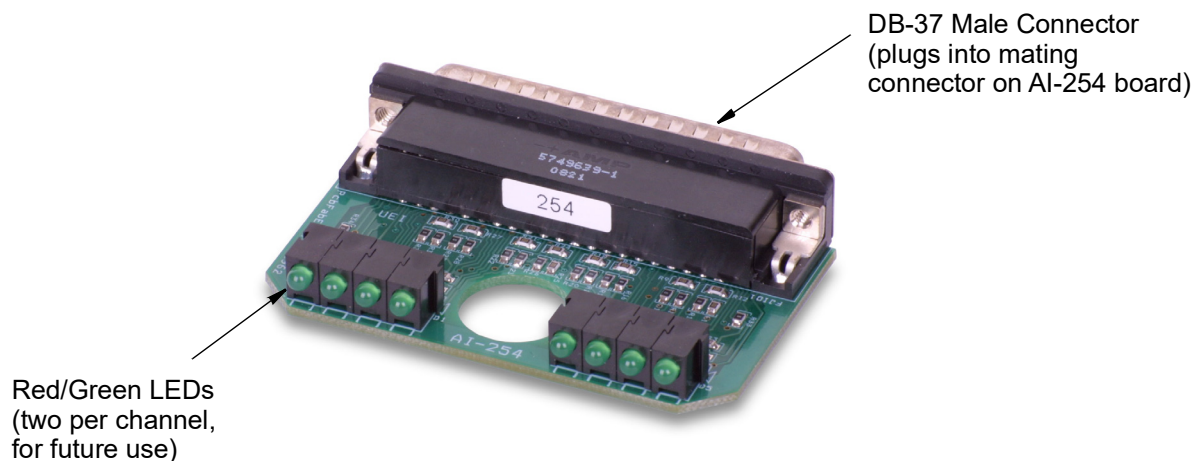


Figure 12-1 Photo of 254 Test Adapter



12.3 Device Architecture

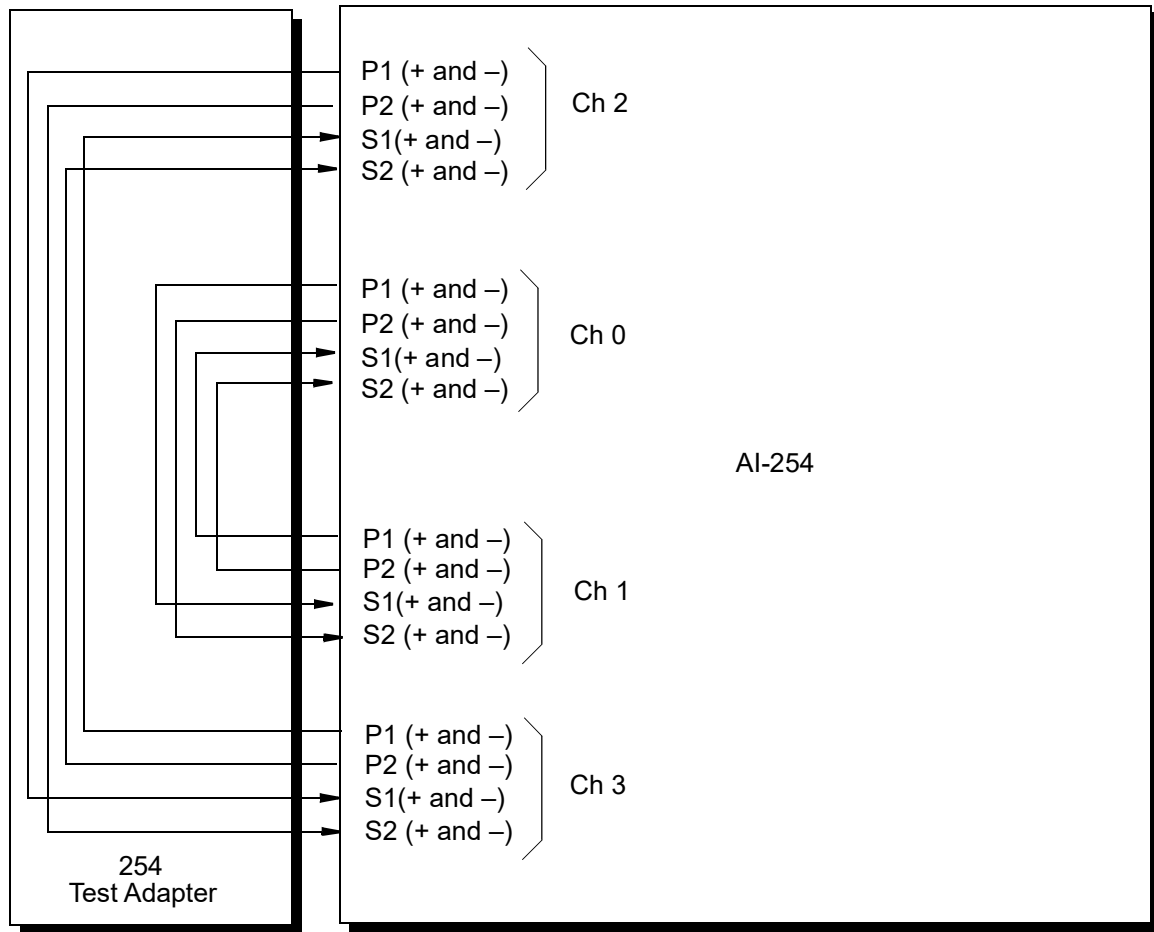


Figure 12-2 Channel Configuration of 254 Test Adapter

As shown in **Figure 12-2**, the P1 output from Channel 0 is wired to S1 on Channel 1, and vice versa. The P2 on Channel 0 is wired to S2 on Channel 1, and vice versa. Similar connections are used between Channels 2 and 3. Two digital outputs per channel and associated LEDs are provided for future use in testing digital I/O and are not currently supported.

For a description of the various wiring configurations of LVDTs and RVDTs, refer to Section 1.8 “Operating Modes” in the DNx-AI-254 User Manual. The diagrams in the DNx-AI-254 User Manual show how inputs and outputs (including simulated signals) are connected for each of the 4-5- and 6-wire configurations and operating modes used with the AI-254 layer.

The pinouts of the AI-254 and the 254 Test Adapter are shown in **Figure 12-3**, along with a schematic of the Test Adapter circuit.



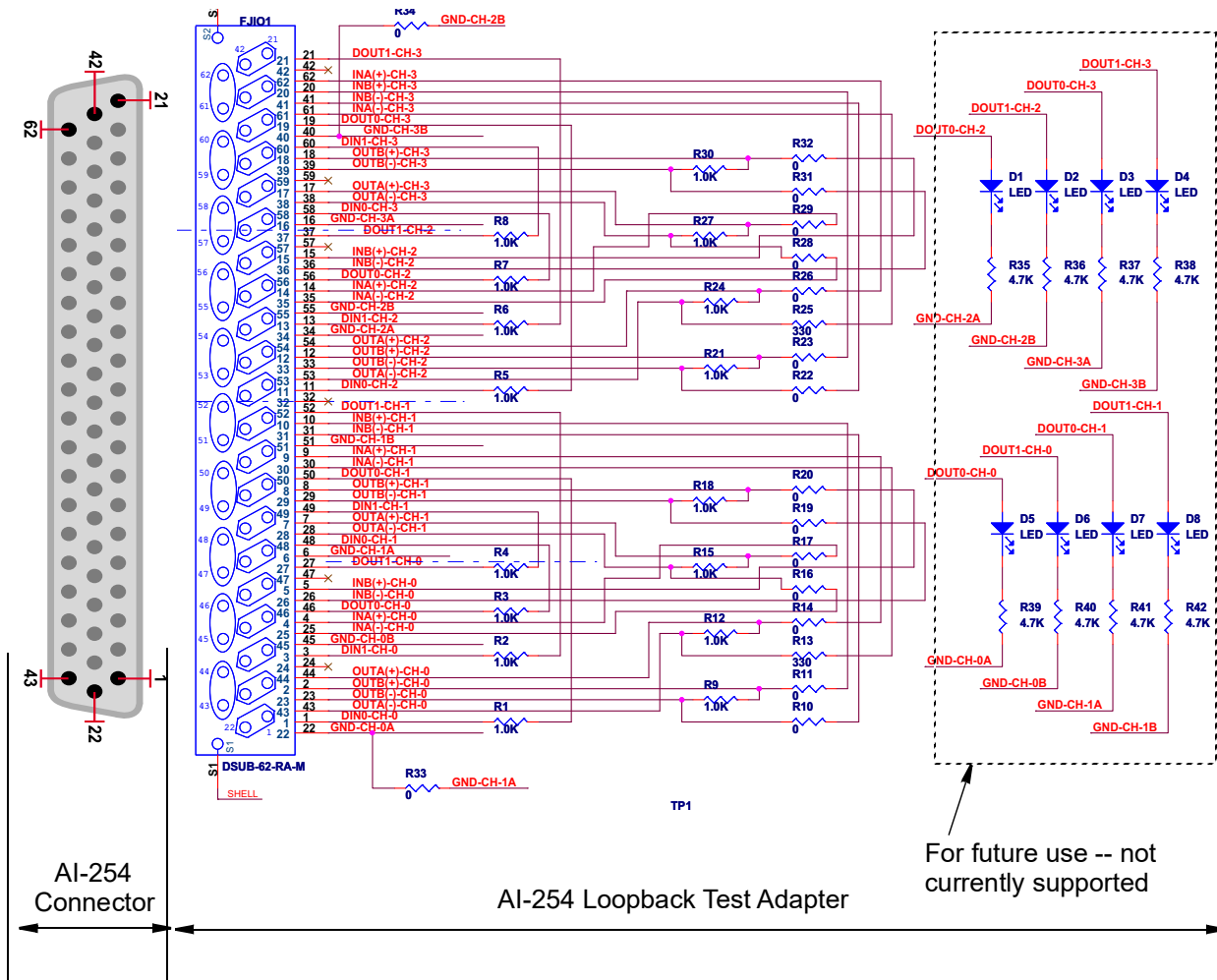


Figure 12-3 Schematic and Pinout of 254 Test Adapter

12.4 Using the 254 Test Adapter

Testing the DNx-AI-254 LVDT/RVDT Interface Board with the DNx-TADP-254 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-AI-254 User Manual for information about programming the AI-254.



12.5 Specifications Technical specifications for the 254 Test Adapter are listed in **Table 12-1** below.

Table 12-1 Technical Specifications (when used with the AI-254)

Inputs	
Number of channels	4
Configuration	Supports all common input/excitation configurations (e.g., 4-, 5-, and 6-wire)
Resolution	16-bit
Accuracy	0.1%
Input Impedance	100 kOhm
Excitation Frequency	100 Hz to 5.0 kHz, programmable with 1Hz resolution, $\pm 0.1\%$ overall accuracy
Excitation Drive	50 mA at 10 Vrms, 65 mA at 6 Vrms
Primary Impedance	90 Ohm min at 6 Vrms (or less) 200 Ohm min at 10 Vrms.
Update rate	Up to 500 readings per second. The default rate is 1/10 the excitation frequency.
Simulation Outputs	
Number of channels	4
Number of Analog Outputs	2 per channel
Configuration	2-, 3-, or 4-wire
Resolution	16-bit
Output Accuracy	0.1%
Output Voltage	2 to 10 Vrms
Output Drive Current	50 mA max
Number of indicating LEDs	2 per channel, 8 total
General Specifications	
Operating Temperature	Tested -40°C to +85°C
Vibration	5g (operating)
Shock	50 g (operating)
Humidity	0 to 95%, non-condensing
Altitude	0 to 70,000 ft.
Connector	DB-37 male
ESD Protection	15 kV
Power Consumption	Less than 1 W



255/256 Test Adapter

The 255/256 Test Adapter (p/n DNx-TADP-255-56) is an accessory designed for testing UEI's DNx-AI-255 Synchro/Resolver Interface Board and DNx-AI-256 LVDT/RVDT/Synchro/Resolver Interface Board.

13.1 Features

The key features of the 255/256 Test Adapter are:

- Facilitates loopback testing of AI-255/256 I/O Boards in all operating modes that do not require external equipment
- Compatible with all standard LVDT/RVDT/Synchro/Resolver wiring configurations
- Tests are easily defined and modified via software
- LEDs on each channel provided for future testing of digital I/O (not currently supported)

13.2 General Description

Under software control, the 255/256 Test Adapter facilitates loopback tests on both channels of a DNx-AI-255 Synchro/Resolver Interface Board or DNx-AI-256 LVDT/RVDT/Synchro/Resolver Interface Board.

Since both of the channels may be configured either as input interface with either internal or external excitation or as a simulator output with external excitation, the 255/256 Test Adapter cross-connects Channels 0 and 1 so that in testing mode an excitation or voltage output from one channel can be used as the external excitation or voltage input for the other channel.

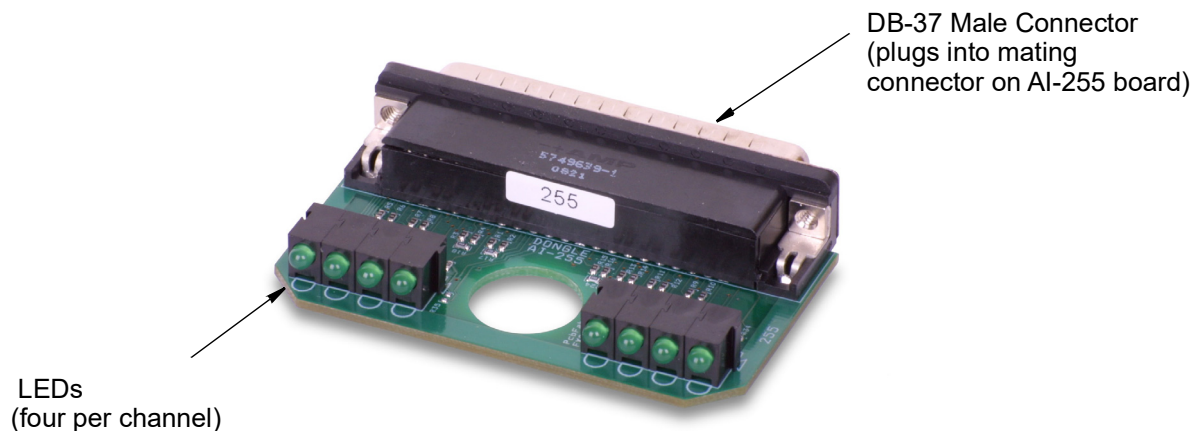


Figure 13-1 Photo of 255/256 Test Adapter



13.3 Device Architecture

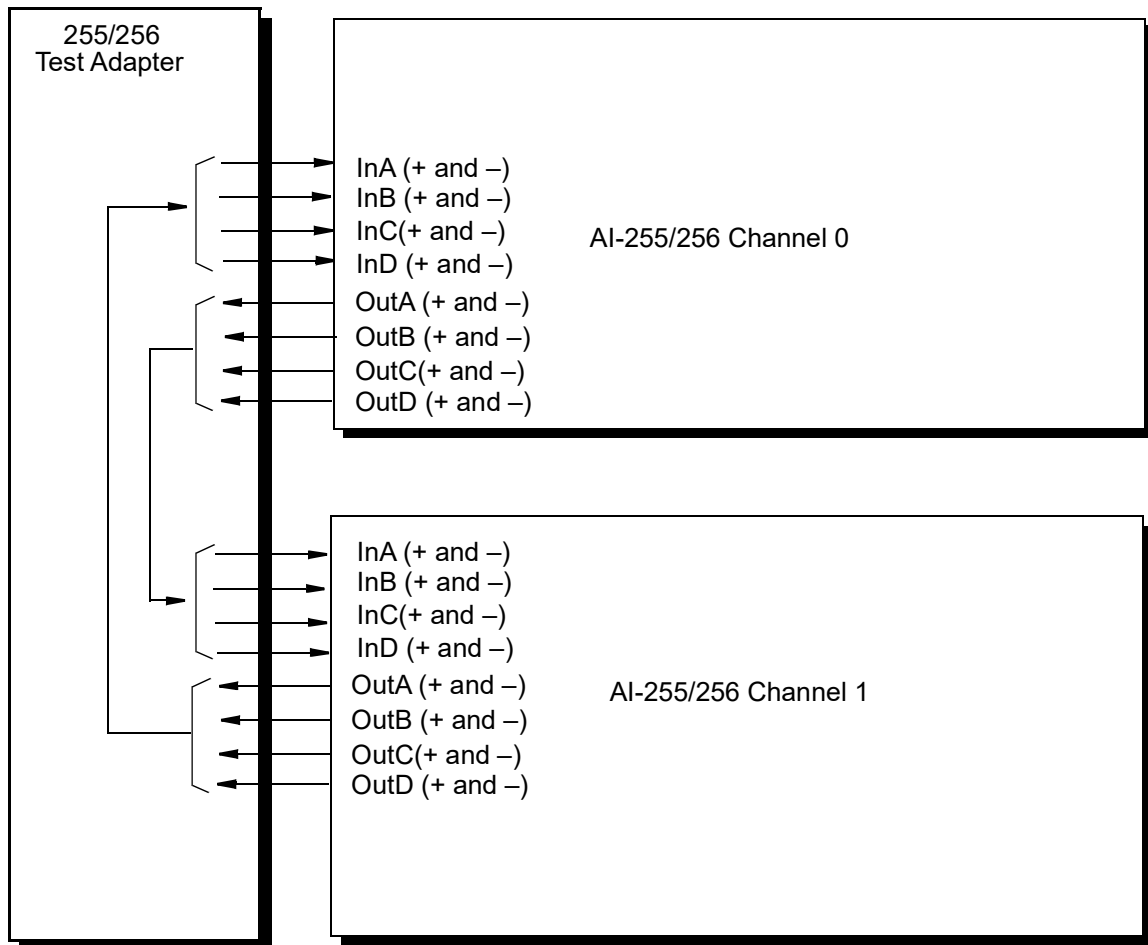


Figure 13-2 Channel Configuration of 255/256 Test Adapter

The OutA output from Channel 0 is wired to InA input on Channel 1, and vice versa. Similar connections are used between OutB, OutC, and OutD on Channel 0 and InB, InC, and InD on Channel 1, and vice versa. Four digital outputs per channel, eight total, are provided for future use in testing Digital I/O (and activating LEDs) and are not currently supported. Refer to the diagram in **Figure 13-3** for an illustration of these interconnections.

For a description of the various wiring configurations of synchros and resolvers, refer to **Appendix B** of the DNx-AI-255 User Manual or the DNx-AI-256 User Manual. These diagrams show how synchro/resolver inputs and outputs (including simulated signals) are connected for each of the various wiring configurations and operating modes used with the AI-255/256 layer.



The pinouts of the AI-255/256 and the 255/256 Test Adapter are shown in **Figure 13-3**, along with a schematic of the Test Adapter circuit.

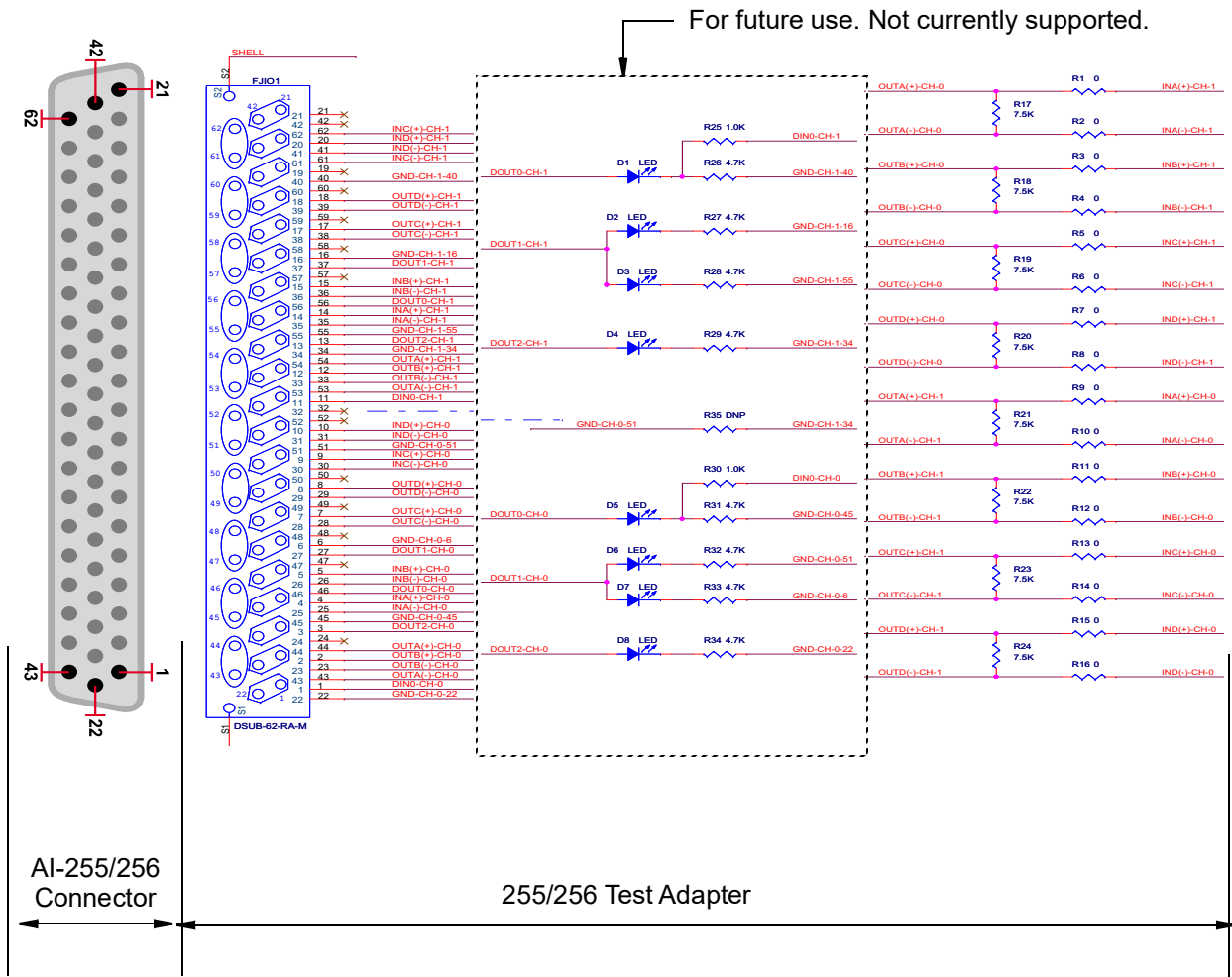


Figure 13-3 Schematic and Pinout of 255/256 Test Adapter

13.4 Using the 255/256 Test Adapter

Testing the DNx-AI-255 Synchro/Resolver Interface Board or DNx-AI-256 LVDT/RVDT/Synchro/Resolver Interface Board with the DNx-TADP-255-56 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-AI-255 User Manual or the DNx-AI-256 User Manual for information about programming the AI-255/256.



13.5 Specifications Technical specifications for the 255/256 Test Adapter are listed in **Table 13-1** below.

Table 13-1 Technical Specifications

Channel Configuration	
Number of channels	2
Channel Configuration	Ch1 simulated output -> Ch0 input Ch0 simulated output -> Ch1 input
Excitation Source	internally supplied by AI-255/256
Number of indicating LEDs	4 per channel, 8 total, programmable
General Specifications	
Connector	DB-37 male
Operating Temperature	Tested -40°C to +85°C
Vibration	5g (operating)
Shock	50 g (operating)
Humidity	0 to 95%, non-condensing
Altitude	0 to 70,000 ft.
Power Consumption	Less than 1 W



401-to-402 Test Adapter

The 401-to-402 Test Adapter (p/n B-D-DNA-207-332 and B-D-DNR-207-332) is an accessory designed for combination testing of UEI's DNx-DIO-401 Digital Input Board and DNx-DIO-402 Digital Output Board. The test adapter requires that the I/O boards be mounted in adjacent slots of a PowerDNA Cube or in adjacent positions of a DNR rack for testing to be performed.

14.1 General Description

Under software control, the 401-to-402 Test Adapter facilitates tests on all 24 channels of a DNx-DIO-401 Digital Input and DNx-DIO-402 Digital Output Board. The DIO-401 is designed to accept digital voltage inputs within a 7-36V (24V nominal) range at sampling rates up to 1kS/sec. The DIO-402 is designed to output digital voltage levels within a 7-36V (24V nominal) range at sampling rates up to 1kS/sec.

The Test Adapter is designed to plug into mating DB37 connectors on adjacent 401 and 402 DIO boards. One model is dedicated to DNA-version boards mounted in a Cube; another model is designed for use with DNR-version boards mounted in a 6- or 12-slot RACKtangle housing. Two versions are needed because the spacing between DIO boards mounted in a Cube (DNA version) is different from the spacing of boards mounted in a half or full sized RACKtangle (DNR version).

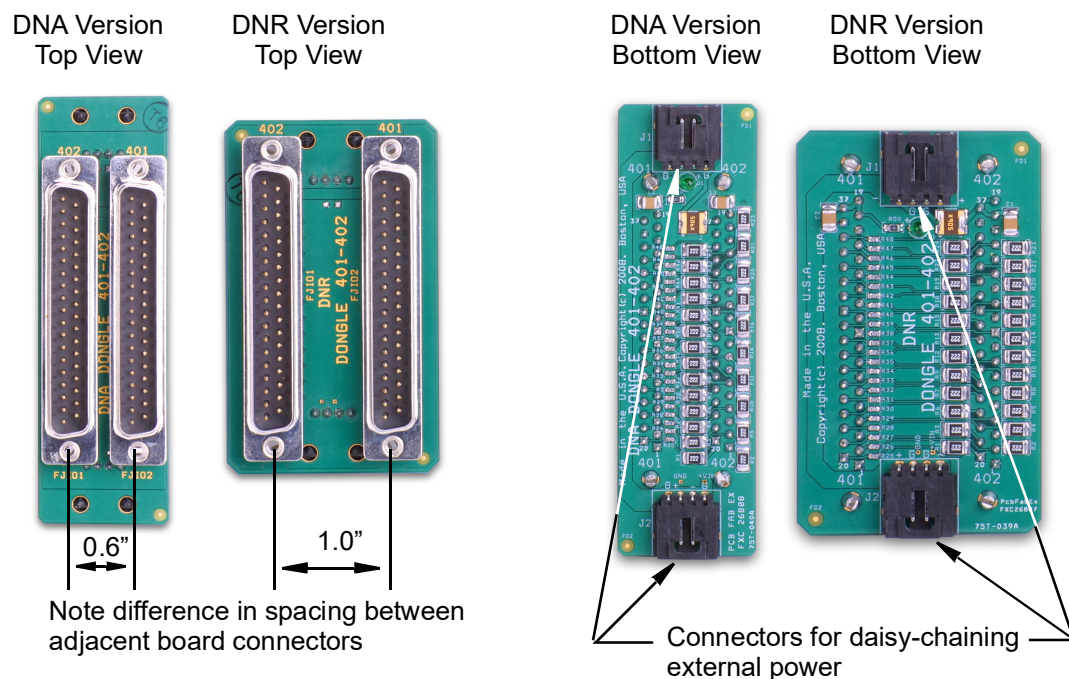


Figure 14-1 Photo of 401-to-402 Test Adapter



The basic concept of the test system is that a digital signal is output from a channel of the DIO-402, passed through the 401-to-402 Test Adapter, and then passed to an input channel on the DIO-401, thus exercising both boards. Power is supplied from an external 7-36V source that may be connected in a daisy-chain from one Test Adapter to another.

14.2 Device Architecture

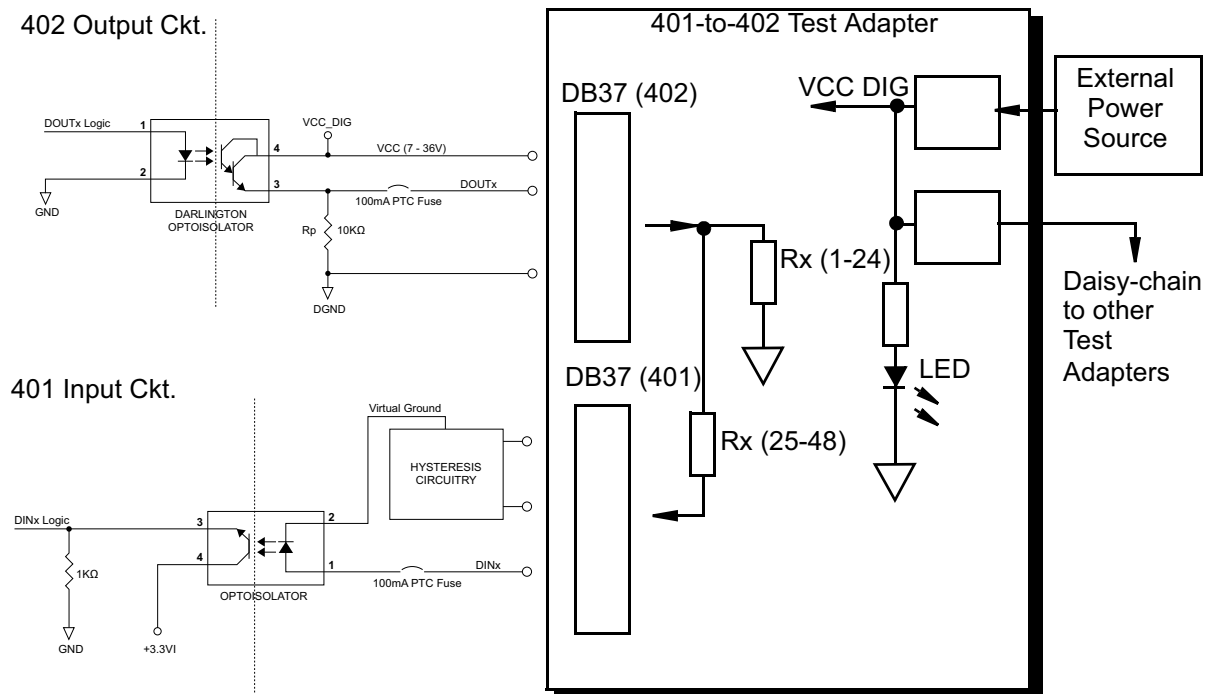


Figure 14-2 Block Diagram of 401-to-402 Test Adapter

As shown in **Figure 14-2** above, a digital output circuit from a channel on the DIO-402 connects the external VCC to ground through a channel load resistor located on the 401-to-402 Test Adapter. The signal then passes through another resistor to the 401 connector and then to an input channel of the 401.

The 402 detects the flow of current through the load resistor and, thus, the presence of the voltage signal on that channel. Similarly, the 401 detects the voltage applied to the input terminals of the 401.

In all cases, the presence of VCC from the external source is visually indicated by an LED mounted on the Test Adapter.



The pinouts of the DIO-401, the DIO-402, and the 401-to-402 Test Adapter are shown in **Figure 14-3**, along with a schematic of the test adapter circuit.

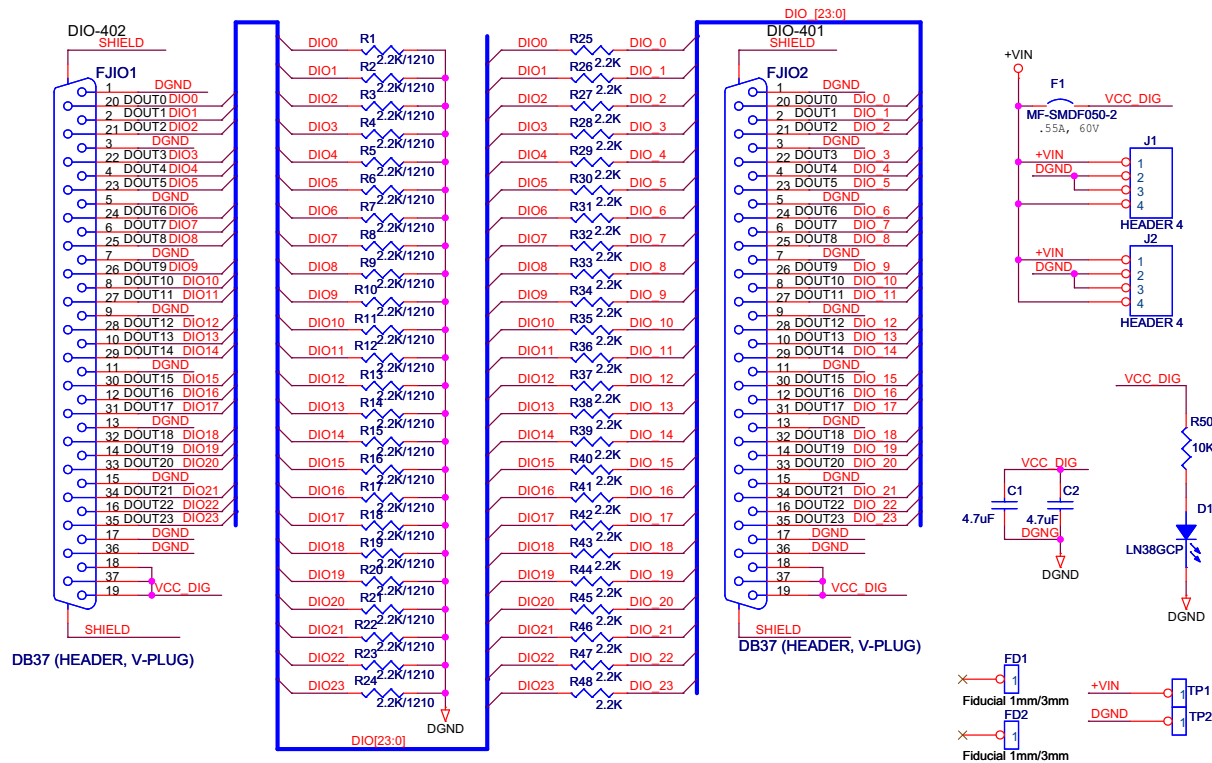


Figure 14-3 Schematic and Pinout of 401-to-402 Test Adapter

14.3 Using the 401-to-402 Test Adapter

Testing the DNx-DIO-401 Digital Input Board and DNx-DIO-402 Digital Output Board with the 401-to-402 Test Adapter requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. In particular, UEI Framework contains examples in the Analog Input folders and Analog Output folders that can be used to operate the AI-207 and AO-332 boards together. Please refer to the DNx-DIO-401 and DIO-402 User Manuals for information about programming the DIO-401 and DIO-402.



14.4 Specifications Technical specifications for the 401-to-402 Test Adapter are listed in **Table 14-1** below.

Table 14-1 Technical Specifications for the 401-to-402 Test Adapter

Channel Configurations	
Number of channels	24 digital outputs (DIO-402) and 24 digital inputs (DIO-401)
Logic level	5V to VCC
Power Input to Test Adapter	7-36V (24V nominal) from external power source
Power Output from Test Adapter	7-36V (24V nominal) from external source can be daisy-chained to other Test Adapters
Visual Indication	LED on Test Adapter indicates presence of VCC.
General Specifications	
Connector	Two DB-37 male
Overvoltage protection	-40V to +55V
ESD Protection	15 kV
Power Consumption	Less than 1 W
Operating Temperature	-40°C to +85°C
Operating Humidity	5 to 90%, non-condensing



403 Test Adapter

The 403 Test Adapter (p/n DNx-TADP-403) is an accessory designed for testing UEI's DNx-DIO-403 Digital Input/Output Board.

15.1 General Description

Under software control, the 403 Test Adapter facilitates tests on all 48 channels of a DNx-DIO-403 Digital Input/Output Board. The Test Adapter is designed to plug into a mating DB62 connector on a DIO-403 board.

The basic concept of the test system is that a digital signal is output from a group of eight channels of the DIO-403, passed to the Test Adapter and looped back through current limiting resistors to another group of eight input channels on the DIO-403. The direction of the signal is then reversed so that all channels are tested both as input and output channels. All 48 channels can be exercised in this manner (three 8-channel input groups and three 8-channel output groups, two directions).

An LED on the 403 Test Adapter indicates when +5V is applied from the DIO-403 to the Test Adapter. Power for the digital output signals is supplied by the DIO-403.

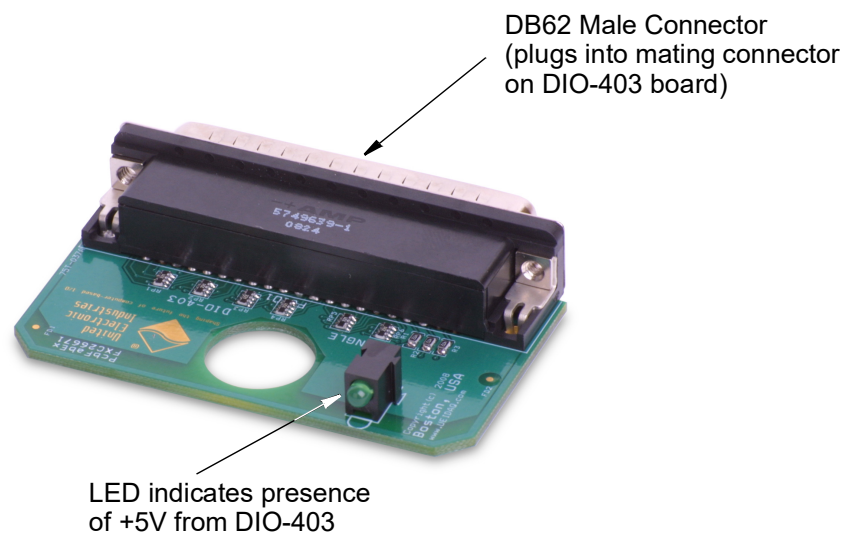


Figure 15-1 Photo of 403 Test Adapter



15.2 Device Architecture

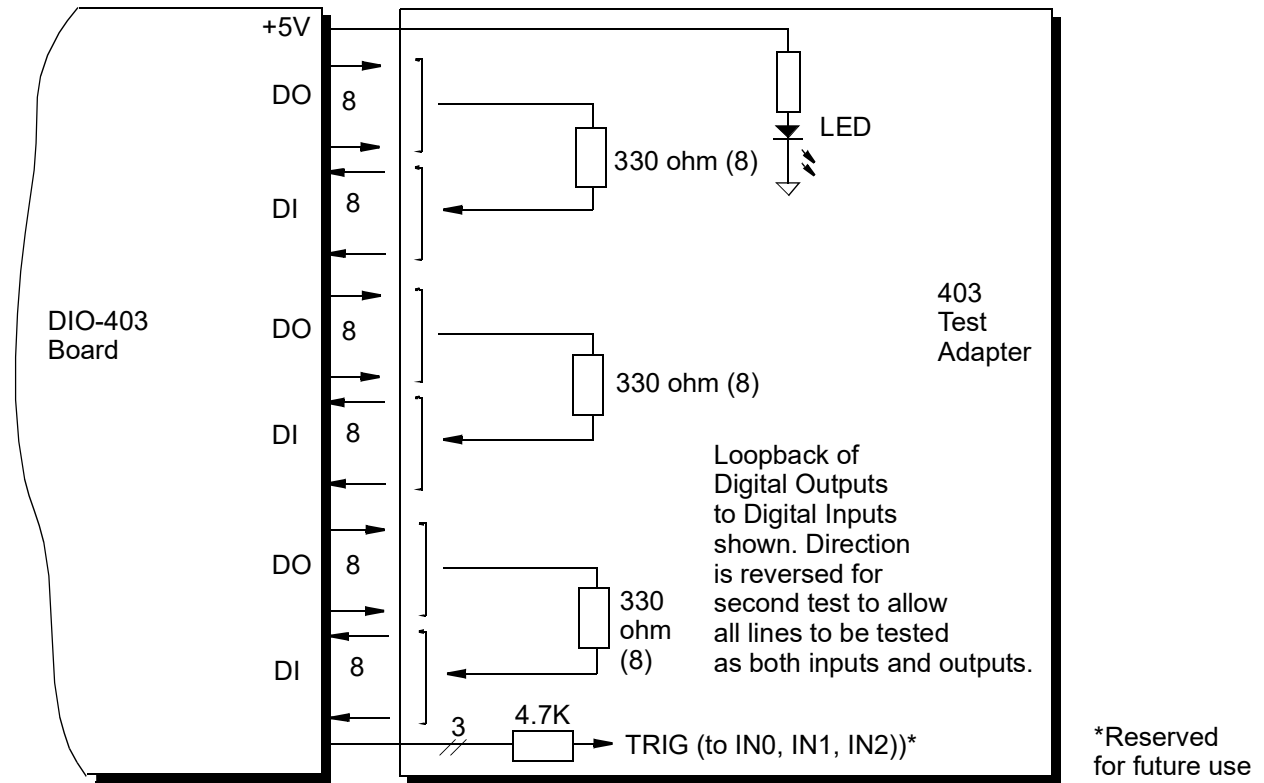


Figure 15-2 Block Diagram of 403 Test Adapter

Figure 15-2 above illustrates how three groups of eight lines on the DIO-403 are connected through resistors to other groups of eight lines and then tested as digital outputs and inputs, first in one direction and then in the opposite. Thus, all lines are tested both as outputs and as inputs.

The pinouts of the DIO-403 and the 403 Test Adapter are shown in **Figure 15-3**, along with a schematic of the Test Adapter circuit.

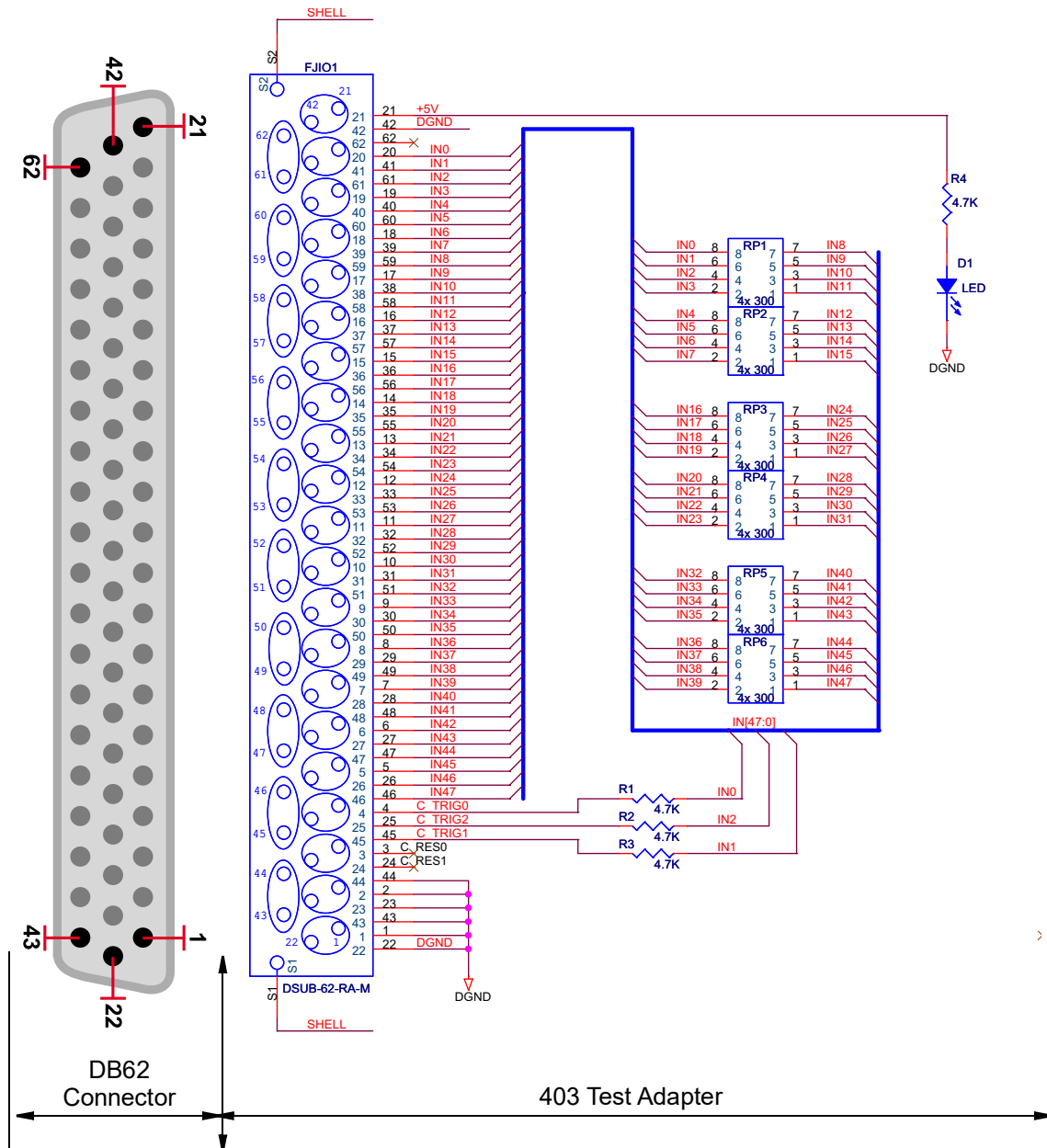


Figure 15-3 Schematic and Pinout of 403 Test Adapter

15.3 Using the 403 Test Adapter

Testing the DNx-DIO-403 Digital Input/Output Board with the DNx-TADP-403 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-DIO-403 User Manual for information about programming the DIO-403.



15.4 Specifications Technical specifications for the 403 Test Adapter are listed in **Table 15-1** below.

Table 15-1 Technical Specifications for the 403 Test Adapter

Channel Configurations	
Number of channels	48 digital inputs/48 digital outputs (direction selectable in groups of eight)
Input high voltage	2.4V
Input low voltage	0.8V
Output high voltage	4.5V @ 2mA, 3V @ 16 mA
Output low voltage	0.5V
I/O throughput	10kS/s (20k aggregate)
Visual Indication	LED on Test Adapter indicates presence of +5VDC.
General Specifications	
Connector	DB-62 male
Overvoltage protection	±30V p-p
ESD Protection	7 kV
Operating Temperature	-40°C to +85°C
Operating Humidity	5 to 90%, non-condensing



404/405/406 Test Adapter

The 404/405/406 Test Adapter (p/n DNx-TADP-404) is an accessory designed for testing UEI's DNx-DIO-404, DNx-DIO-405, and DNx-DIO-406 Digital Input/Output Boards.

16.1 General Description

Under software control, the 404/405/406 Test Adapter facilitates input or output tests on all 24 channels of a DNx-DIO-404, -405, or -406 Digital Input/Output Board. The Test Adapter is designed to plug into a mating DB37 connector on the applicable DIO board. It also accepts power from a 3-36VDC external power source via a daisy-chained cable.

The basic concept of the test system is that a simulated digital signal is either input to or output from a channel of the DIO-404, -405, or -406 and connected through resistors in the Test Adapter to a power source or to ground. A board mounted jumper permits the user to select a current sink or current source type of circuit for the test.

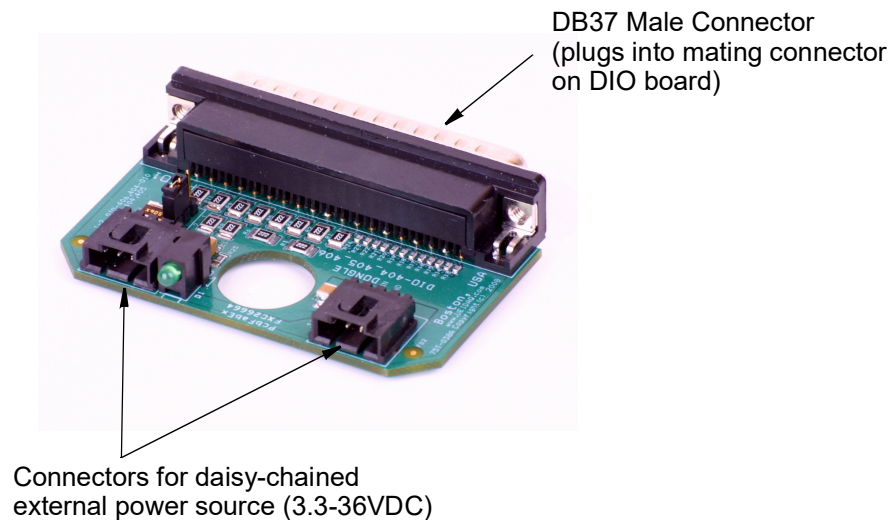


Figure 16-1 Photo of 404/405/406 Test Adapter



16.2 Device Architecture

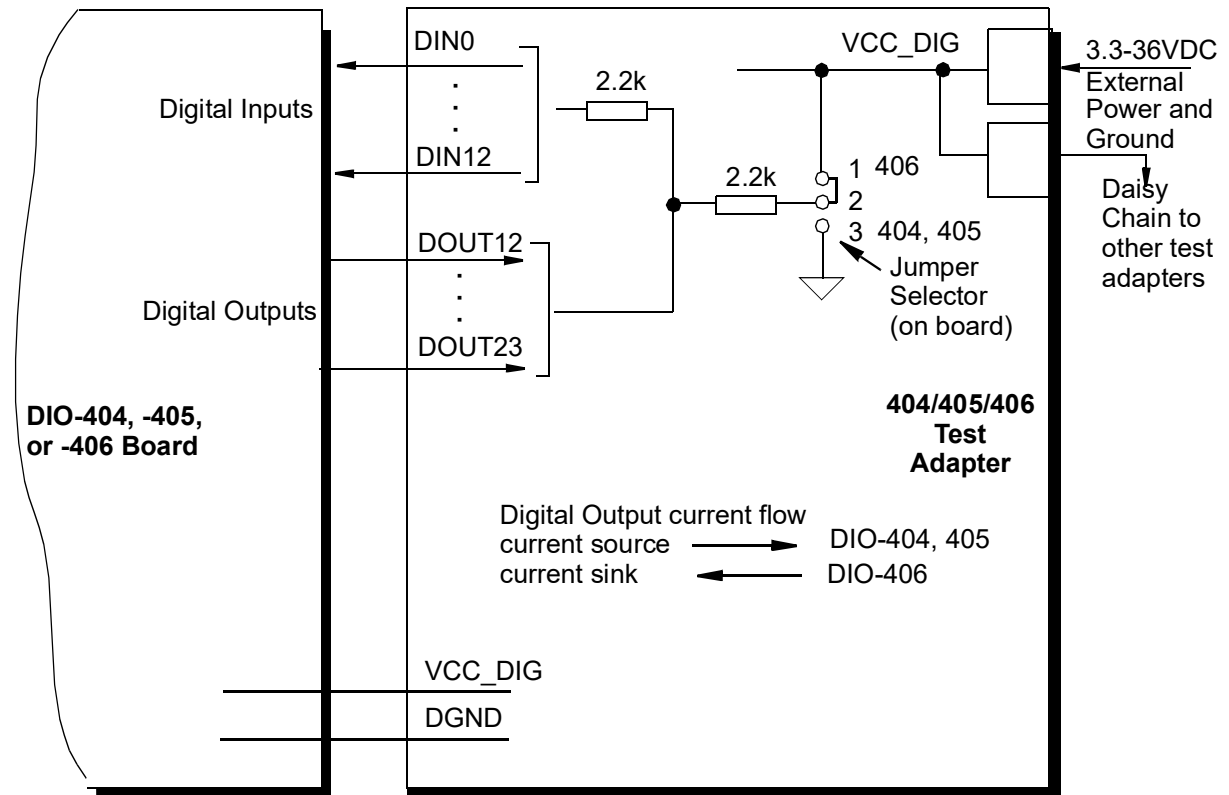


Figure 16-2 Block Diagram of 404/405/406 Test Adapter

Figure 16-2 above shows how digital inputs are connected via a jumper to **VCC_DIG**, where **VCC_DIG** is input from an external power source. For the **DIO-406**, the jumper connects terminals 1 and 2, which also connects digital outputs as current sinks. For the **DIO-404** and **-405**, the jumper is connected between terminals 2 and 3, which also connects digital outputs to ground as current sources. External power is connected to the Test Adapter by a daisy-chained cable.



The pinouts of the DIO-404/405/406 and the 404/405/406 Test Adapter are shown in **Figure 16-3**, along with a schematic of the Test Adapter circuit.

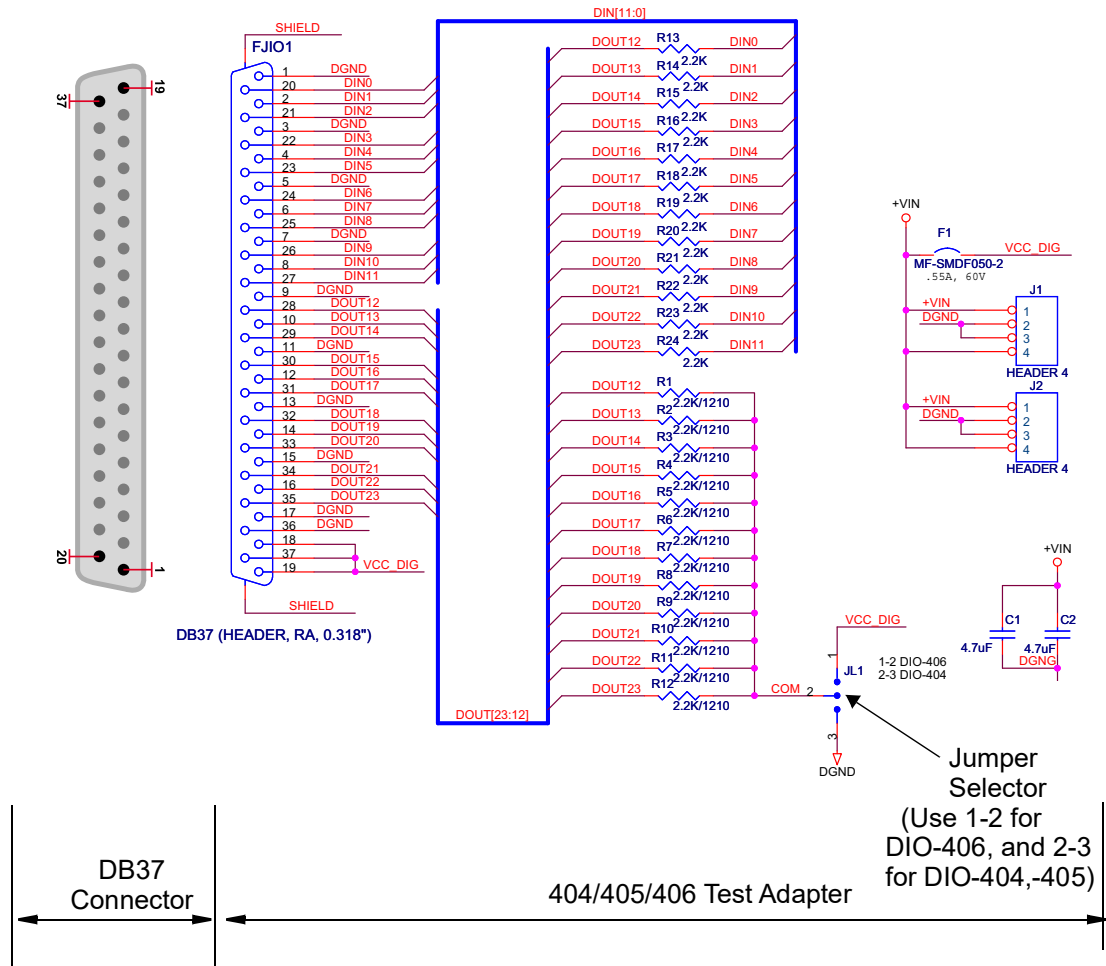


Figure 16-3 Schematic and Pinout of 404/405/406 Test Adapter

16.3 Using the 404/405/406 Test Adapter

Testing the DNx-DIO-404, DNx-DIO-405, and DNx-DIO-406 Digital Input/Output Boards with the DNx-TADP-404 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-DIO-404/405/406 User Manuals for information about programming the DIO-404/405/406.



16.4 Specifications Technical specifications for the 404/405/406 Test Adapter are listed in **Table 16-1** below.

Table 16-1 Technical Specifications for the 404/405/406 Test Adapter

Channel Configuration					
Number of channels	12 digital inputs/12 digital outputs (jumper selectable for current sink or current source operation with DIO-404, -405, -406)				
Logic Level	3.3-36V; rated for 4.4V, 5V, 12V, 24V, 36V				
Input Current	360uA max				
Input Protection	±40 V over/under voltage, 3 kV ESD				
Input High Voltage	@3.3V	@5V	@12V	@24V	@36V
(with default hysteresis)	1.6V	2.7V	7.5V	12V	17V
Input Low Voltage	@3.3V	@5V	@12V	@24V	@36V
(with default hysteresis)	1.5V	1.8V	2.0V	3.0V	12.5V
Output High Voltage	3.1V 4.5V 23.4V 35.4V				
3.3V at 10 ohm load					
5V at 18 ohm load					
24V at 66 ohm load					
36V at 100 ohm load					
Output low voltage	Floating when driven with logic "0"				
I/O Throughput	100kHz max				
Power Requirements (VCC)	3.3-36V (24V nominal) from external source, or use the DIO board's internal 24V supply				
General Specifications					
Connector	DB-37 male				
Operating Temperature	-40°C to +85°C				
Operating Humidity	90%, non-condensing				



429-566 Test Adapter

The 429-566 Test Adapter (p/n DNx-TADP-566) is an accessory designed for testing UEI's DNx-ARINC-429-566 ARINC Interface Board.

17.1 General Description

Under software control, the 429-566 Test Adapter facilitates loopback tests on all channels of a DNx-429-566 ARINC Interface Board. (A different Test Adapter is required for a DNx-429-512 and DNx-429-516 Interface board.) As shown in the block diagram of **Figure 17-2**, the Dnx-429-566 layer is configured with 6 transmitter channels with internal loopback connection to 6 receiver channels plus 6 independent receiver channels. The 6 independent channels are connected to the transmitter outputs via external loopback in the 429-566 Test Adapter.

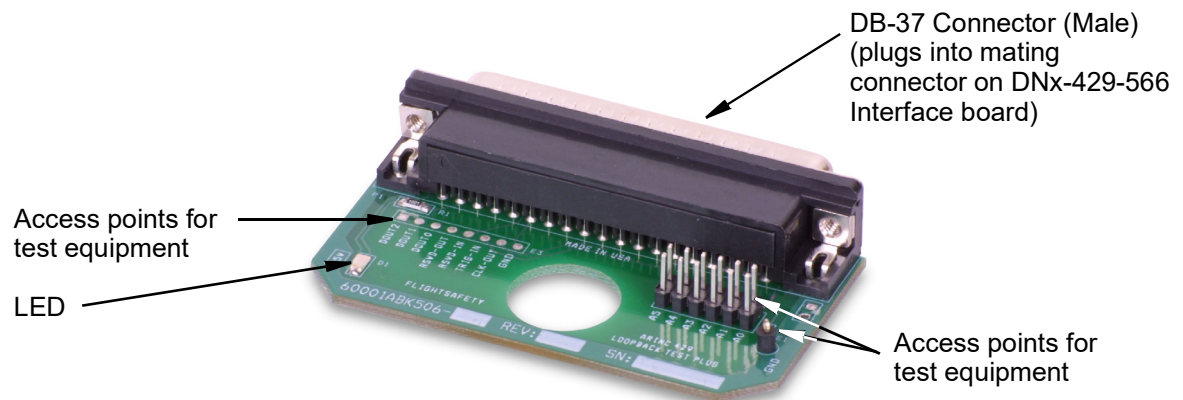


Figure 17-1 Photo of 429-566 Test Adapter



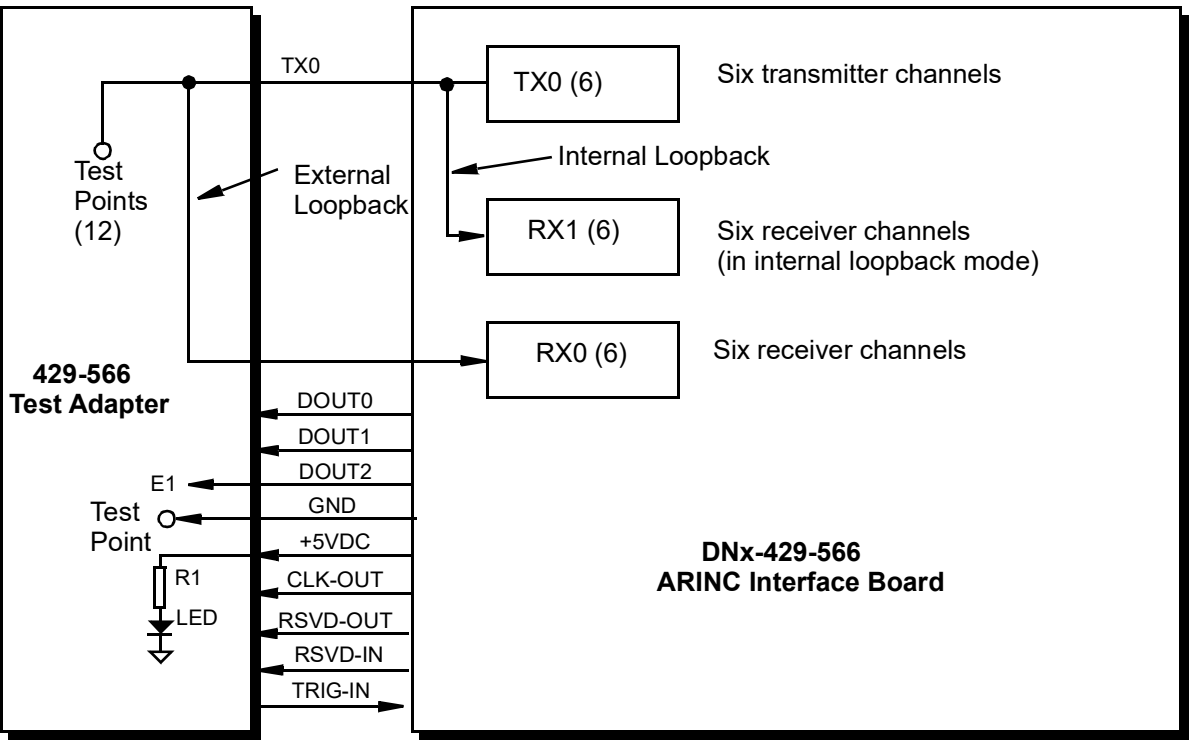


Figure 17-2 Block Diagram of 429-566 Test Adapter



The external loopback connections on the Test Adapter are shown in the schematic diagram in **Figure 17-3** below.

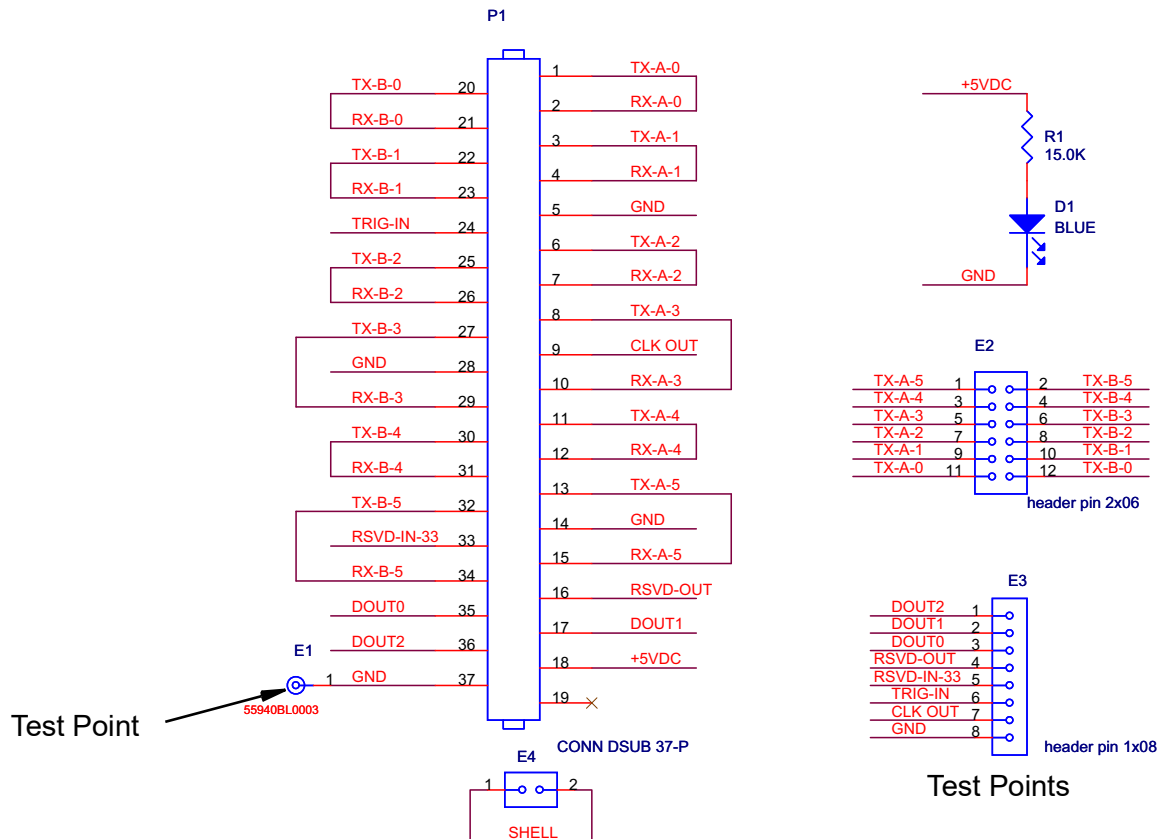


Figure 17-3 Schematic of the 429-566 Test Adapter

17.2 Pinout

The pinout for the DB-37 connector is shown in **Figure 17-4**.

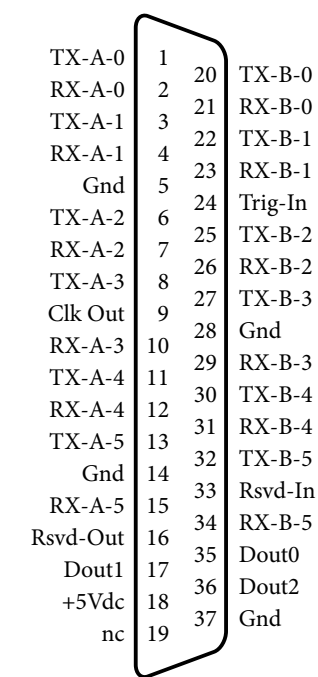


Figure 17-4 Pinout of 429-566 Test Adapter

17.3 Using the 429-566 Test Adapter

Testing the DNx-ARINC-429-566 ARINC Interface Board with the DNx-TADP-566 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-429-566-512 User Manual for information about programming the ARINC-429-566.

17.4 Specifications Technical specifications for the 429-566 Test Adapter are listed in **Table 17-1** below.

Table 17-1 Technical Specifications for the 429-566 Test Adapter

Channel Configurations	
Number of channels	Test Adapter connects 6 transmitter inputs to six receivers. Internal loopback on layer connects the same transmitters to six additional receivers.
Inputs	6 Transmitter, 3 Dout, 5VDC, 4 Gnd, 1 Clk-Out, 1 Rsvd-Out
Outputs	6 Receiver, 1 Rsvd-In, 1 Trig-In
LED	One to indicate 5VDC present
Test Points	20 access points plus ground
General Specifications	
Connector	DB-37 male
ESD Protection	15 kV
Power Consumption	Less than 1 W.
Operating Temperature	-40°C to +85°C



432/433 Test Adapter

The 432/433 Test Adapter (p/n DNx-TADP-432 and DNx-TADP-433) is an accessory designed for testing UEI's DNx-DIO-432 and DNx-DIO-433 Digital Output Boards. The 432 is configured for current sinking; the 433 is designed for current sourcing. Both provide continuous monitoring of current and voltage on each channel.

18.1 General Description

Under software control, the 432/433 Test Adapter facilitates tests on all 32 channels of a DNx-DIO-432/433 Digital Output board. The circuit of the Test Adapter connects a resistor to each output, causing a current to flow when the switch/bit is activated. The current through the resistor and the voltage across a known resistor in the circuit are monitored by the 432 or 433 being tested. The magnitude of the current and voltage vary with the voltage applied by the external power source. The user test program, therefore, can be written to test the digital outputs at various levels as needed by the application. The test program can also be written to verify accuracy of overcurrent and overvoltage protection trip points on each channel.

The LED is ON when the external power source is connected and ON.

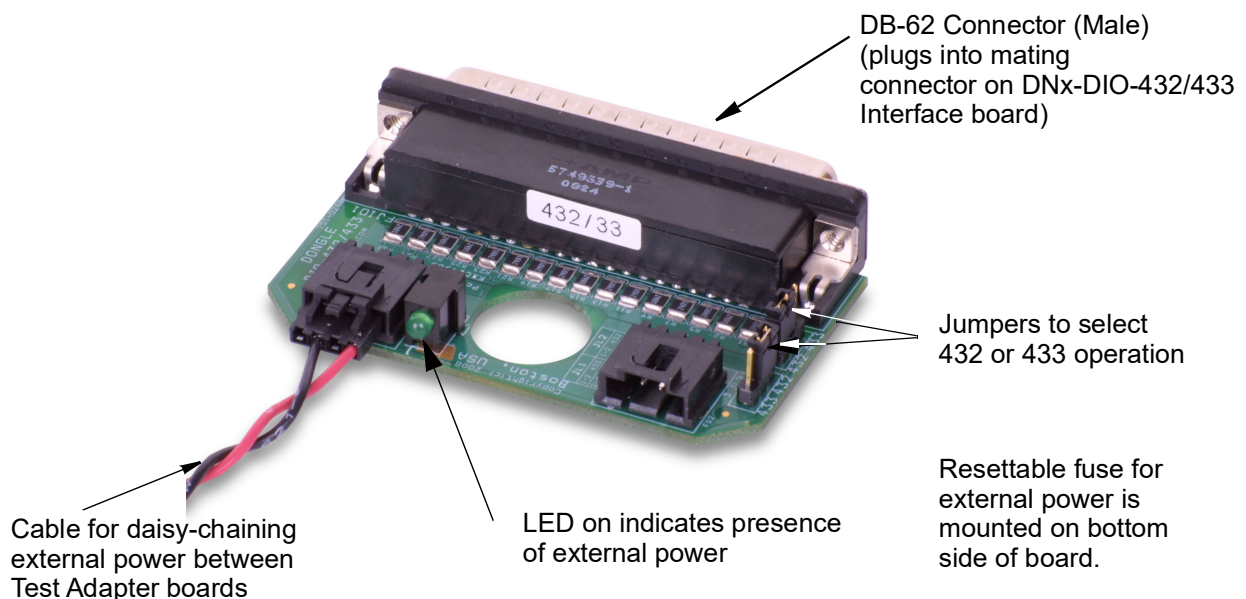


Figure 18-1 Photo of 432/433 Test Adapter



18.2 Device Architecture

As shown in **Figure 18-2** and **Figure 18-3**, the circuit of the 432/433 Test Adapter connects a resistor between each digital output terminal and ground for 432 mode, and between each output terminal and VIN+ for 433 mode.

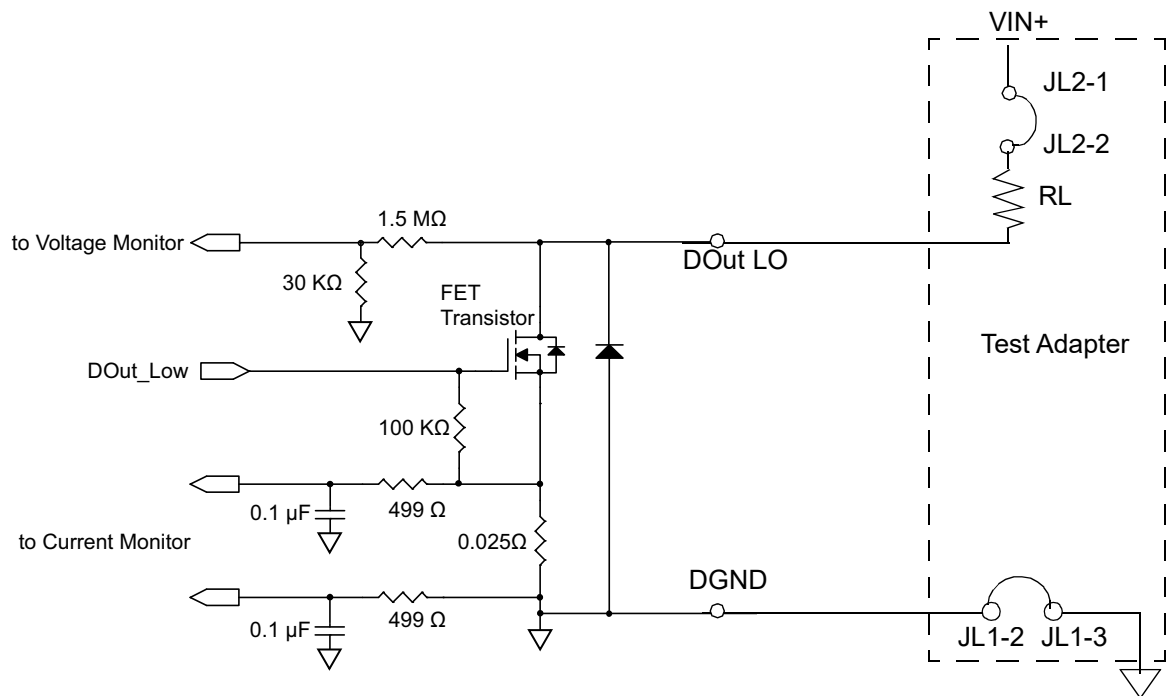


Figure 18-2 Output Circuit Diagram of DIO-432

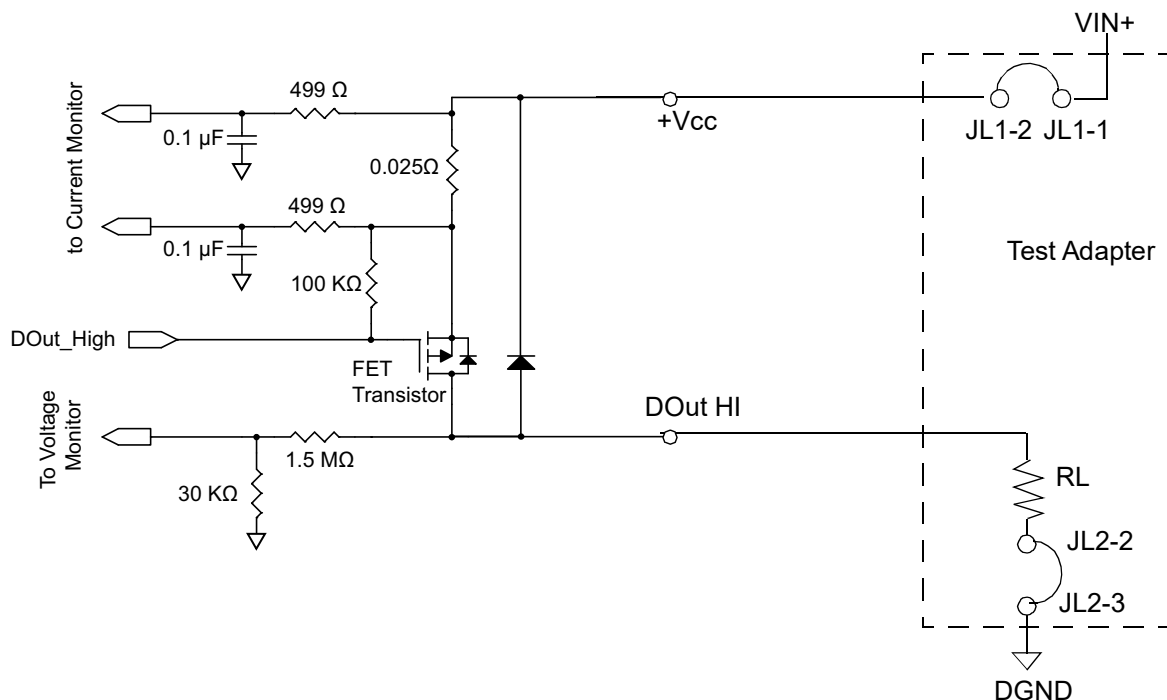


Figure 18-3 Output Circuit Diagram of DIO-433



The pinouts of the DIO-432/433 and the 432/433 Test Adapter are shown in **Figure 18-4**, along with a schematic of the Test Adapter circuit. Note that the user can select 432 or 433 configuration of the Test Adapter by inserting jumpers in the marked positions for the J1 and J2 headers.

The external power source should be wired to the 4-pin cable connector on the Test Adapter. Additional cables can be used to daisy-chain power to other test adapters.

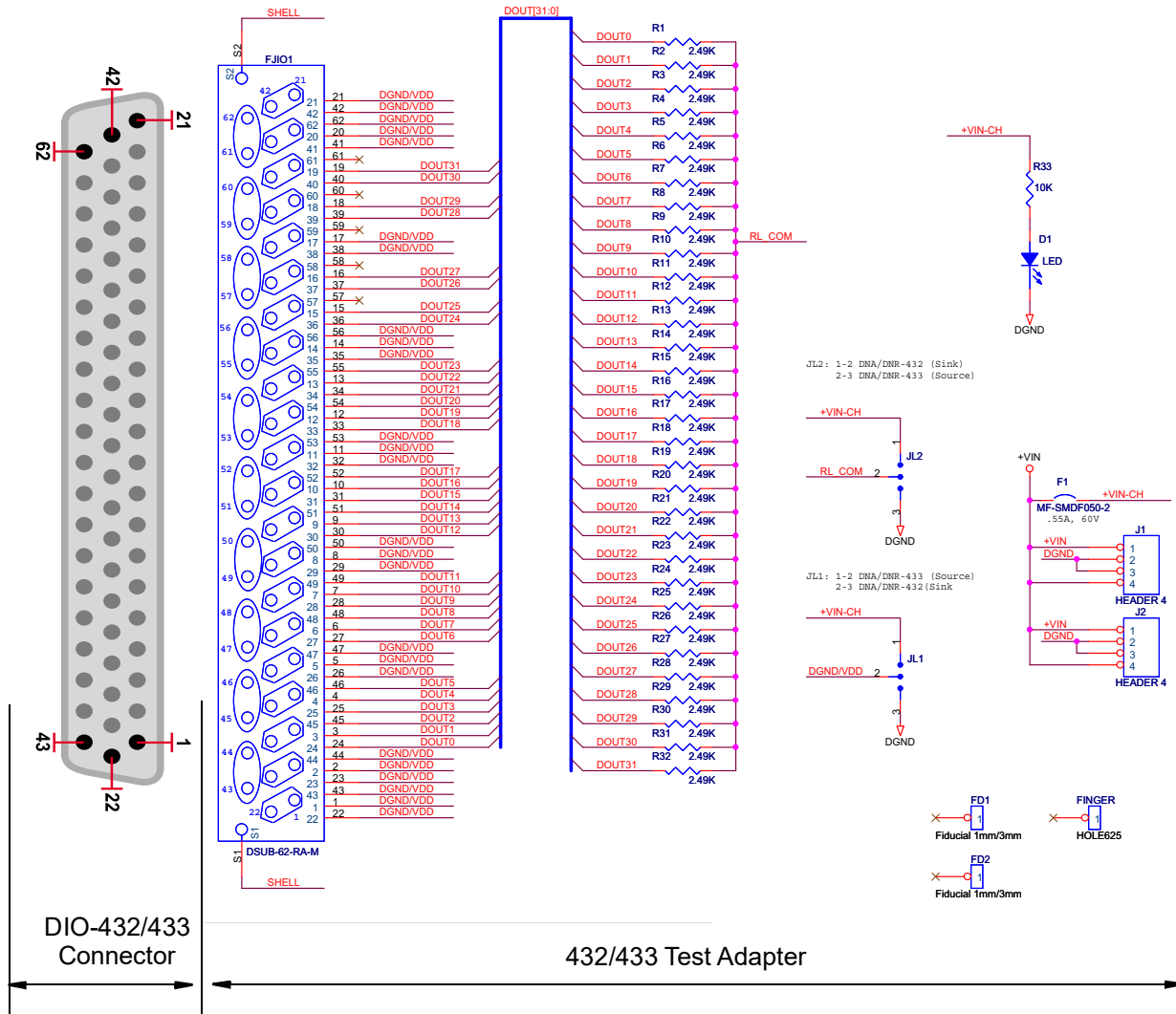


Figure 18-4 Schematic and Pinout of 432/433 Test Adapter

18.3 Using the 432/433 Test Adapter

Testing the DNx-DIO-432 and DNx-DIO-433 Digital Output Boards with the 432/433 Test Adapter requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-DIO-432-3 User Manual for information about programming the DIO-432/433.



18.4 Specifications Technical specifications for the 432/433 Test Adapter are listed in **Table 18-1** below.

Table 18-1 Technical Specifications for the 432/433 Test Adapter

Channel Configurations	
Number of channels	32
Configuration	Jumper-selectable for DIO-432 or DIO-433 tests.
Input Specifications	
Input Types	Digital Output, either current source (433) or current sink (432)
Output Port Configuration	Single 32-bit word
DIO-432/433 Output Drive	600 mA per channel continuous, 3.5A peak 10% duty cycle 100 ms max.
Output ON voltage drop	<500 mV @600 mA
Output ON impedance	0.9 ohm
Output OFF impedance	>1 Megohm
Output OFF leakage	<25 uA
Overvoltage protection	±40 VDC (reverse current must be limited to prevent damage)
Overcurrent protection	
Current limit	50 mA - 2A
Overload response time	10 - 5000 ms (user programmable)
Output Monitoring	
Configuration	Multiplexed
Voltage Accuracy	±10 mV max (sampled at 2 Hz)
Current Accuracy	±1 mA max (sampled at 10 Hz)
Soft-Start PWM Output	256 uS to 5 seconds
Steady State PWM Output	0 to 100% in 0.4% increments. (Minimum period is 256 uSec.)
Output Throughput Rate	1 kHz max
Power up/reboot state	Off
Power dissipation	<2 W, not including output switches
Operating Temp. Range	-40°C to +85°C
Operating Humidity	95%, non-condensing
General Specifications	
Connectors	DB-62 male, two 4-pin Molex RA cable
ESD Protection	15 kV
Power Consumption	Less than 2 W



448/449 Test Adapter

The 448/449 Test Adapter (p/n DNx-TADP-448 and DNx-TADP-449) is an accessory designed for testing UEI's DNx-DIO-448 and DNx-DIO-449 Digital Input Boards.

19.1 General Description

Under software control, the 448/449 Test Adapter facilitates tests on all 48 channels of a DIO-448/449 board. The Test Adapter circuit connects an external reference voltage V_{in} to even channels (DIO0, DIO2,...DIO46) and $0.5 \cdot V_{in}$ to odd channels (DIO1, DIO3,...DIO47). Users can configure the high and low voltage thresholds in their test program to verify that the digital state correlates with changes to the external supply.

The LED is ON when the external power source is connected and powered on. The external power source should be connected to the 4-pin cable connector on the Test Adapter. Additional cables can be used to daisy-chain power to other test plugs.

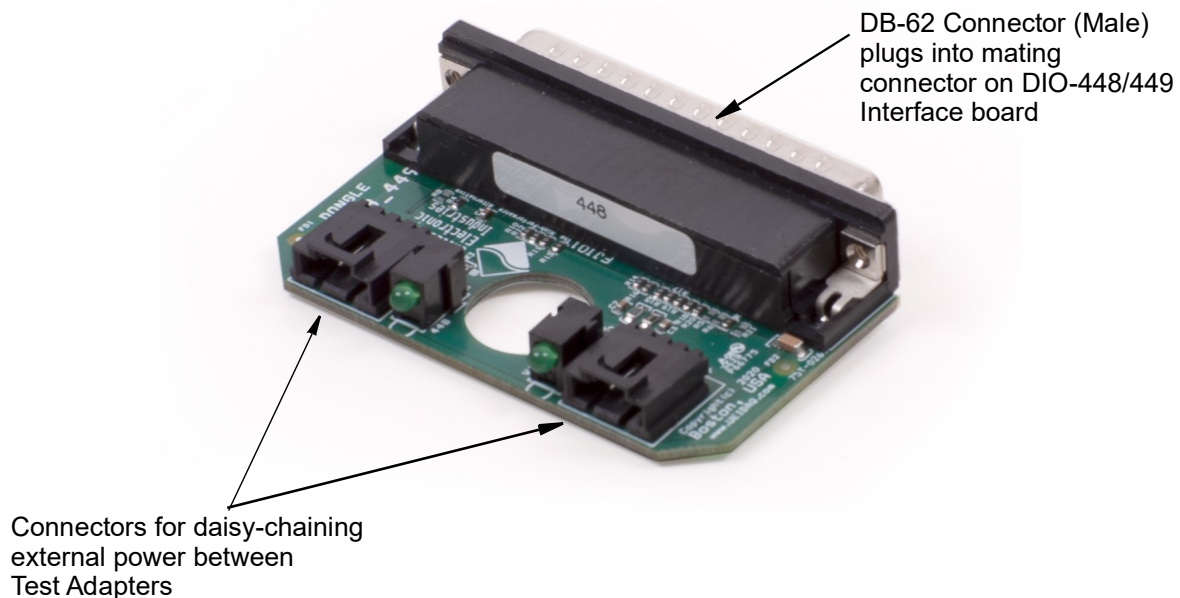


Figure 19-1 Photo of 448/449 Test Adapter

The pinouts of the DIO-448/449 and the 448/449 Test Adapter are shown in **Figure 19-2**, along with a schematic of the Test Adapter circuit. **Figure 19-3** shows how the $33k\Omega$ pullup/pulldown resistors on the DIO-448/449 divide the input voltage in half on odd channels.



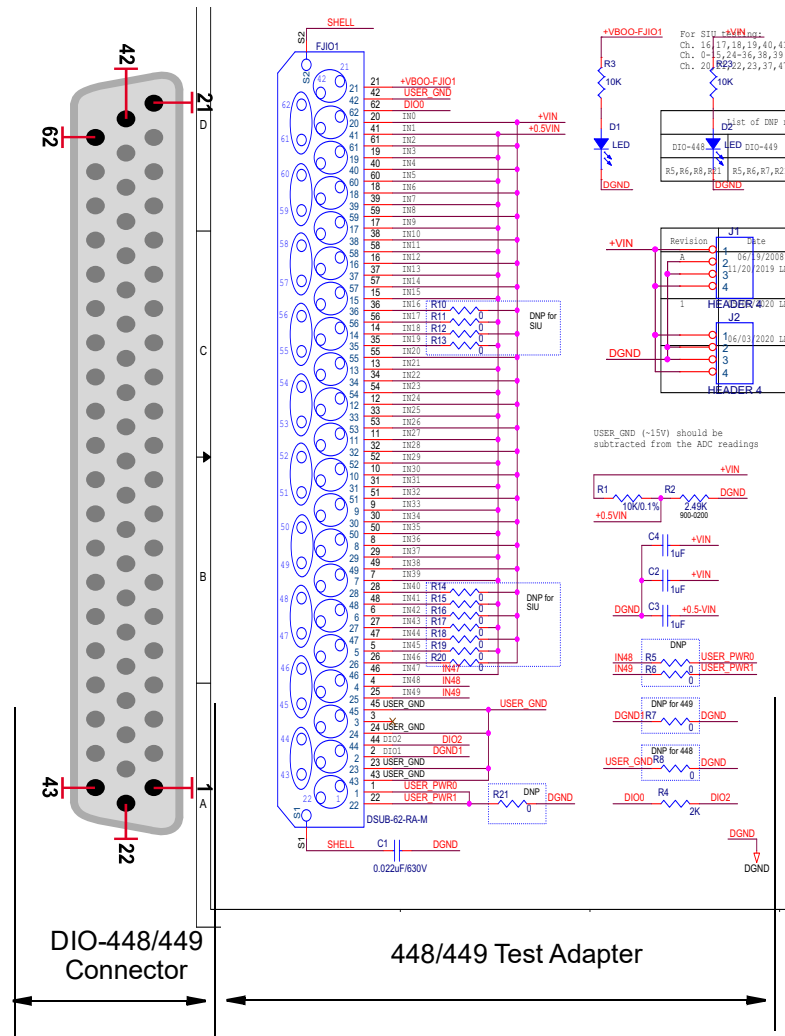


Figure 19-2 Schematic and Pinout of 448/449 Test Adapter

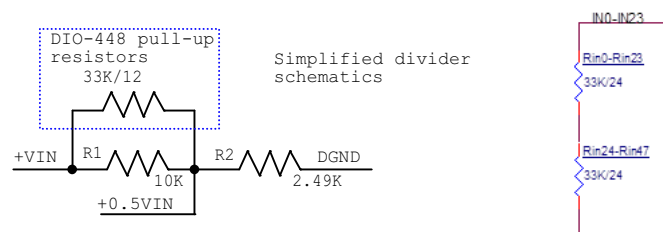


Figure 19-3 Divider Circuit on Odd Channels



19.2 Using the 448/449 Test Adapter

Testing the DNx-DIO-448 and DNx-DIO-449 Digital Input Boards with the DNx-TADP-448 and DNx-TADP-449 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-DIO-448 User Manual or DNx-DIO-449 User Manual for information about programming the DIO-448/449.



19.3 Specifications Technical specifications for the 448/449 Test Adapter are listed in **Table 19-1** below.

Table 19-1 Technical Specifications for the 448/449 Test Adapter

Number of channels	48 digital inputs
Expected Values	Even channels: +VIn Odd channels: +0.5*VIn
Power Source	Supplied by user
General Specifications	
Connectors	DB-62 male, two 4-pin Molex RA
Overvoltage Protection	-40V to +55V
ESD Protection	15 kV
Power Consumption	Less than 2 W
Operating Temp. Range	-40°C to +85°C
Operating Humidity	95%, non-condensing



501 Test Adapter

The 501 Test Adapter (p/n DNx-TADP-501) is an accessory designed for testing UEI's DNx-SL-501 Serial Interface Board.

20.1 General Description

Under software control, the 501 Test Adapter facilitates loopback tests on all channels of a DNx-SL-501 Serial Line Interface Board. Jumpers are used to switch between RS-232 mode and RS-422/485 modes.

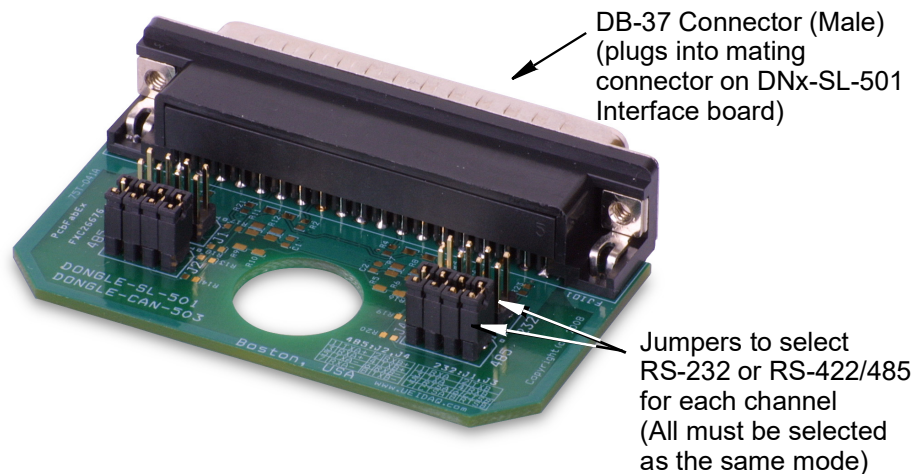
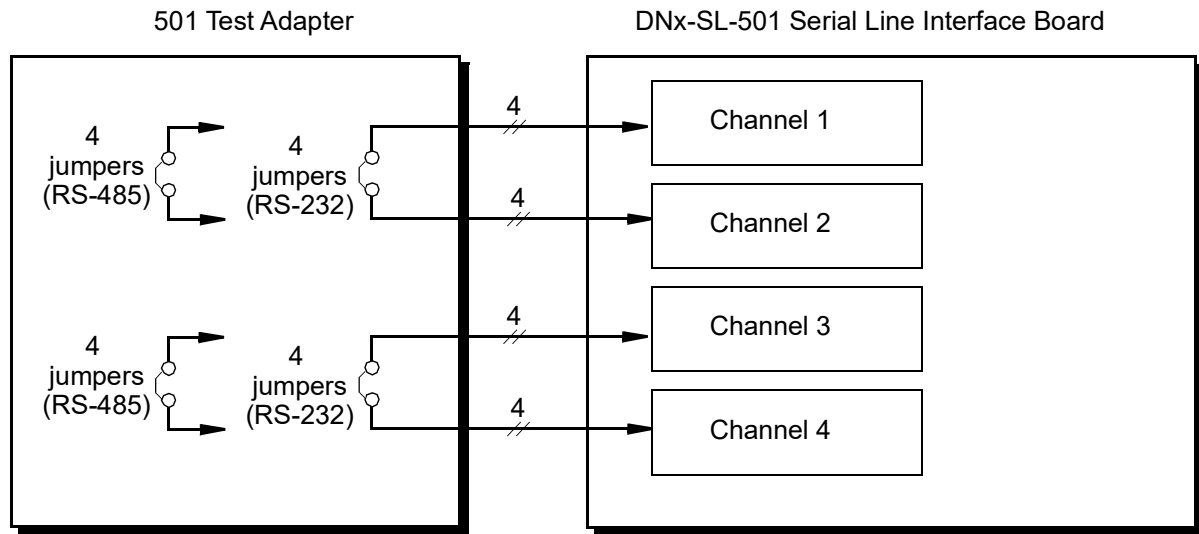


Figure 20-1 Photo of 501 Test Adapter



20.2 Device Architecture

As shown in **Figure 20-2**, the 501 Test Adapter provides 4 serial channels with loopback connections between Ch1 and Ch2, and Ch3 and Ch4. Note that headers are provided for insertion of jumpers to configure the Test Adapter as either an RS-232 or RS-485 device. To use the Test Adapter, all jumpers must be inserted and all must be in RS-232 headers or in RS-485 headers. The device will not function with any jumper in the wrong position.



Note:

All jumpers must be inserted in either 232 or 485 headers and cannot be mixed.

Figure 20-2 Block Diagram of 501 Test Adapter



The pinouts of the SL-501 and the 501 Test Adapter are shown in Figure 20-3, along with a schematic of the Test Adapter circuit.

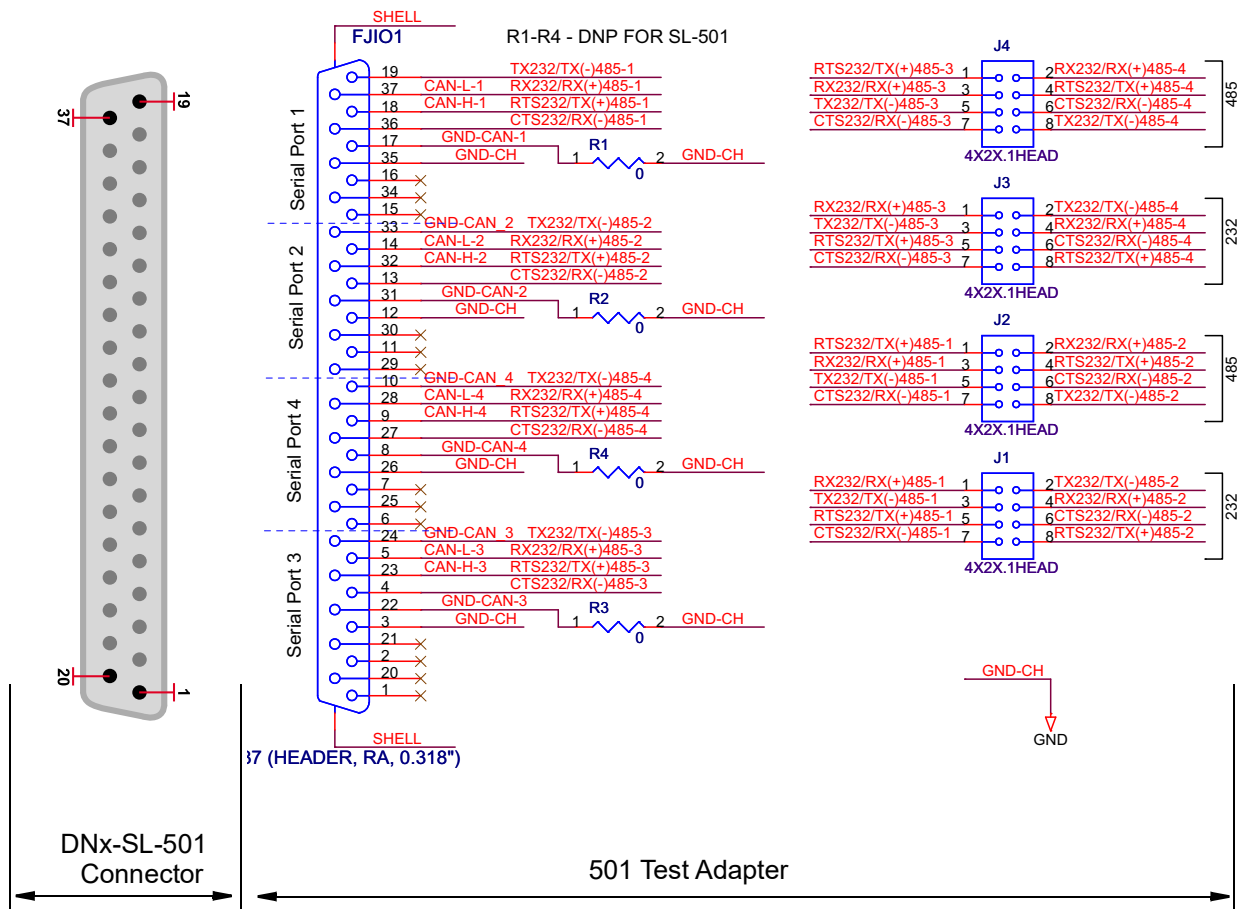


Figure 20-3 Schematic of 501 Test Adapter

20.3 Using the 501 Test Adapter

Testing the DNx-SL-501 Serial Interface Board with the DNx-TADP-501 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-SL-501 User Manual for information about programming the SL-501.



20.4 Specifications Technical specifications for the 501 Test Adapter are listed in **Table 20-1** below.

Table 20-1 Technical Specifications for the 501 Test Adapter

Channel Configurations	
Number of channels	Test Adapter cross-connects each channel to an adjacent channel (2 pairs). Software tests transmission of messages in both directions.
Serial Interfaces	All channels can be jumper-selected as RS-232 or RS-422/485 (all must be selected)
RS-422/485 Modes	Half and full duplex
Baud Rates RS-232 RS-422/485	Standard rates up to 250 kbaud Standard rates up to 1Mbaud as well as 12 kb, 12.5 kb, and 50.0 kb
General Specifications	
Connector	DB-37 male
ESD Protection	15 kV
Power Consumption	Less than 1 W
Operating Temperature	-40°C to +85°C
Operating Humidity	95%, non-condensing



503 Test Adapter

The 503 Test Adapter (p/n DNx-TADP-503) is an accessory designed for testing UEI's DNx-CAN-503 Controller Area Network Board.

21.1 General Description

Under software control, the 503 Test Adapter facilitates loopback tests on all channels of a DNx-CAN-503 Controller Area Network Board. As shown in **Figure 21-2**, the 503 Test Adapter provides four CAN channels with loopback connections between all channels, allowing you to send test messages in either direction between any channel and any other channel.

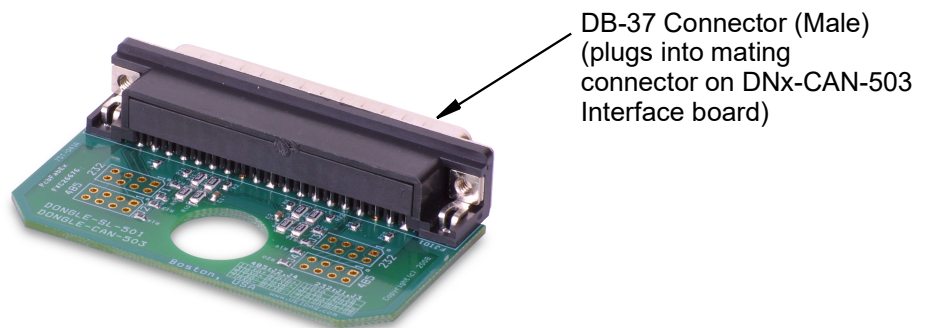


Figure 21-1 Photo of 503 Test Adapter

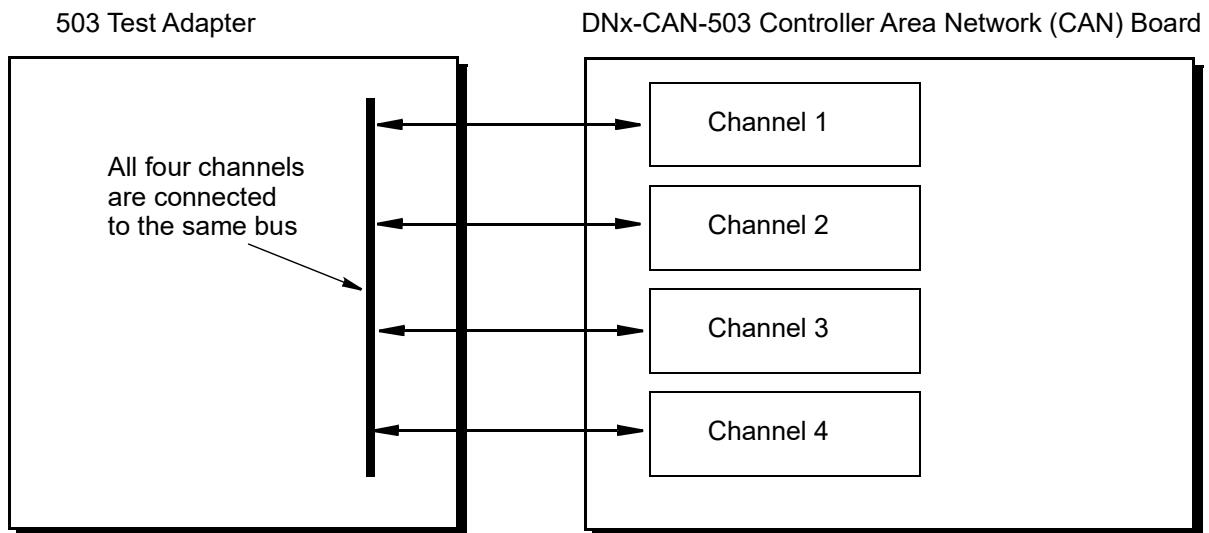


Figure 21-2 Block Diagram of 503 Test Adapter

The pinouts of the CAN-503 and the 503 Test Adapter are shown in **Figure 21-3**, along with a schematic of the Test Adapter circuit.

Note: Headers not populated

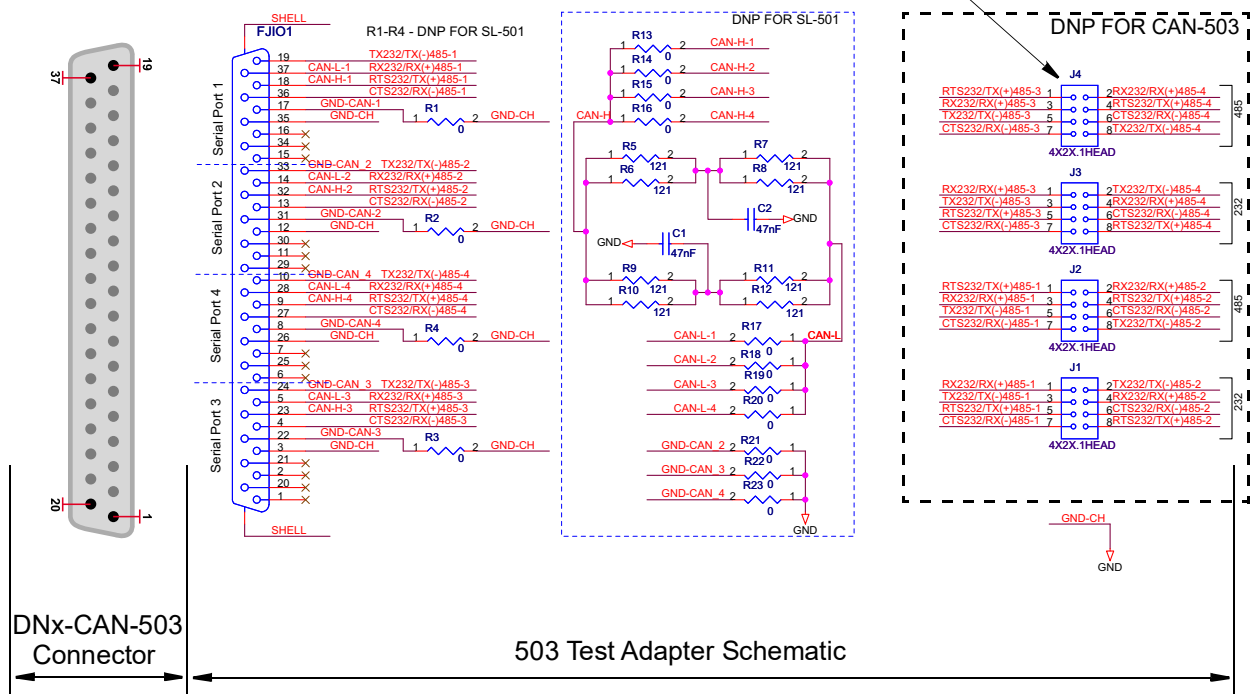


Figure 21-3 Schematic of 503 Test Adapter

21.2 Using the 503 Test Adapter

Testing the DNx-CAN-503 Controller Area Network Board with the DNx-TADP-503 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-CAN-503 User Manual for information about programming the CAN-503.



21.3 Specifications Technical specifications for the 503 Test Adapter are listed in **Table 21-1** below.

Table 21-1 Technical Specifications for the 503 Test Adapter

Channel Configurations	
Number of channels	Test Adapter connects all channels to the same CAN bus. Software tests transmission of messages in both directions among all four channels.
Max transfer rate	Up to 1 Mbit/s
General Specifications	
Connector	DB-37 male
ESD Protection	15 kV
Power Consumption	Less than 1 W
Operating Temperature	-40°C to +85°C
Operating Humidity	95%, non-condensing



508 Test Adapter

The 508 Test Adapter (p/n DNx-TADP-508) is an accessory designed for testing UEI's DNx-SL-508 Serial Interface Board.

22.1 General Description

Under software control, the 508 Test Adapter facilitates loopback tests on all channels of a DNx-SL-508 Serial Interface Board. Jumpers are used to switch between RS-232 mode and RS-422/485 modes.

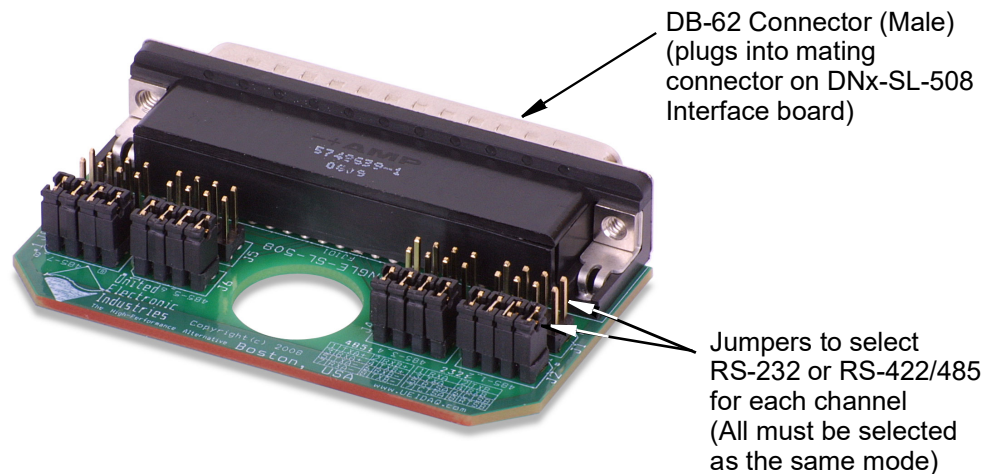


Figure 22-1 Photo of 508 Test Adapter



22.2 Device Architecture

As shown in **Figure 22-2**, the 508 Test Adapter provides 8 serial channels with loopback connections between Ch1 and Ch2, Ch3 and Ch4, Ch5 and Ch6, and Ch7 and Ch8. Note that headers are provided for insertion of jumpers to configure the Test Adapter as either an RS-232 or RS-485 device. To use the Test Adapter, all jumpers must be inserted and all must be in RS-232 headers or in RS-485 headers. The device will not function with any jumper in the wrong position.

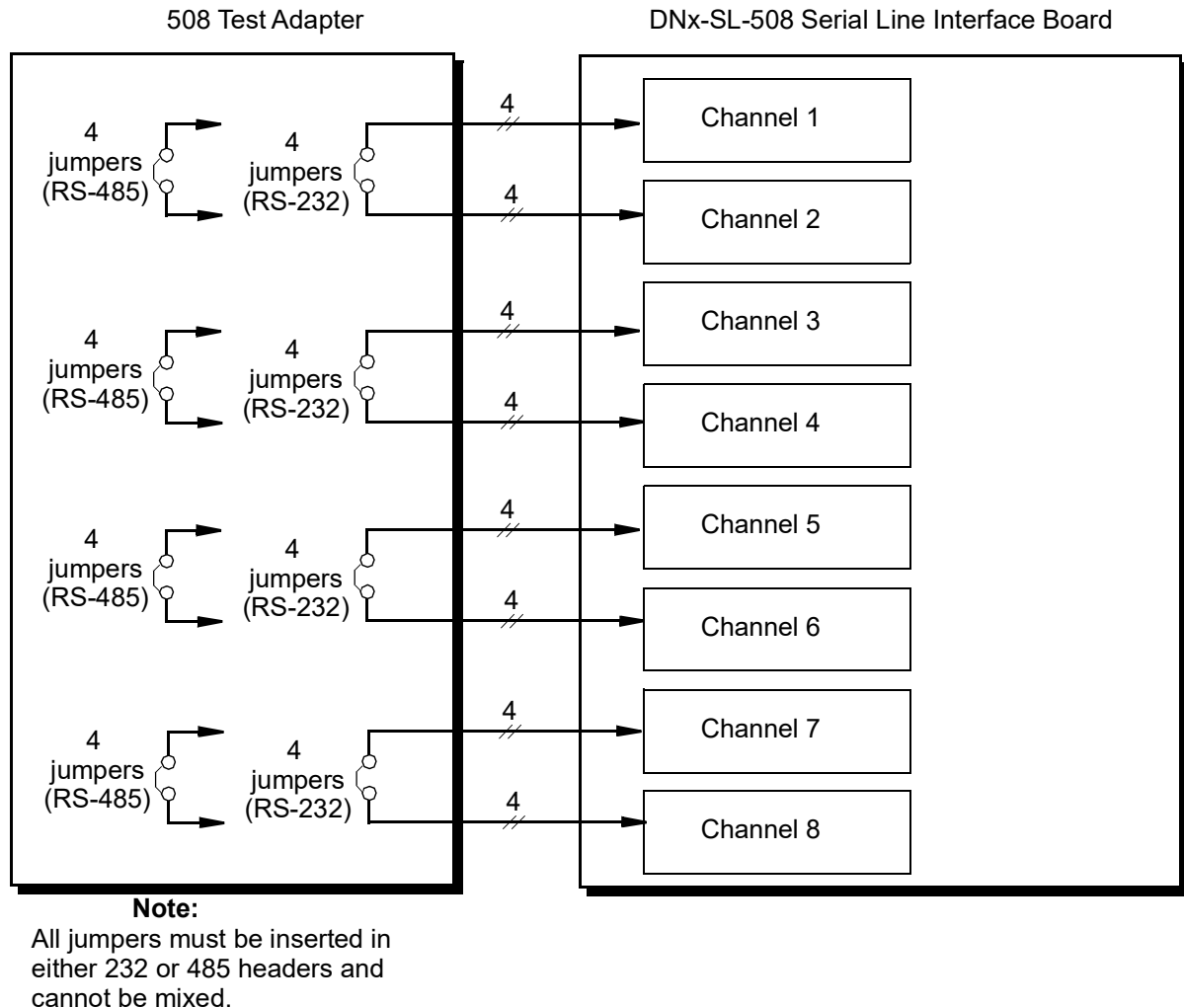


Figure 22-2 Block Diagram of 508 Test Adapter

The pinouts of the SL-508 and the 508 Test Adapter are shown in Figure 22-3, along with a schematic of the Test Adapter circuit.

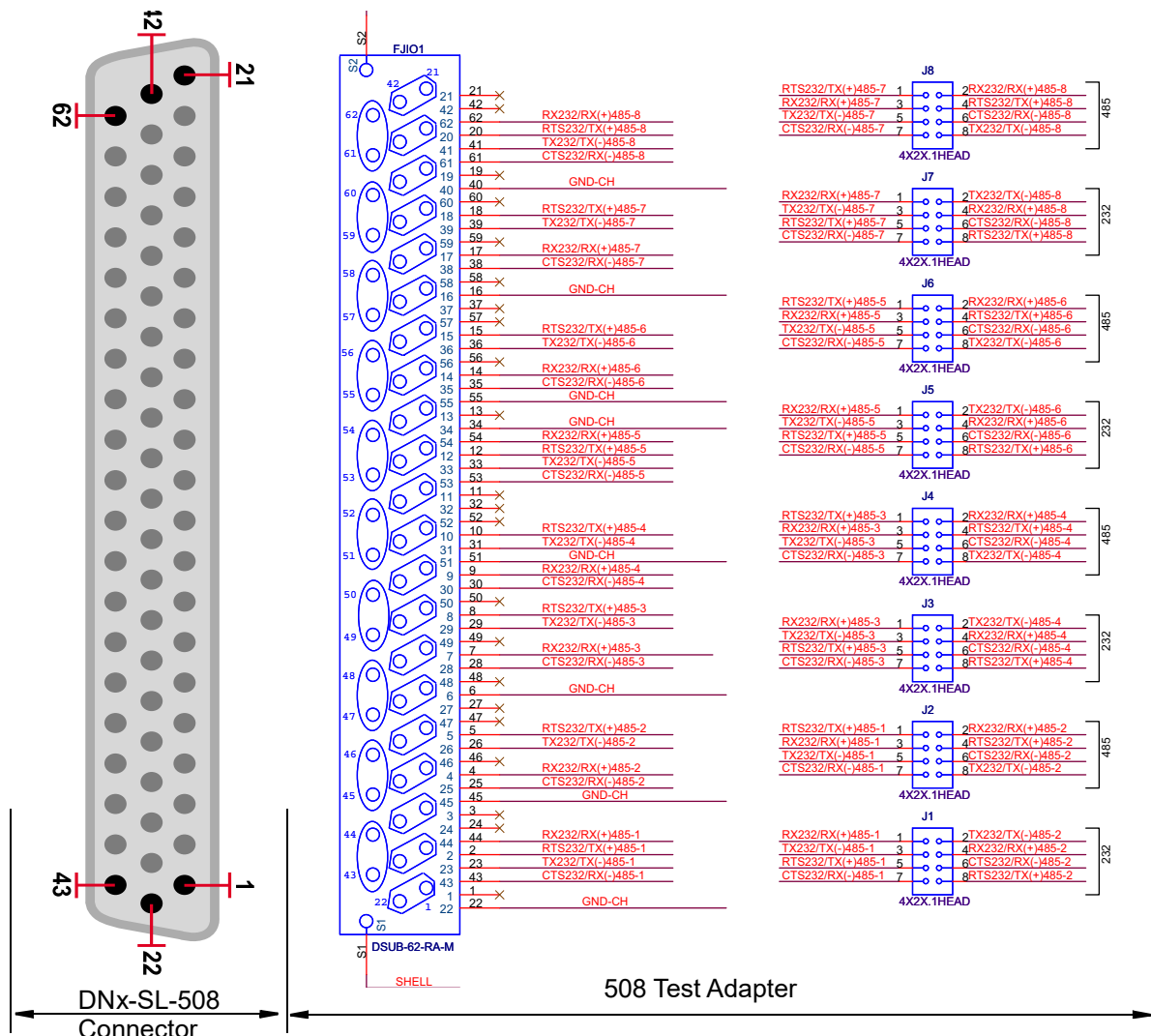


Figure 22-3 Schematic of 508 Test Adapter

22.3 Using the 508 Test Adapter

Testing the DNx-SL-508 Serial Interface Board with the DNx-TADP-508 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-SL-508 User Manual for information about programming the SL-508.



22.4 Specifications Technical specifications for the 508 Test Adapter are listed in **Table 22-1** below.

Table 22-1 Technical Specifications for the 508 Test Adapter

Channel Configurations	
Number of channels	Test Adapter cross-connects each channel to an adjacent channel (4 pairs). Software tests transmission of messages in both directions.
Serial Interfaces	All channels can be jumper-selected as RS-232 or RS-422/485 (all must be selected)
RS-422/485 Modes	Half and full duplex
Baud Rates RS-232 RS-422/485	Standard rates up to 250 kbaud Standard rates up to 1Mbaud as well as 12 kb, 12.5 kb, and 50.0 kb
General Specifications	
Connector	DB-62 male
ESD Protection	15 kV
Power Consumption	Less than 1 W
Operating Temperature	-40°C to +85°C
Operating Humidity	95%, non-condensing



601 Test Adapter

The 601 Test Adapter (p/n DNx-TADP-601) is an accessory designed for testing UEI's DNx-CT-601 Counter/Timer Interface Board.

23.1 General Description

Under software control, the 601 Test Adapter facilitates DC tests on all eight channels of a DNx-CT-601 Counter/Timer Interface Board. The DNx-CT-601 board is designed so that each counter/timer unit can be configured to accept pulse inputs from an external clock or timing device or to output a clock signal. Each CTU can also accept a gate input, which can be used to start/stop a counter/timer and to specify count direction when used with a quadrature encoder input.

The 601 Test Adapter facilitates testing of a CTU by using inputs from other CTUs as clock inputs and gates for controlling start/stop and selection of count direction. Two on-board LEDs indicate the presence of clock outputs on the two groups of gates (GCOM-1 for Channel 0, 1, 2, and 3 and GCOM-2 for Channels 4, 5, 6, and 7).

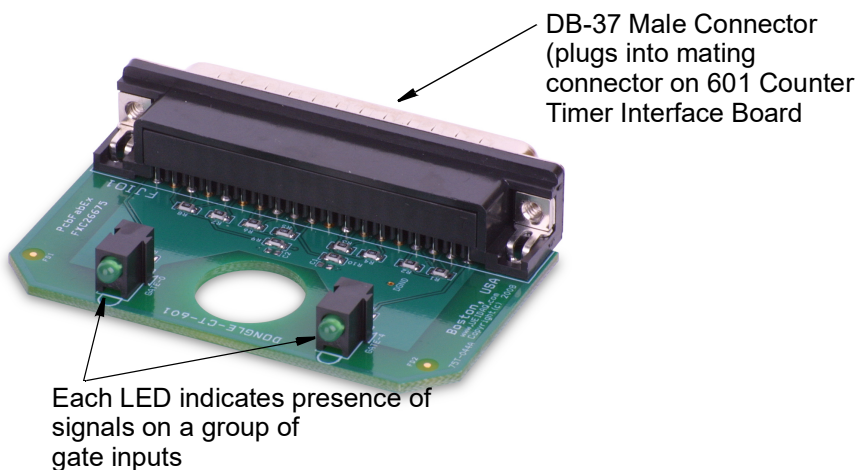


Figure 23-1 Photo of 601 Test Adapter



23.2 Device Architecture

Figure 23-2 shows how CTU outputs and inputs are cross connected in the 601 Test Adapter. For example, testing of CTU1 as a counter uses the output of CTU0 (CT-OUT-0) as a clock input and the output of CTU4 (CT-OUT-4) as its gate input. Similarly, testing of CTU1 as a clock output uses CT-OUT-1 as a pulse input to CTU0 and CT-OUT-4 as the gate input to CTU0.

In this way, performance of each channel in all modes can be tested.

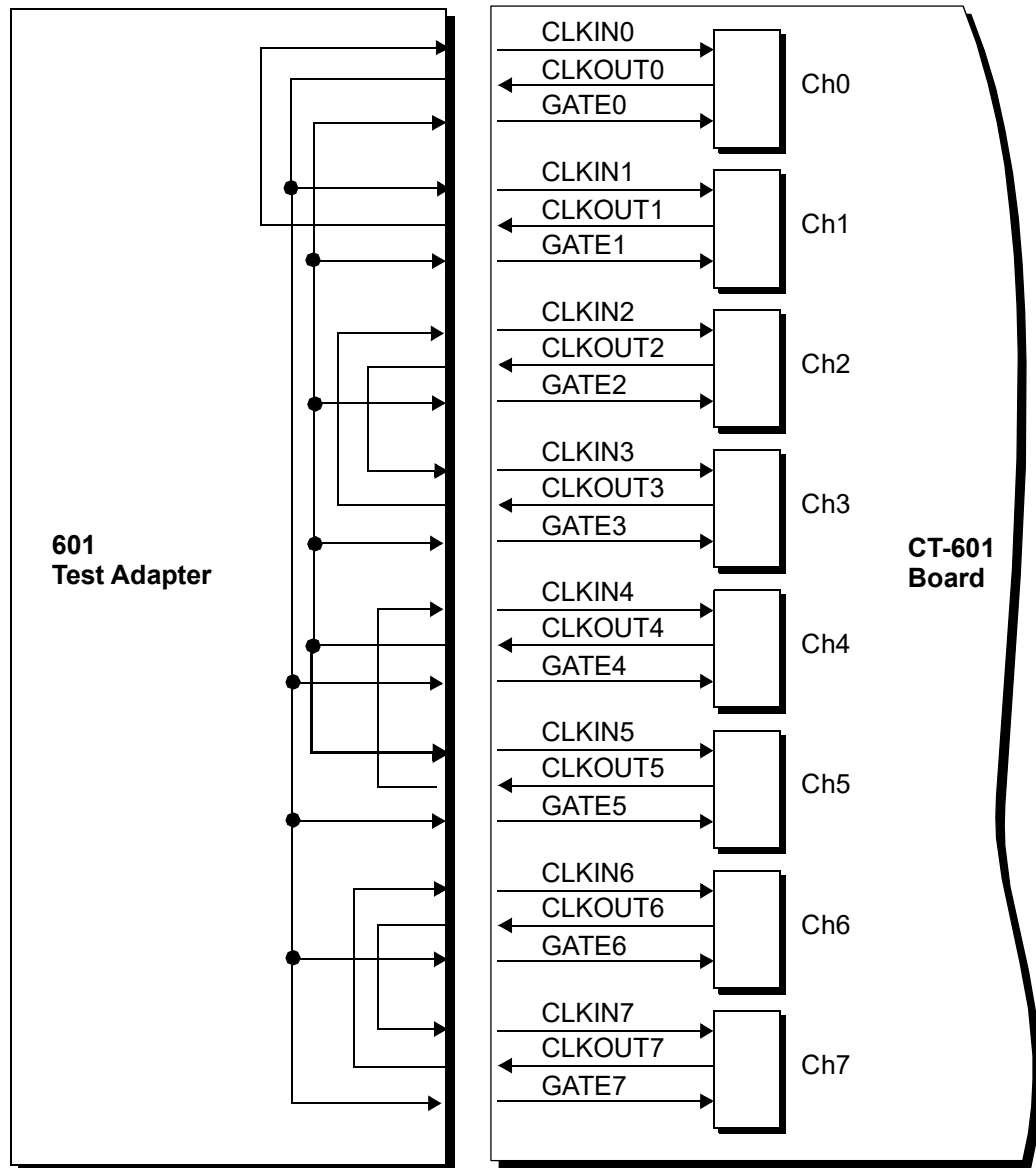


Figure 23-2 Connection Diagram of CT-601 Board and 601 Test Adapter

These cross-connections are listed below in **Table 23-1**.

Table 23-1 Source and Destination of Channel Signals

Signal Source (Output)		Signal Destination (Input)							
	Chn.	Ch 0	Ch 1	Ch 2	Ch 3	Ch 4	Ch 5	Ch 6	Ch 7
CT-OUT	0		IN-1			GATE-4	GATE-5	GATE-6	GATE-7
CT-OUT	1	IN-0							
CT-OUT	2				IN-3				
CT-OUT	3			IN-2					
CT-OUT	4	GATE-0	GATE-1	GATE-2	GATE-3		IN-5		
CT-OUT	5					IN-4			
CT-OUT	6								IN-7
CT-OUT	7							IN-6	

The pinouts of the CT-601 and the 601 Test Adapter are shown in **Figure 23-3**, along with a schematic of the Test Adapter circuit.

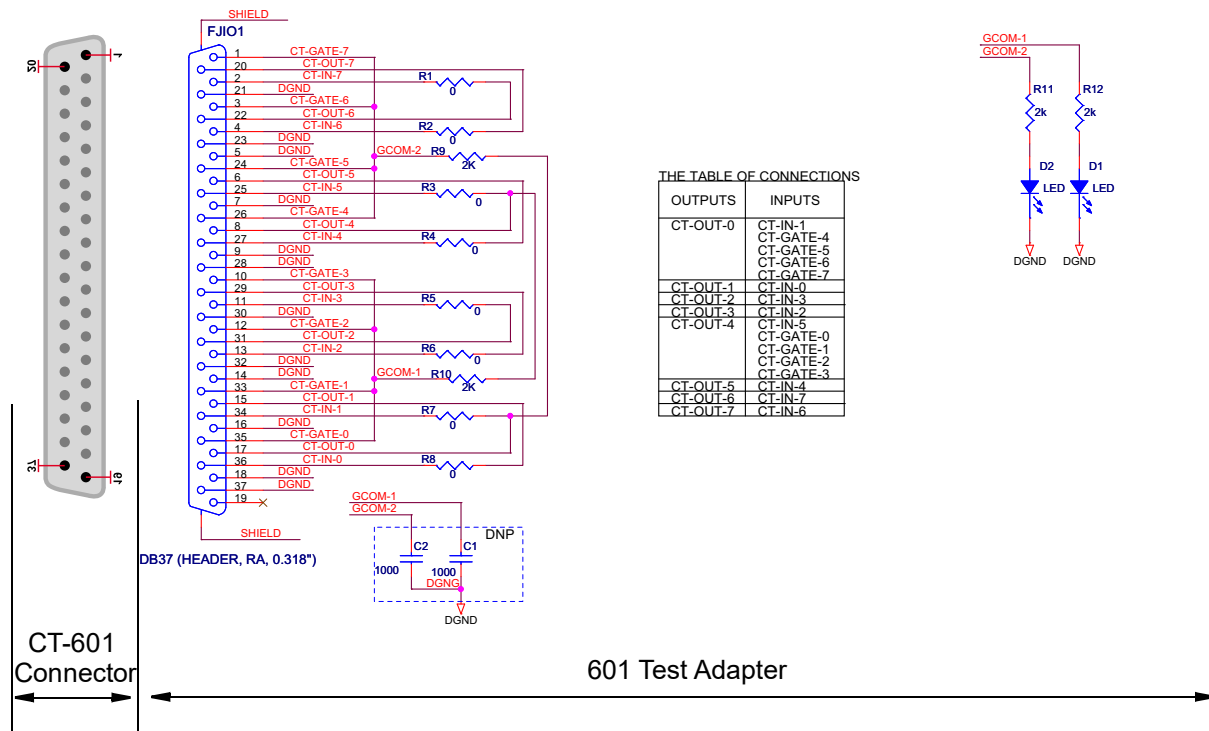


Figure 23-3 Schematic of 601 Test Adapter



23.3 Using the 601 Test Adapter

Testing the DNx-CT-601 Counter/Timer Interface Board with the DNx-TADP-601 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-CT-601 User Manual for information about programming the CT-601.

23.4 Specifications

Technical specifications for the 601 Test Adapter are listed in **Table 23-2** below.

Table 23-2 Technical Specifications for the 601 Test Adapter

Channel Configurations	
Number of channels	8
Maximum input frequency	33 MHz from CT-601 internal input clock
Minimum Input rise/fall time	1 usec
Minimum frequency	no low limits
Minimum pulse width/period	15.15 nsec / 30.30 nsec
Input low voltage	0.0 - 0.8V
Input high voltage	2.0 - 5.0V
Output low voltage	0.0 - 0.8V
Output high voltage	2.0 - 5.0V
General Specifications	
Connector	DB-37 male
Power Consumption	Less than 1 W
Operating Temperature	-40°C to +85°C
Operating Humidity	90%, non-condensing



604 Test Adapter

The 604 Test Adapter (p/n DNx-TADP-604) is an accessory designed for testing UEI's DNx-QUAD-604 Quadrature Encoder Interface Board.

24.1 General Description

Under software control, the 604 Test Adapter facilitates DC tests on all four channels of a DNx-QUAD-604 Quadrature Encoder Interface Board. The DNx-QUAD-604 board is designed to accept standard A, B, and Z (index) inputs from four independent quadrature encoder devices. It also accepts a trigger input and transmits a clock and trigger output for each of the four channels.

The 604 Test Adapter simulates encoder inputs for each channel by using the trigger and clock output signals from another channel as a source. On-board LEDs indicates the presence of clock outputs on channels 0 and 2.

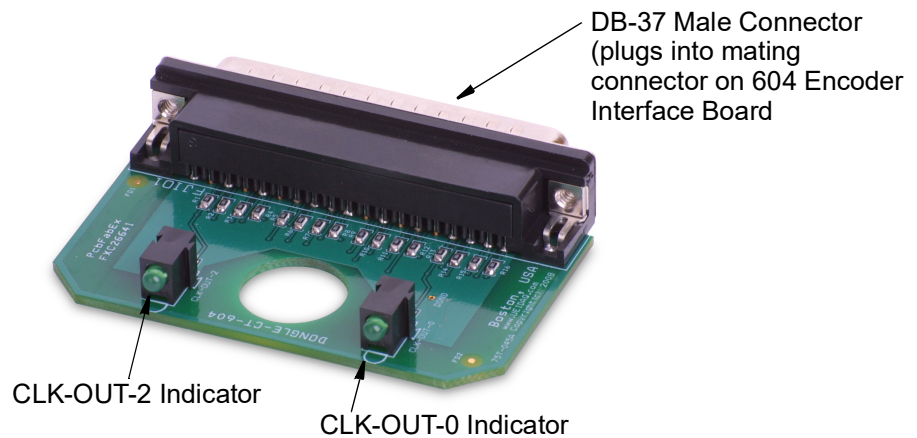


Figure 24-1 Photo of 604 Test Adapter



24.2 Device Architecture

As shown in **Figure 24-2**, the input signals for Channel 0 of the DNx-QUAD-604 board are generated by the trigger and clock outputs of Channels 2 and 3. Signals for other channels are described in **Table 24-1**.

In this way, performance of each channel can be tested by varying the bit rate and phase of each simulated input and output.

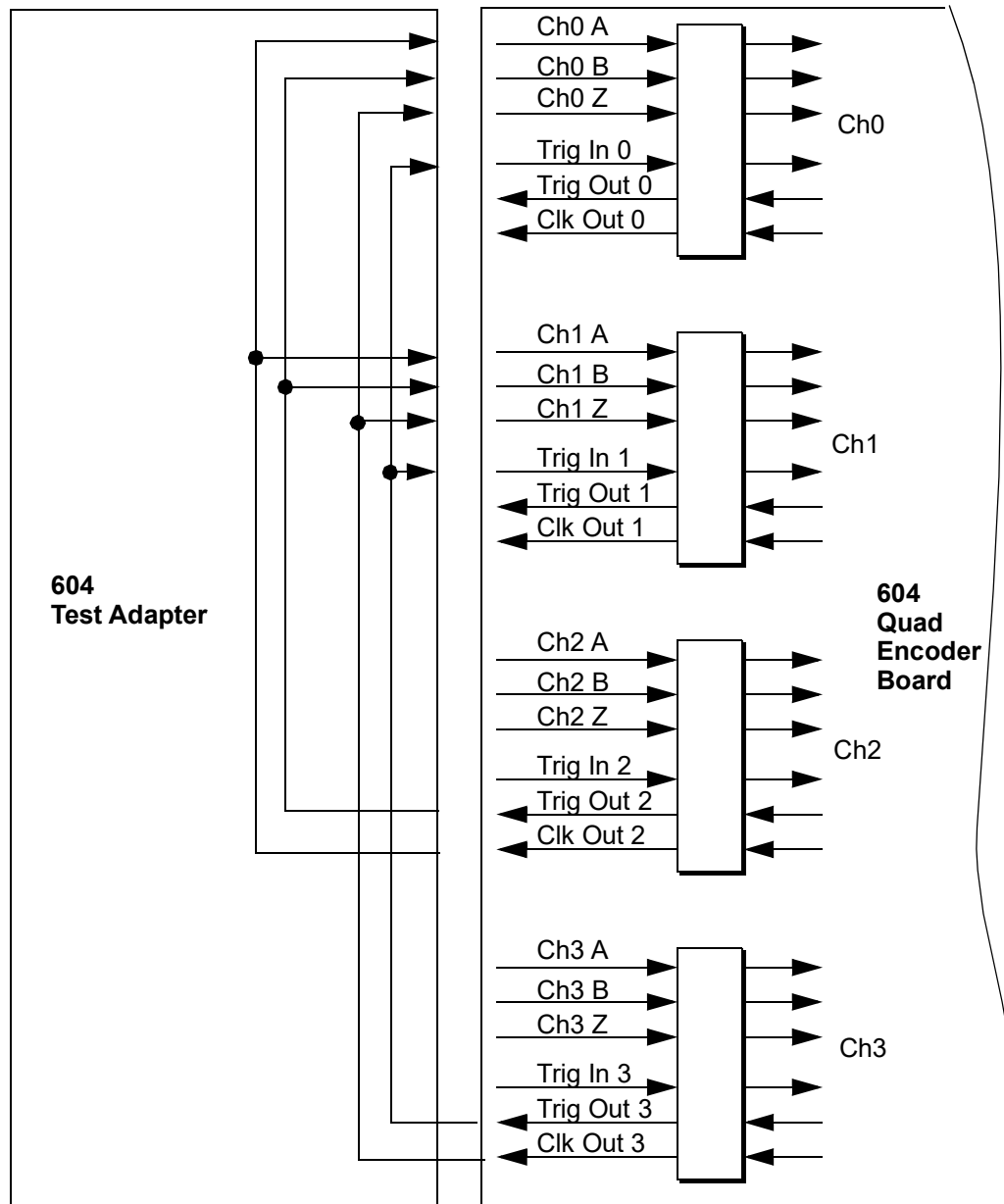


Figure 24-2 Connection Diagram of QUAD-604 and 604 Test Adapter

These cross-connections are listed below in **Table 24-1**.

Table 24-1 Source and Destination of Channel Signals

Signal Source (Output)		Signal Destination (Input)			
	Channel	Ch 0	Ch 1	Ch 2	Ch 3
CLK-OUT-0	0			A	A
TRIG-OUT-0	0			B	B
CLK-OUT-1	1			Z	Z
TRIG-OUT-1	1			TRIG-IN	TRIG-IN
CLK-OUT-2	2	A	A		
TRIG-OUT-2	2	B	B		
CLK-OUT-3	3	Z	Z		
TRIG-OUT-3	3	TRIG-IN	TRIG-IN		

The pinouts of the QUAD-604 and the 604 Test Adapter are shown in **Figure 24-3**, along with a schematic of the Test Adapter circuit.

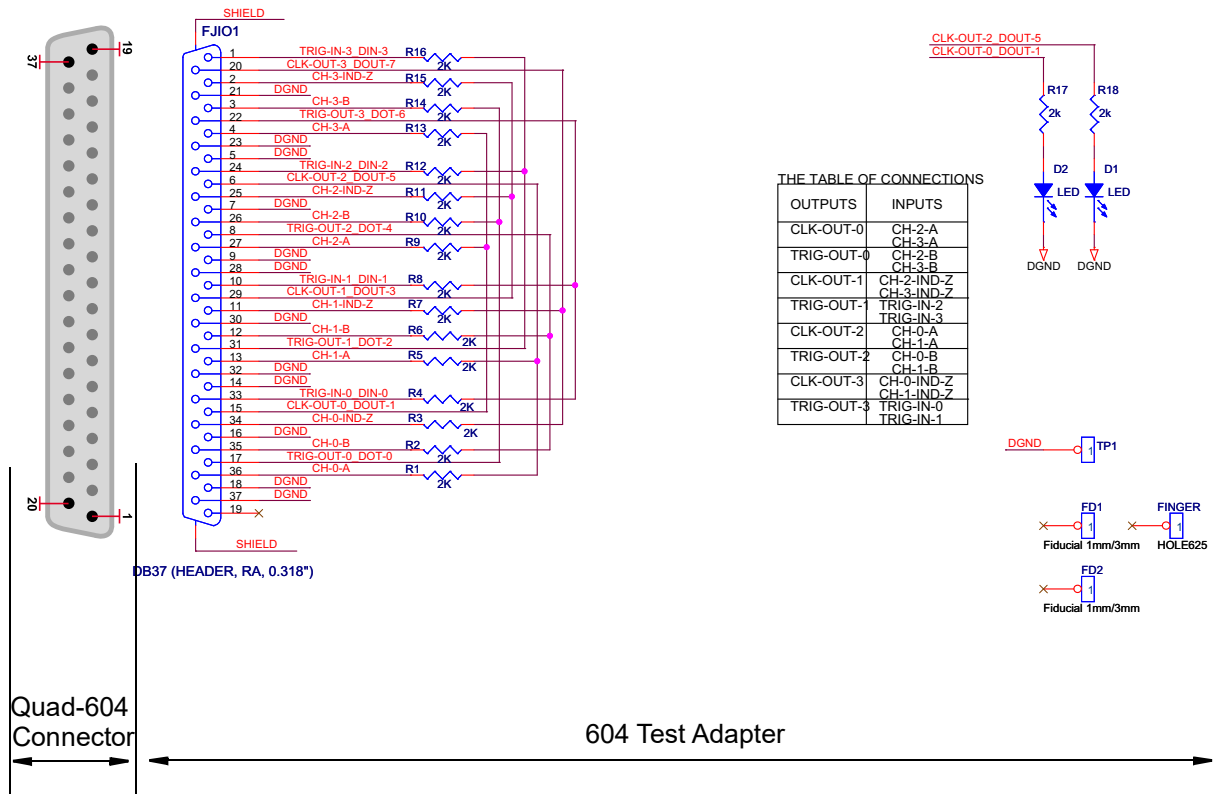


Figure 24-3 Schematic of 604 Test Adapter



24.3 Using the 604 Test Adapter

Testing the DNx-QUAD-604 Quadrature Encoder Interface Board with the DNx-TADP-604 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-QUAD-604 User Manual for information about programming the QUAD-604.

24.4 Specifications

Technical specifications for the 604 Test Adapter are listed in **Table 24-2** below.

Table 24-2 Technical Specifications for the 604 Test Adapter

Channel Configurations	
Number of channels	4
Input encoder modes	x1, x2, x4
Maximum input frequency	16.5 MHz
Minimum Input rise/fall time	1 usec
Minimum frequency	no low limits
Minimum pulse width/period	15.15 nsec / 30.30 nsec
Input low voltage	0.0 - 0.8V
Input high voltage	2.0 - 5.0V
Output low voltage	0.0 - 0.8V
Output high voltage	2.0 - 5.0V at ± 12 mA
General Specifications	
Connector	DB-37 male
Overvoltage protection	-40V to +55V
Power Consumption	Less than 1 W
Operating Temperature	-40°C to +85°C
Operating Humidity	90%, non-condensing



1553 Test Adapter

The 1553 Test Adapter (p/n DNx-TADP-1553) is an accessory designed for testing UEI's DNx-1553-553 MIL-STD-1553 Interface Board.

25.1 General Description

Under software control, the 1553 Test Adapter facilitates loopback tests on both redundant channels of a DNx-1553-553 MIL-STD-1553 Interface Board. The 1553 Test Adapter is designed to receive and loopback MIL-STD 1553 messages over either channel of the 1553 Interface board.

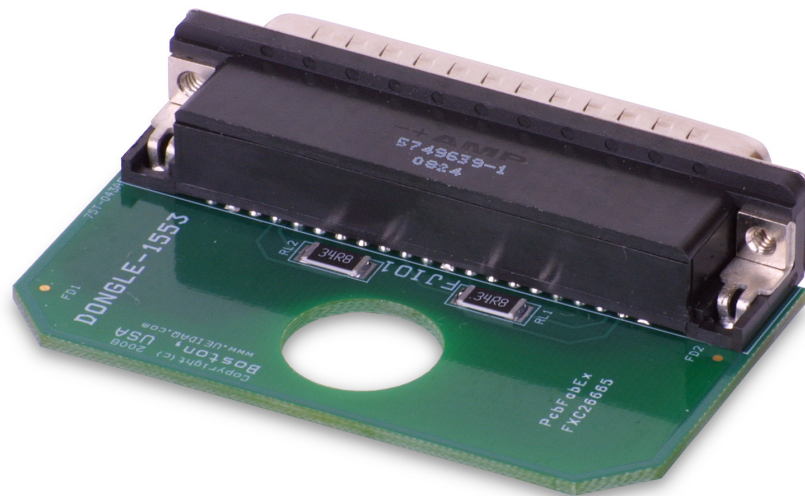


Figure 25-1 Photo of 1553 Test Adapter



As shown in **Figure 25-2**, the 1553 Test Adapter receives an incoming 1553 message on one channel of a 1553 layer and loops the message back on the second channel. A termination resistor connected across the P and N lines of each bus emulates the impedance of the actual bus.

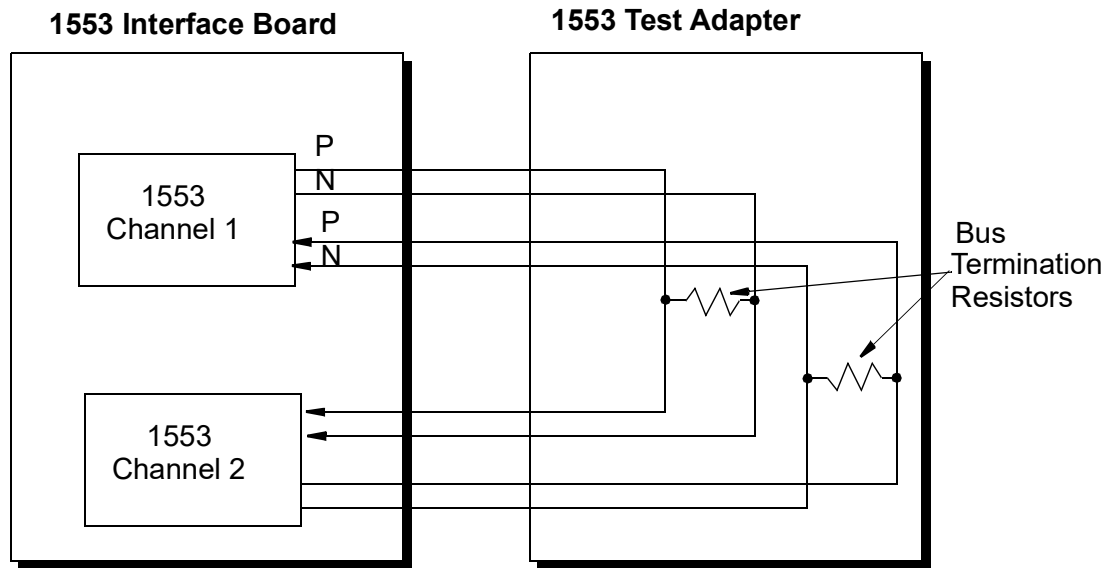


Figure 25-2 Block Diagram of 1553 Test Adapter

The pinouts of the 1553-553 and the 1553 Test Adapter are shown in **Figure 25-3**, along with a schematic of the Test Adapter circuit.

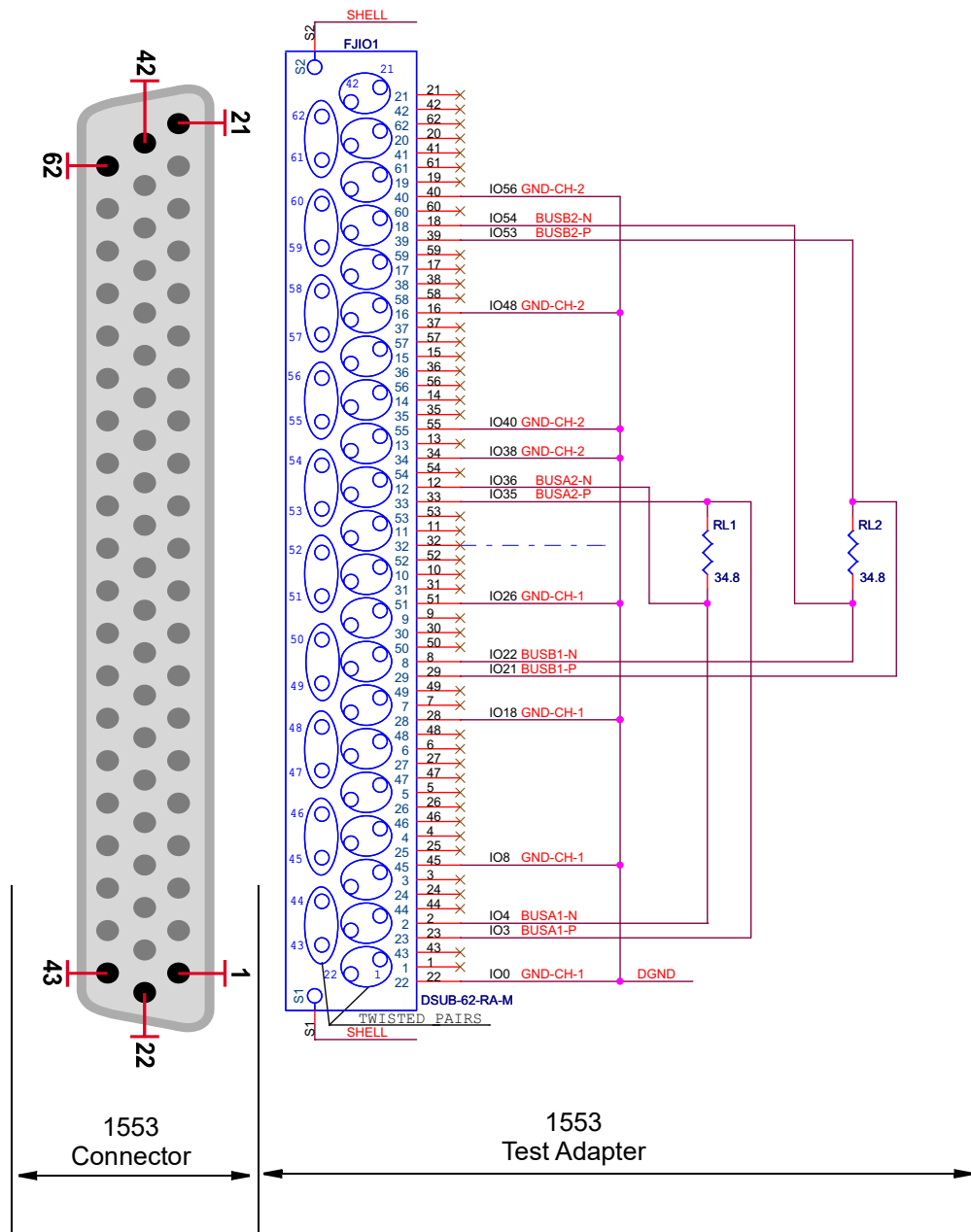


Figure 25-3 Schematic of 1553 Test Adapter

25.2 Using the 1553 Test Adapter

Testing the DNx-1553-553 MIL-STD-1553 Interface Board with the DNx-TADP-1553 requires you to develop a simple program for performing tests of each channel and accumulating/displaying the test results. This can be done by using the sample code provided by UEI as guides and modifying them to fit your specific needs. The code samples are included in the UEI software suite. Please refer to the DNx-1553-553 User Manual for information about programming the 1553-553.



25.3 Specifications Technical specifications for the 1553 Test Adapter are listed in **Table 25-1** below.

Table 25-1 Technical Specifications for the 1553 Test Adapter

Channel Configurations	
Number of channels/ports	2, independent
Channel configuration	Dual redundant interfaces
Specification compliance	MIL-STD-1553a or MIL-STD-1553b, including Notices 1 and 2
General Specifications	
Connector	DB-62 male
Overvoltage protection	-40V to +55V
ESD Protection	15 kV
Power Consumption	Less than 1 W
Operating Temperature	-40°C to +85°C
Operating Humidity	90%, non-condensing

