UEIPAC G6 Intel
Data Acquisition Systems
—
Hardware Manual

October 2025

PN Man-UEIPAC-INTEL-HW

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Chapter 1 Introduction

This document describes hardware features, performance specifications, and operating functions of UEIPAC G6 Intel data acquisition systems.

NOTE: To learn more about UEIPAC G6 Intel software development, configuration, and usage, please refer to the *UEIPAC Intel Software Manual*.

This chapter provides the following information about the UEIPAC G6 Intel systems:

- Organization of This Manual (Section 1.1)
- Product Versions Described in This Manual (Section 1.2)
- UEIPAC Intel Operating Systems (Section 1.3)
- UEIPAC Intel CPU Options (Section 1.4)

1.1 Organization of This Manual

This *UEIPAC G6 Intel Hardware Manual* is organized as follows:

- **Chapter 1 – Introduction**
  This chapter describes the organization of the document and the conventions used throughout the manual.
- **Chapter 2 – UEIPAC Intel Cube Series Chassis**
  This chapter provides an overview of hardware for UEIPAC Intel systems in a Cube chassis.
- **Chapter 3 – UEIPAC Intel RACK Series Chassis**
  This chapter provides an overview of hardware for UEIPAC Intel systems in a RACKtangle and FLATRACK chassis.
- **Chapter 4 – UEIPAC Intel Core CPU / Power Module**
  This chapter summarizes the UEIPAC Intel CPU / Power Core Module.
- **Chapter 5 – Installation and Configuration**
  This chapter summarizes the recommended procedures for installing, configuring, starting up, and troubleshooting a UEIPAC Intel system.
- **Chapter 6 – PowerDNA Explorer**
  This chapter provides a general description of the capabilities of UEI's GUI-based communication application, PowerDNA Explorer, when used with a UEIPAC G6 Intel system.
- **Appendix A – Field Replacement of Fuses**
  This appendix describes procedures for replacing fuses in the field.
- **Index**
  This is an alphabetical listing of topics covered in the manual, identified by page number.

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Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:

Tips are designed to highlight quick ways to get the job done or to reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.

***CAUTION!** advises you of precautions to take to avoid injury, data loss, damage to your boards, or a system crash.*

Text formatted in **bold** typeface generally represents text that should be entered verbatim. For instance, it can represent a filename, as in the following example: "You can instruct users how to run setup using the **setup.exe** executable."

Bold typeface will also represent button names, as in "Click **Scan Network**."

Text formatted in `fixed` typeface generally represents commands, source code, or other text that should be entered verbatim into a file (e.g., source code file, initialization file, etc.), or text to be entered at a command prompt.

Before you begin:

Before plugging any I/O connector into the chassis or board(s), be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

No HOT SWAP

Always turn POWER OFF before performing maintenance on a UEI system. Failure to observe this warning may result in damage to the equipment and possible injury to personnel.

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1.2 Product Versions Described in This Manual

This manual provides information for the UEIPAC G6 Intel.

Where applicable, we highlight differences between earlier generations of UEIPAC CPUs in comparison to the UEIPAC G6 Intel for customers transitioning from earlier generations.

Table 1-1 provides a summary of features for UEIPAC product versions.

Table 1-1 Summary of UEIPAC Product Versions

Item	Summary of Features
UEIPAC PowerPC (UEIPAC -00 / -02 / -03)	• 10/100/1000Base-T Ethernet interface • Freescale MPC8347 PowerPC CPU • 1PPS / IEEE 1588 synchronization support[1] • Optional solid-state hard drives • Up to 256 MB RAM • 32 MB flash memory (-00 / -01/ -02) 128 MB flash memory (-03)
UEIPAC SoloX (G4) (UEIPAC -11 / -12)	• 10/100/1000Base-T Ethernet interface • NXP i.MX6 SoloX Series ARM CPU (Cortex-A9 @ 1 GHz) • 1PPS / IEEE 1588 synchronization support[1] • Optional solid-state hard drives • 1 GB RAM • 8 GB flash memory (& U-boot QSPI flash) • HDMI support (UEIPAC SoloX -12 version only) • Optional GSM / Wireless support
UEIPAC Zynq (G5) (UEIPAC -33 / -34 / -3A)	• 3x 10/100/1000Base-T Ethernet interfaces • Xilinx Zynq UltraScale+ MPSoC (Quad core: Cortex-A53 & Arm Mali GPU) • 1PPS / IEEE 1588 synchronization support[1,2] • 4 GB RAM (-33 and -34 options) 2 GB RAM (-3A option) • 8 GB flash memory (U-boot, FPGA Logic, QSPI flash) • DisplayPort support
UEIPAC Intel (G6) (UEIPAC -40)	• Two independent Gigabit Ethernet ports • 1 USB 3.0 port, 1 USB 2.0 port • Quad-Core Intel x6425RE 64-bit CPU • 1PPS / IEEE 1588 synchronization support[3] • TSN protocol 802.1AS, 802.1Qbv, 802.1Qav, 802.1Qbu[3] (Linux only) • TPM 2.0 security • 8 GB RAM • 32 GB on-board eMMC memory • DisplayPort support

1. 1PPS and IEEE 1588 synchronization support is described in the *PowerDNx 1PPS Sync Interface Manual*.
2. IEEE 1588 PTP is currently only supported on NIC1/eth0 on Zynq
3. Only supported on NIC1

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1.3 UEIPAC Intel Operating Systems

UEIPAC G6 Intel systems provide 64-bit development environments. The systems come pre-configured with either Windows 11 IoT Enterprise or Rocky Linux 9.6.

The UEIPAC G6 Intel can also be ordered with Concurrent Real-Time's RedHawk™ Linux RTOS. RedHawk Linux is ideally suited for applications where precise control and reliable data acquisition are essential. An extensive suite of features is provided to meet the specific requirements of real-time and mission-critical environments. To learn more about RedHawk Linux, visit the RedHawk Linux page on Concurrent Real-Time's website at https://concurrent-rt.com/products/software/redhawk-linux. RedHawk Linux is based on Rocky Linux.

1.4 UEIPAC Intel CPU Options

The UEIPAC G6 Intel is currently available in a single option, the -40. A second generation, designated the -60 series, is being developed with an auxiliary PCIe interface.

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Chapter 2 UEIPAC G6 Intel Cube System

This chapter provides the following information about the Cube chassis and system hardware for the UEIPAC G6 Intel:

- UEIPAC Intel Cube System Overview (Section 2.1)
- Specifications (Section 2.2)
- Key Features (Section 2.3)
- UEIPAC Cube Enclosure (Section 2.4)
- DNA-CPU / Power Module (Section 2.5)
- DNA I/O Boards (Section 2.6)

2.1 UEIPAC Intel Cube System Overview

The UEIPAC G6 Intel Cubes are Gigabit Ethernet-based programmable automation controllers (PACs).

Each UEIPAC G6 Intel Cube houses an embedded data acquisition system in a Cube chassis that can accept a set of user-selected I/O boards:

- UEIPAC-100-1G-40 accepts 1 user-selected I/O board
- UEIPAC-300-1G-40 accepts up to 3 user-selected I/O boards
- UEIPAC-600-1G-40 accepts up to 6 user-selected I/O boards
- UEIPAC-700-1G-40 accepts up to 7 user-selected I/O boards

Standard UEIPAC G6 Intel Cubes are shown in Figure 2-1. Cooling fans are mounted on the rear cover of the cube.

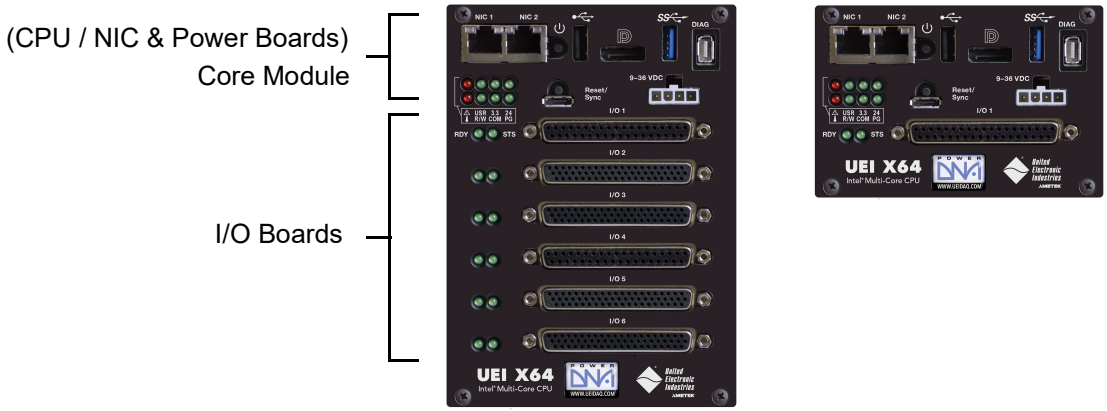

Figure 2-1. UEIPAC-600-1G-40 & UEIPAC-100-1G-40 Systems

NOTE: As an option for rack-mount solutions, up to four Cube systems can be mounted in UEI's DNA-19RACKW accessory assembly.

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2.1.1 UEIPAC Intel Cube Modules

A standard UEIPAC Cube consists of the following modules:

- One Cube enclosure
- One CPU / POWER 2-board module
- Selection of DNA I/O boards
- DNA-IO-FILLER panels (one for each unused I/O slot)
- DNA-PSU-24-100 100 W, 120/230 VAC to +24 VDC external power supply with cable and Molex connector

The CPU board occupies the top portion of the Cube and houses the Intel CPU, Ethernet Network Interface Controllers (NICs), indicator lights, timing/trigger interface, configuration ports, and more. It controls the unit's operations and supervises the activity of the I/O boards.

The remainder of the Cube is dedicated to I/O slots or layers. These slots are populated with the user-selected I/O boards used in your application.

To configure a complete data acquisition system, specify up to 7 DNA I/O boards for installation into your Cube enclosure. I/O boards may be specified in any combination of UEI's DNA I/O boards.

NOTE: For detailed descriptions of all I/O boards and accessories available for the UEIPAC, refer to www.ueidaq.com.

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2.2 Specifications

Table 2-1 and Table 2-2 list the technical specifications for UEIPAC Intel systems. Unless noted, the specifications apply to all UEIPAC Intel types.

Table 2-1 UEIPAC Intel Technical Specifications

Computer Interface	UEIPAC xxx-1G-40 series GigE Cubes
Primary Ethernet Port	Gigabit Ethernet, RJ-45 connector
Secondary Ethernet Port	Gigabit Ethernet, RJ-45 connector
Other Port Functions	Ports may optionally be bonded/teamed
Config/Serial Port	Reserved
Synchronization Options	• DNA-SYNC-1G series cables and boards provide both clock and trigger sync signals. • DNA-IRIG-650 for IRIG and GPS synch. • IEEE 1588 / PTP timing synchronization
I/O Board Support	
Series supported	All DNA-series boards All DNR-series boards (DNF for FLATRACK)
Software / Operating Systems	
Windows	Windows 11 IoT Enterprise
Linux	Rocky Linux 9.6
Dev Languages	C/C++, Python, Visual Studio 2010 to 2022
Dev Environments	Locally on UEIPAC G6 Intel Windows development workstation Linux development workstation
Processor/system	
CPU	Intel x6425RE
Cores/Threads	4/4
Base CPU Frequency	1.9 GHz
Turbo Frequency	2.7 GHz (operating temperature limited)
Memory	
RAM	8 GB
Cache L2	1.5 MB
On-board eMMC	32 GB
M.2 NVMe slot	Supports 2242, 2260, or 2280 sizes Supports industrial pSLC drives up to 320 GB and TLC drives up to 2 TB
Additional Functionality	
DisplayPort	Intel UHD graphics, 400 MHz, 4k@60 fps
USB Ports	1 USB 3.0 1 USB 2.0
TSN Protocol (Linux only)	802.1AS, 802.1Qbv, 802.1Qav, 802.1Qbu
TCC Support (Linux only)	Yes
TPM security support	TPM 2.0
Synchronization/Diagnostic port	Yes
Power Requirements	
Voltage	9-36 VDC (115/220 VAC adaptor included)
Power	20 W at 24 VDC (not including I/O boards)
Power Monitoring	
I/O Board Power	All internal power supplies monitored to ±1% accuracy. All PS voltages may be read by API. LED annunciators indicate out of range
Input Current	Monitored by host, API indicates overcurrent
Input Voltage	Monitored by host, API indicates out of range

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Table 2-2 UEIPAC Intel Physical and Environmental Technical Specifications

Physical Dimensions		
UEIPAC 100-1G	1 I/O Slot Cube	4.1” x 4.0” x 2.7”
UEIPAC 300-1G	3 I/O Slot Cube	4.1” x 5.0” x 4.0”
UEIPAC 400R	4 I/O Slot FLATRACK	1.75” x 7.8” x 16” (Std 1U)
UEIPAC 600-1G	6 I/O Slot Cube	4.1” x 5.0” x 5.8”
UEIPAC 700-1G	7 I/O Slot Cube	4.1” x 5.0” x 6.6”
UEIPAC 1200R	12 I/O Slot RACKtangle	5.25” x 6.2” x 17.5” (Std 3U)
Environmental		
Temperature (operating)		-40 °C to 70 °C
Temperature (storage)		-40 °C to 85 °C
Humidity		0 to 95%, non-condensing
Vibration (pending testing)		
IEC 60068-2-6		10-500 Hz, 3 *g*, Sinusoidal
IEC 60068-2-64		10-500 Hz, 3 *g* (rms), Broadband random
Shock (pending testing)		
IEC 60068-2-27		100 *g*, 3 ms half sine, 18 shocks at 6 orientations 30 *g*, 11 ms half sine, 18 shocks at 6 orientations
MTBF		TBD hours

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2.3 Key Features

Table 2-3 lists the key features of the UEIPAC Intel.

Table 2-3 UEIPAC Intel Key Features

Extended Features	**Flexible Connectivity**
Rocky Linux 9.6	Dual Gigabit Ethernet ports with TSN support
Win11 IoT Enterprise	USB 3.0 and USB 2.0 ports
DisplayPort video	**Compact Size and High Channel Density**
Over 70 different I/O boards available	Analog Inputs: up to 175/300 channels per Cube/RACK
Built-in signal conditioning	ICP/IEPE: up to 28/48 channels per Cube/RACK
M.2 PCIe slot	Analog Outputs: up to 224/384 channels per Cube/ RACK
Flange kit for mounting to wall/flat surface	Digital I/O: up to 336/576 DIO per Cube/RACK
DIN rail and Rack Mount kits	ARINC 429: up to 112/192 channels per Cube/RACK
Standard “Off-the-shelf” products and delivery	Counter/Timer: up to 56/96 counter channels per Cube /RACK
Cybersecurity	CAN bus: up to 28/48 ports per Cube/RACK
NIST 800-213	RVDT/LVDT: up to 28/48 channels per Cube/RACK
TPM 2.0	RS-232/422/485: up to 56/96 ports per Cube/RACK
Rugged and Industrial[1]	Synchro: up to 28/48 channels per Cube/RACK
RACKS and GigE Cubes operation tested from -40 °C to70 °C	MIL-1553: up to 14/24 redundant ports per Cube/RACK
RACKs and GigE Cubes vibration tested to 3 g	
Shock tested to 100 g (operating)	

1. Vibration and shock testing are planned but have not been performed at the time this user manual was released.

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2.4 UEIPAC Cube Enclosure

The UEIPAC -40, Cube enclosures are rigid, extruded aluminum, mechanical structures with complete EMI shielding. Unused slots are filled with blank filler panels.

The UEIPAC Intel Cube enclosure houses the following components:

- One DNA-CPU and POWER module:
  - a DNA-CPU-INTEL CPU board (slot 1)
  - a DNA-POWER-1GB DC/DC power board (slot 2)
- DNA Cube-based IO boards (slot 3 up to slot 9, where the number of supported boards depends on the product version)
- Blank filler panels for unused slots
- A 24 V fan mounted on the rear cover of the cube that is connected to the DNA-CPU-INTEL CPU board
  - UEIPAC-600-1G-40 and UEIPAC-700-1G-40 Cubes have an additional 12 V fan located below the 24 V fan. The 12 V fan is connected to the DNA-POWER-1GB board.

Behind the faceplate, the Power/CPU/IO board stack is positioned in the cube chassis on grooved guides.

The DC power module provides output voltages of 24, 3.3, 2.5, 1.5, and 1.2 VDC for the logic / CPU and 12 VDC to power the lower fan (if present).

2.4.1 Fans & Air Flow

Air is drawn into the rear of the enclosure, routed forward over the electronic circuit boards, up to the top of the enclosure, and then out the top rear of the enclosure. The system is designed to maintain positive pressure cooling within the enclosure at all times.

A temperature sensor mounted on the POWER board above the CPU monitors temperature within the cube. The system turns on the fan(s) if the temperature exceeds 45°C and shuts down power to the cube if a high limit is exceeded.

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2.5 DNA-CPU / Power Module

UEI offers the DNA-CPU-1G-40 option for the UEIPAC Intel CPU/Power Module. This includes the CPU module (DNA-CPU-INTEL) and POWER board.

Please refer to **Chapter 4** for detailed descriptions of the CPU / POWER module's boards, components, and capabilities. Section 4.2.7 on page 32 provides information on system power control and monitoring.

Note that the CPU / POWER module is a two-board module. One board is dedicated to CPU functions (DNA-CPU-INTEL). The second board is dedicated to power management (DNA-POWER-1GB).

For UEIPAC products in a Cube chassis, all power management and monitoring is provided by the DNA-POWER-1GB board.

The key power capabilities are:

- Input power — 9-36 VDC 80 W maximum, protected by resettable fuses and EMI chokes
- Output power sources (all with greater than 90% efficiency)
  - 24 V, 1 A (24 W)
  - 3.3 V, 5 A (16.5 W, including the 2.5 V derived voltage)
  - 2.5 V, 3 A (derived from 3.3 V source)
  - 1.5 V, 5 A, (7.5 W, including the 1.2 V derived voltage)
  - 24 V, 0.5 A (4 W) for upper fan
  - 12 V, 0.5 A (4 W) for lower fan (UEIPAC-600-1G-40 and UEIPAC-700-1G-40 Cubes)
- DC/DC for 24 V, 3.3 V, and 1.5 V are synchronized from the single spread- spectrum clock source in the DNA-POWER-1GB for low EMI noise level
- Fan control (Forced ON) and status ON/OFF
- Monitoring and LED indicators (1% accuracy, 0.25 Hz update rate) for the following:
  - All output voltages
  - Input current for the 9-36 VDC for the cube housing
  - All voltages from the NIC/Power Module (24 V, 3.3 V, 2.5 V)
  - Temperature of the cube housing and boards
- Provides 9-36 VDC for all modules from an external power source

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2.6 DNA I/O Boards

All standard UEI I/O boards are available for cube-based UEIPAC G6 Intel systems:

- Cube-based UEIPAC XXX-1G systems use a DNA- prefix, (e.g., DNA-AI-207)
- RACK-based UEIPAC 1200R systems use a DNR- prefix, (e.g., DNR-AI-207)
- FLATRACK-based UEIPAC 400R systems use a DNF- prefix, (e.g., DNF-AI-207)

These boards are electronically identical. The only difference between DNA-, DNR-, and DNF- IO boards is the physical mounting arrangement for installation in the different chassis types.

I/O boards are populated into your chassis in the order you specify.

NOTE: Refer to the IO board datasheets and user manuals for detailed electrical specifications, board descriptions, and user instructions. These documents are available on the UEI website at www.ueidaq.com.

No HOT SWAPPING

Always turn POWER OFF before performing maintenance on a UEI system. Failure to observe this warning may result in damage to the equipment and possible injury to personnel.

NOTE: Refer to Section 5.8 on page 47 for IO board removal and replacement instructions.

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Chapter 3 UEIPAC G6 Intel RACK System

This chapter provides the following information about the RACK chassis and system hardware for the UEIPAC G6 Intel:

- UEIPAC Intel RACK System Overview (Section 3.1)
- Specifications (Section 3.2)
- Key Features (Section 3.3)
- UEIPAC RACK Enclosures (Section 3.4)
- UEIPAC RACK-based Modules (Section 3.5)
- DNR- / DNF- CPU / POWER Module(s) (Section 3.6)
- DNR- / DNF-POWER Modules (Section 3.6.1)
- I/O Boards (Section 3.7)

3.1 UEIPAC Intel RACK System Overview

UEIPAC Intel systems in a RACKtangle™ or FLATRACK chassis are rack-mounted versions of the UEIPAC Intel Cube-based data acquisition systems:

- UEIPAC 1200R: accepts up to 12 user-selected I/O boards (RACKtangle, pictured in Figure 3-1)
- UEIPAC 400R: accepts up to 4 user-selected I/O boards (FLATRACK, Figure 3-2)

The UEIPAC Intel systems that are RACK-based house an embedded data acquisition system in a rack enclosure with cabling, installation hardware, LEDs, and a power switch accessible from the front of the rack chassis. Multiple systems may be mounted in a single rack.

All standard DNA- Cube I/O boards are also available in DNR- versions for use in RACKtangle systems or DNF- versions for use in FLATRACK systems.

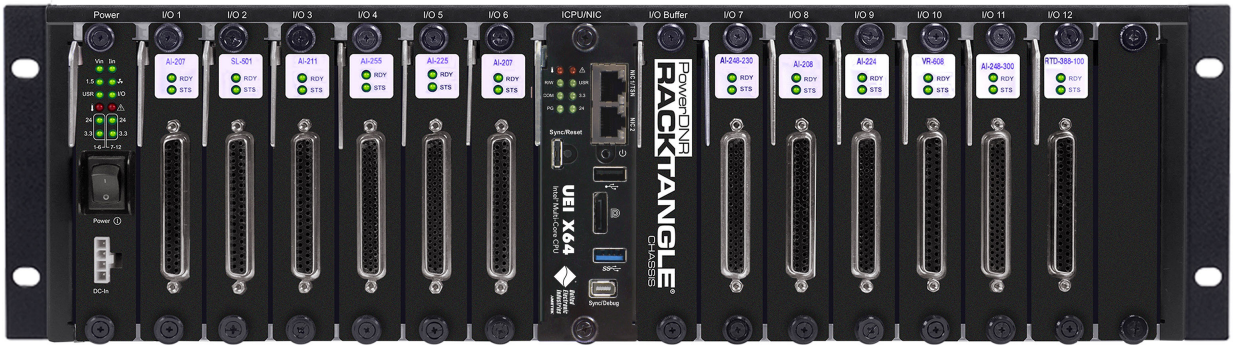

Figure 3-1. Typical UEIPAC 1200R RACKtangle System (Intel)

Figure 3-2. Typical UEIPAC 400R FLATRACK System

3.1.1 UEIPAC Intel RACK Modules

A standard UEIPAC Intel system in a RACK chassis consists of the following modules:

- One RACKtangle or FLATRACK enclosure
- One DNR-CPU-1G / POWER module
- One DNR-POWER-DC Power Module
  (DNF-POWER-DC or DNF-POWER-AC are available for the FLATRACK chassis)
- Your selection of I/O boards
- One DNR-BUFFER Board Module with fan for additional cooling (only used with UEIPAC 1200R RACKtangle chassis)
- Optional IO-FILLER panels (one for each unused I/O slot)
  Note: Slot covers are optional and not included in the price of the rack
- DNA-PSU-180 180-Watt, 120/230 VAC to +24 VDC External Power Supply (one for each enclosure) with cable and Molex connector for plug-in to the POWER-DC module

The CPU module houses the Intel CPU, Ethernet Network Interface Controllers (NICs), indicator lights, timing/trigger interface, configuration ports, and more. It controls the unit's operations, as well as supervising the activity of the I/O boards.

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To configure a complete data acquisition system, specify any combination of UEI's I/O boards:

- UEIPAC 400R: up to 4 DNF I/O boards for installation into a FLATRACK enclosure (see Figure 3-2)
- UEIPAC 1200R: up to 12 DNR I/O boards for installation into a RACKtangle enclosure

NOTE: For detailed descriptions of all I/O boards and accessories available for the UEIPAC G6 Intel, refer to www.ueidaq.com.

3.2 Specifications

Refer to Section 2.2 on page 7 for a table of UEIPAC Intel specifications for both Cube- and RACK-based systems.

3.3 Key Features

Refer to Section 2.3 on page 9 for a table of UEIPAC Intel key features for both Cube- and RACK-based systems.

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3.4 UEIPAC RACK Enclosures

The RACK enclosures are rigid mechanical structures with complete EMI shielding (see **Figure 3-3** and **Figure 3-4**). Unused slots can be filled with filler panels (filler panel diagram shown in **Figure 3-7**).

3.4.1 UEIPAC 1200R Enclosure

The exploded view of a UEIPAC 1200R RACKtangle enclosure is shown in Figure 3-3. The corresponding parts list is shown in Table 3-1.

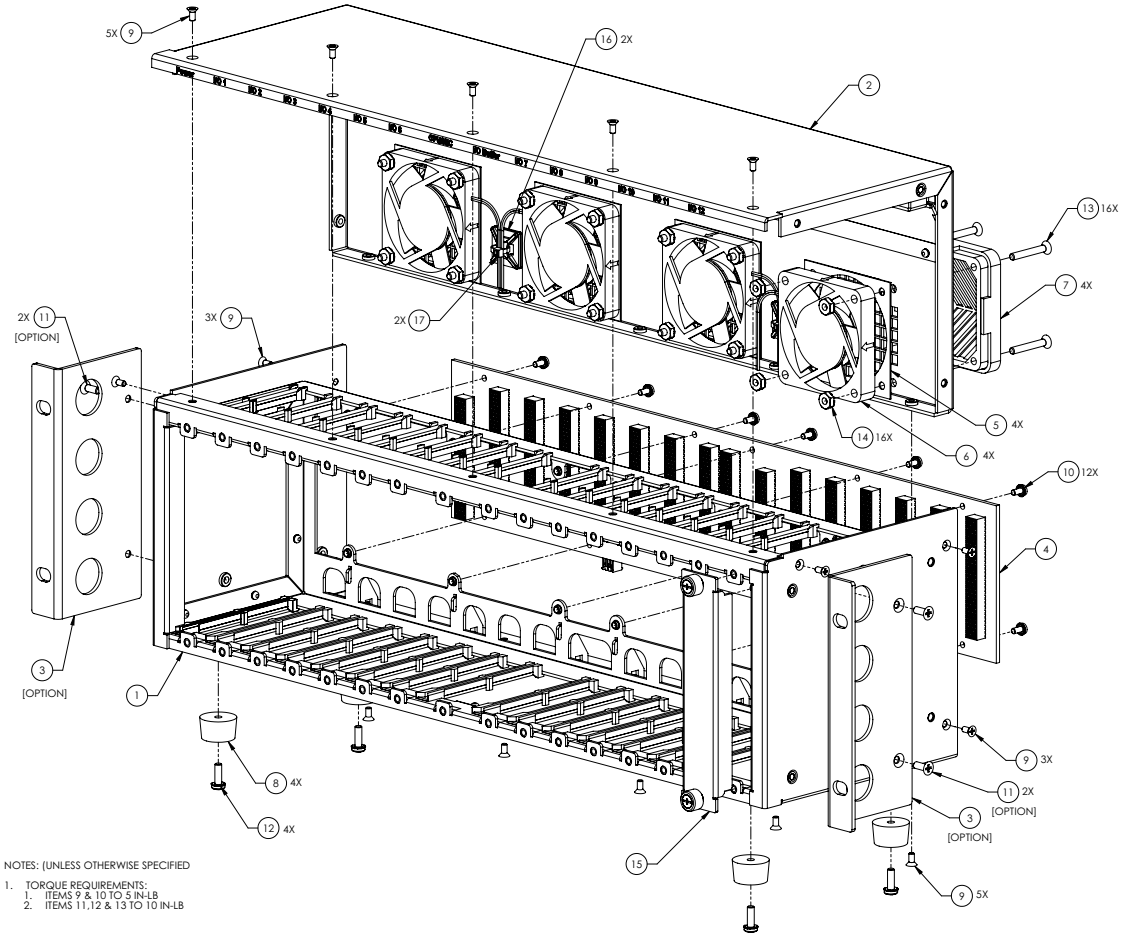

Figure 3-3. Typical RACKtangle Enclosure (Exploded View)

NOTE: The rightmost module (I/O board slot 12) is 2-slots wide (to accommodate future designs and/or custom modules). The enclosure has reversible mounting flanges designed for rack or surface mounting. Rubber feet are supplied for desktop or tabletop mounting. Refer to Section 5.4 on page 45 for more information about mounting options and field connections.

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Table 3-1 UEIPAC 1200R RACKtangle Enclosure Part List (Refer to Figure 3-3)

Item No.	Quantity	Description
1	1	Enclosure, UEIPAC 1200R 2000-241A
2	1	Rear Panel, UEIPAC 1200R 2000-242A
3	2	Bracket, MOUNTING, STEEL, DNR-12 2000-0033 X
4	1	Assembly, PCB, BACKPLANE, DNR-12 DNR-12BP
5	4	Spacer, FAN, 60MM 2004-6060
6	4	Fan, AXIAL, 60x10mm, 12VDC . DNR-FAN
7	4	Filter Assembly, 60mm, 45PPI 806-5023
8	4	Bumper, RECESSED, 3/4DIA, 7/16H 1000-728
9	16	Screw, #4-40x¼,82° FH,PHIL,SST,BLK OXIDE 1001-082
10	12	Screw, #4-40x.250,PAN HD,PH,SEMS,SQ CONE 1001-028
11	4	Screw, #6-32x.375,100D FH,PHIL,SST,BLK OXIDE 1001-375 X
12	4	Screw, #6-32x.437,PAN HD,PHIL,SEMS,EXT 1001-437
13	16	Screw, #6-32x1.00,82° FH,PHIL 1001-635
14	16	Nut, HEX, KEPS, #6-32 1001-634
15	1	IO Filler, DNR-12 2000-0101
16	2	Mount, CABLE TIE 1000-214
17	2	Cable Tie 1000-213

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3.4.2 UEIPAC 400R Enclosure

The exploded view of a UEIPAC 400R FLATRACK system is shown in Figure 3-4. The corresponding parts list is shown in Table 3-2.

The UEIPAC Intel FLATRACK is available in AC or DC powered versions. The DC version requires a DC power source between 9 and 36 volts. The AC unit operates from 100 to 240 VAC, from 50 to 60 Hz. The power module provides output voltages of 24, 3.3, 2.5, 1.5, and 1.2 VDC for the logic/CPU and 8 VDC to power three cooling fans.

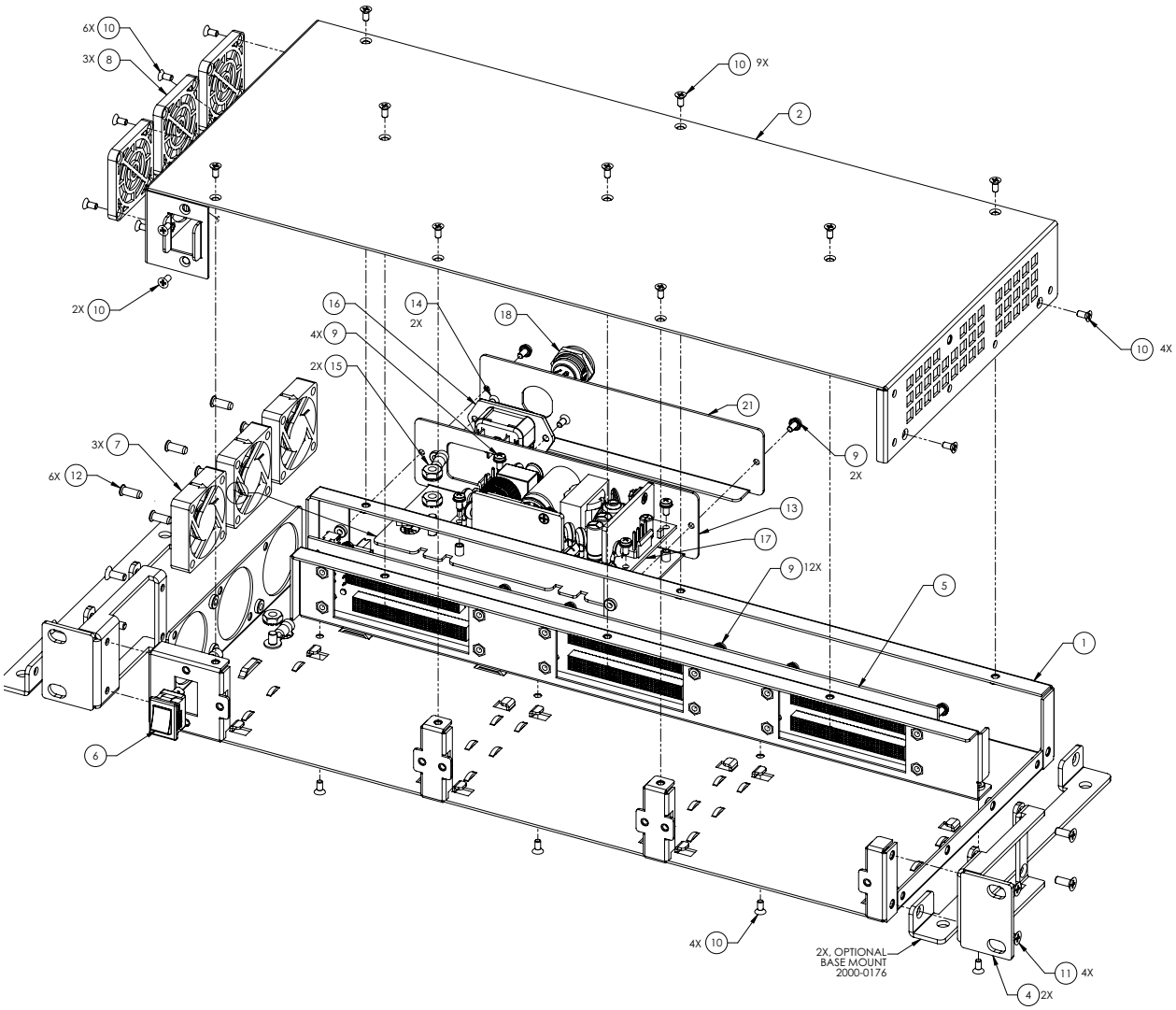

Figure 3-4. Typical FLATRACK Enclosure (Exploded View)

Table 3-2 UEIPAC 400R FLATRACK Enclosure Parts List (Refer to Figure 3-4)

Item No.	UEIPAC 400R-AC Quantity	UEIPAC 400R-DC Quantity	Description (Vendor/Vendor Part No.)
1	1	1	Chassis, UEIPAC 400R Base
2	1	1	Chassis, UEIPAC 400R Cover
3	1	1	Support, UEIPAC 400R Backplane
4	2	2	Bracket, Mounting, 19" RACK, DNF-4-1G
5	1	1	Backplane Assembly, PCB, DNFBP4-RA DNFBP4-RA
6	1	1	Power Switch, Rocker, SNAP-IN, 2A 250VAC ITT DA102J12S215PQF
7	3	3	Fan, Axial, 40x10mm
8	3	3	Filter Assembly, 40MM FAN QUALTEK 09150-F/30PPI
9	18	14	Screw, #4-40x.250, PAN HD, PH, SEMS, SQ CONE 1001-028
10	25	25	Screw, #4-40x¼,82° FH,PHIL,SST,BLK OXIDE 1001-082
11	8	8	Screw, #6-32x.375,100D FH,PHIL,SST,BLK OXIDE 1001-375
12	6	6	Screw, M3.9x1.2 x 10.5mm, FH, PHIL, FAN MOUNT PENCOM M3.9 X 10.5mmPHFL-FAN-NI
13	1	NA	Plate, Mounting, CUI POWER SUPPLY 2000-0178
14	2	NA	Screw, Oval Head, #4-40 X .250, SLT/Z MCMASTERCARR 91802A106
15	3	NA	Nut, Hex, KEPS, #8-32
16	1	NA	Connector, AC Inlet, IEC 320 SCHURTER 6100-3300
17	1	NA	Power Supply, 60W, 24VDC, 2"X4" CUI INC VMS-60-24
18	NA	1	Connector, RCPT, MINI CIRC DIN, 4P CUI SD-40LS
21	NA	1	Plate, Mounting, CUI POWER SUPPLY 2000-0184

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3.5 UEIPAC RACK-based Modules

Typical UEIPAC RACK-based modules are shown in Figure 3-5 and Figure 3-6 and described in Table 3-3.

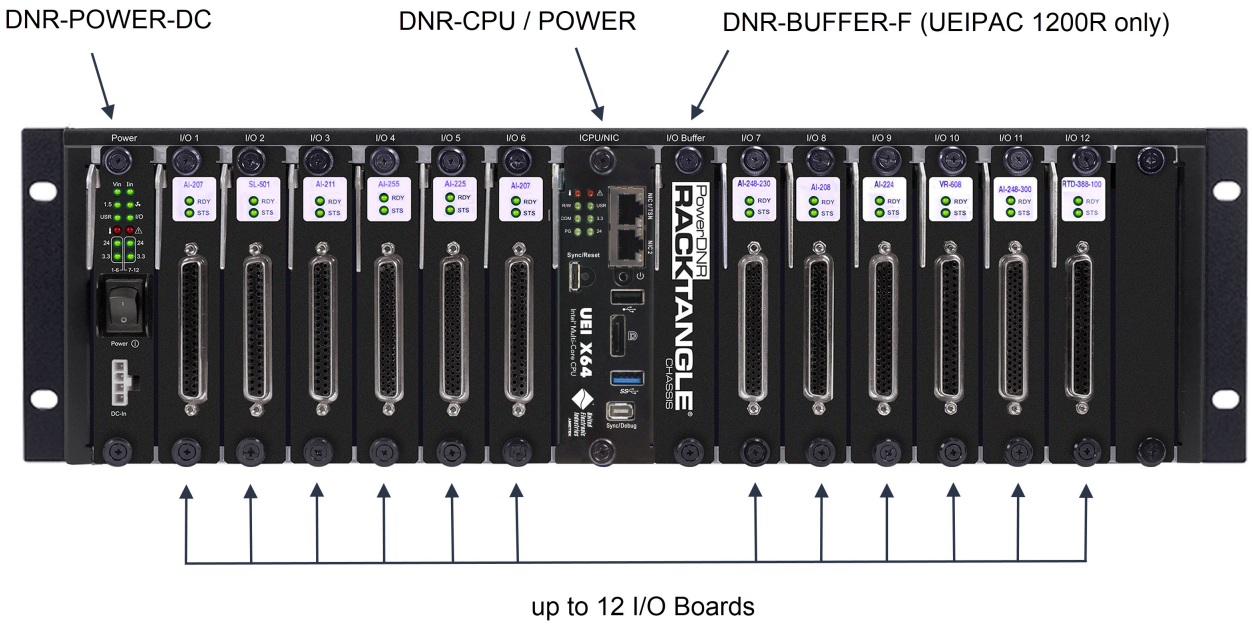

Figure 3-5. Typical UEIPAC 1200R Board Placement

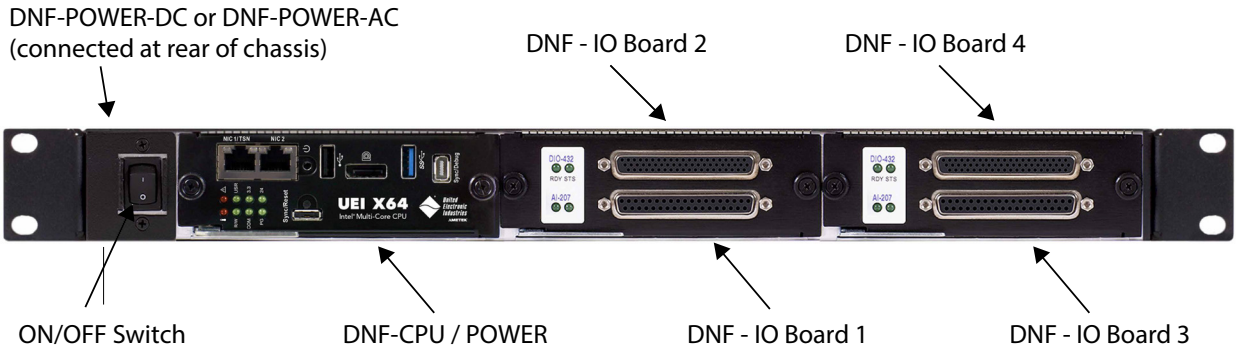

Figure 3-6. Typical UEIPAC 400R Board Placement

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Table 3-3 Modules in UEIPAC Intel RACK-based Enclosure

Item	Part No.	Description
Power board	DNR-POWER-DC DNF-POWER-DC or DNF-POWER-AC	**UEIPAC**: Isolated DC/DC Power Module/Power Monitor with status indicators, a local on/off switch, and 4-pin Molex Power-In connector. (Refer to Section 3.6.1) **UEIPAC 400R-DC**: Mounting plate & connecting hardware or **UEIPAC 400R-AC**: Mounting plate, connecting hardware, and 9-36 VDC power supply for use with -AC
CPU / POWER module	DNF-CPU-1G-40 DNR-CPU-1G-40	One dual-slot CPU / POWER module DNF - denotes UEIPAC 400R FLATRACK chassis DNR - denotes UEIPAC 1200R RACKtangle chassis HalfRACK chassis (Refer to **Chapter 4** for detailed information)
Buffer module	DNR-BUFFER-F (RACKtangle only)	**UEIPAC 1200R:** One for buffering address/control/clock lines (not currently addressable). (Refer to Section 3.5.1). This module includes a fan located directly over the Intel processor to allow for optimal cooling. **Not applicable for UEIPAC 400R**
I/O boards	DNR- / DNF-	RACK I/O boards designed for front removal and installation. (Refer to Section 3.7)
Enclosure	DNF-4-ENCL	One backplane/assembly with temperature sensors (see Section 3.4 for diagrams)
Filler panels	DNR-IO-FILLER DNF-IO-FILLER	Blank filler panels for all unused slots (Note that this item is optional / not included in price of rack)
Fans		8-volt cooling fans mounted in enclosure (Refer to Section 3.4)

3.5.1 DNR-BUFFER-F Module

The UEIPAC 1200R includes a DNR-BUFFER-F module which provides buffering between the CPU and I/O board address/control/clock lines for 12-board RACKtangle systems. This buffer module also includes an additional fan to assist with cooling the Intel processor.

Refer to Figure 3-5 on page 20 for location of buffer board in the RACKtangle chassis.

3.5.2 DNR-IO-FILLER & DNR-BRACKET

The following section provides drawings for the DNR-IO-FILLER (Figure 3-7) and DNR-BRACKET (Figure 3-8).

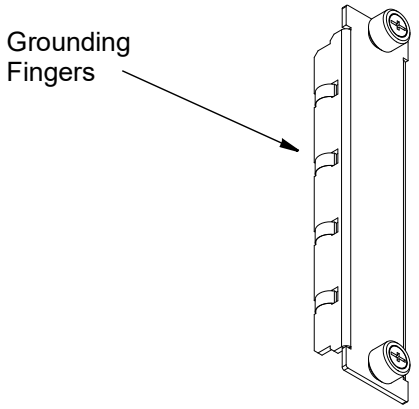

Figure 3-7. Optional DNR-IO-Filler Panel for Empty Slots

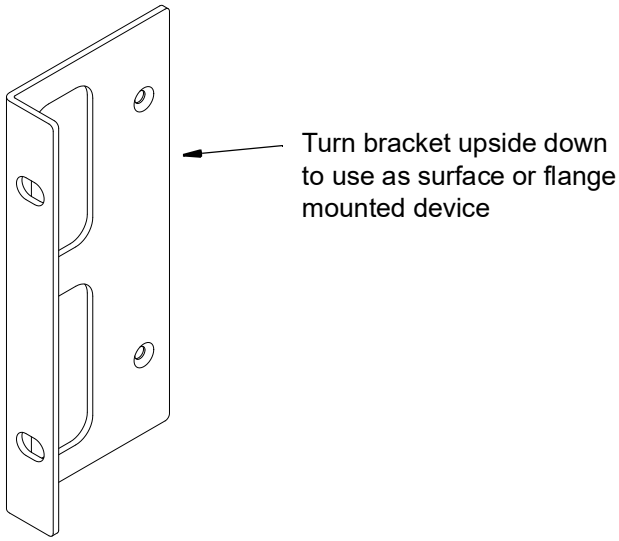

Figure 3-8. DNR-BRACKET Reversible Mounting Bracket

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3.5.3 RACK Air Flow

As shown **Figure 3-9**, cooling air is drawn into the rear of the enclosure via fans, routed forward over the electronic circuit boards, up to the top of the enclosure, and then out the top rear of the enclosure. The system is designed to maintain positive pressure cooling within the enclosure at all times.

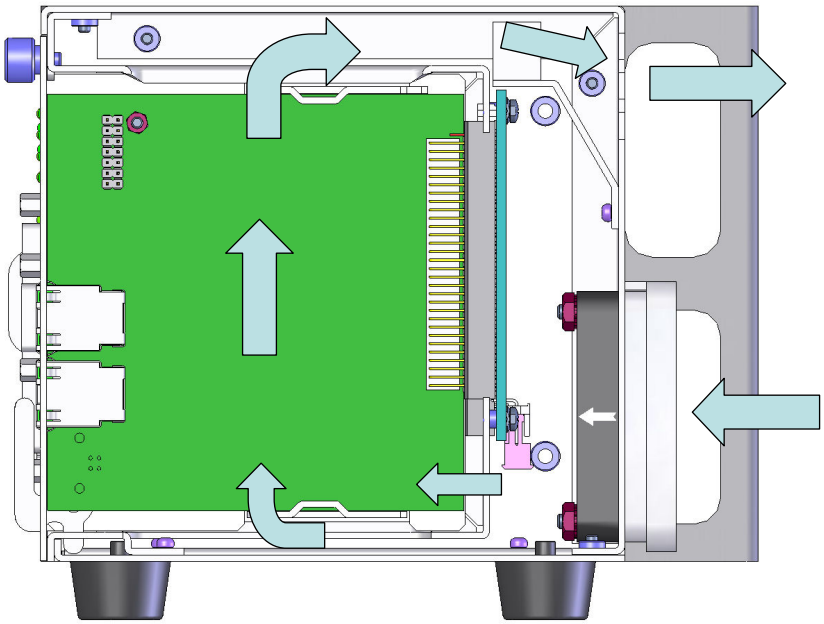

Figure 3-9. Example of UEIPAC 1200R RACKtangle Air Flow

Two sensors mounted on the backplane over the Power Module and over the CPU board continuously monitor internal temperatures, turning fans on if the internal temperature exceeds 45°C, off if it falls below 45°C, and shutting down power if a high limit is exceeded.

3.6 DNR- / DNF-CPU / POWER Module(s)

The UEIPAC Intel CPU/Power Module (DNx-CPU-1G-40) includes the CPU module (DNx-CPU-INTEL) and the POWER board.

Please refer to **Chapter 4** for detailed descriptions of the CPU / POWER module's boards, components, and capabilities. Section 4.2.7 on page 32 provides information on system power control and monitoring.

3.6.1 DNR- / DNF-POWER Modules

In addition to the power hardware included in the DNx-CPU / POWER module, RACK-based systems include a separate power module:

- **UEIPAC 400R:** The UEIPAC 400R in a FLATRACK chassis is available in AC or DC powered versions. The DC version requires a DC power source between 9 and 36 volts. The AC unit operates from 100 to 240 VAC at 50 to 60 Hz. Power is connected at the rear of the FLATRACK chassis.
- **UEIPAC 1200R**: The power module for the UEIPAC Intel in a RACKtangle chassis is the DNR-POWER-DC. Power is connected via a Molex connector on the DNR-POWER-DC module (left-most module in the chassis).

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The key features of the unit are:

- Input power — 9-36 VDC, 80 W maximum, protected by resettable fuses and EMI chokes
- Output power sources (all with greater than 90% efficiency)
  - 24 V, 1 A (24 W)
  - 3.3 V, 5 A (16.5 W, including the 2.5 V derived voltage)
  - 2.5 V, 3 A (derived from 3.3 V source)
  - 1.5 V, 5 A, (7.5 W, including the 1.2 V derived voltage)
  - 8 V, 0.5 A (4 W for fans)
- DC/DC for 24 V, 3.3 V, and 1.5 V are synchronized from the single spread- spectrum clock source in the DNA-POWER-1GB for low EMI noise level
- Fan control (Forced ON) and status ON/OFF
- Monitoring and LED indicators (1% accuracy, 0.25 Hz update rate) for the following. See Section 4.3.2 on page 37 for more information.
  - All output voltages
  - Input current for the 9-36 VDC for the DNR-POWER-DC board
  - All voltages from the NIC/Power Module (24 V, 3.3 V, 2.5 V)
  - Temperature internal to the chassis housing
  - Fan status
- Provides 9-36 VDC for all modules from an external power source

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3.6.2 UEIPAC RACK DC Power Thresholds

Table 3-4 lists the DC power threshold specifications for RACK systems.

Table 3-4 DC Power Thresholds for UEIPAC Intel RACKtangle and HalfRACK Systems

	Backplane Power Rail Voltages	Turn-on Voltage, V[1]	Reset Voltage, V	Turn-off Voltage, V[2]	Notes
Logic power supply	+3.3V, +2.5V, +1.5V, +1.2V	7.5	7.2 (When Vin is below 7.2V, a voltage reset puts all boards into reset mode.)	7.0	Supplies power to all CPUs and FPGAs. DNR can communicate with Ethernet when CPU is functional.
Analog power supply	+24V	8.5	-	7.8	Analog power supply is used as a regulated source for on-board DC/DCs on most boards.
Fan power supply	+12V	8.5	-	8.4	
On-board DC/DCs that use input power	+VIn	7.8-8.8	-	7.5-8.5	Varies with board type.

1. Turn-on, V: The value of Vin at which the corresponding DC/DCs are turned on.
2. Turn-off, V: The value of Vin at which the corresponding DC/DCs are turned off.

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3.7 I/O Boards

All standard UEI I/O boards are available for rack-based UEIPAC Intel systems:

- Cube-based UEIPAC XXX-1G systems use a DNA- prefix, (e.g., DNA-AI-207)
- RACK-based UEIPAC 1200R systems use a DNR- prefix, (e.g., DNR-AI-207)
- FLATRACK-based UEIPAC 400R systems use a DNF- prefix, (e.g., DNF-AI-207)

These boards are electronically identical. The only difference between DNA-, DNR-, and DNF- I/O boards is the physical mounting arrangement for installation in the different chassis types.

I/O boards are populated into your chassis in the order you specify.

NOTE: Refer to the I/O board datasheets and user manuals for detailed electrical specifications, board descriptions, and user instructions. These documents are available on the UEI website at www.ueidaq.com.

Individual boards can be removed, rearranged, and/or replaced in the field once the chassis is no longer powered up.

No HOT SWAPPING

Always turn POWER OFF before performing maintenance on a UEI system. Failure to observe this warning may result in damage to the equipment and possible injury to personnel.

NOTE: Refer to Section 5.8 on page 47 for I/O board removal and replacement instructions.

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Chapter 4 UEIPAC Intel CPU / POWER Core Module

This chapter provides the following information about the hardware, ports, and capabilities of the UEIPAC G6 Intel CPU / POWER module:

- UEIPAC Intel CPU / Power Core Module Overview (Section 4.1)
- Intel CPU / POWER Module Components (Section 4.2)
  - Ethernet Ports (Section 4.2.1)
  - CPU Processor (Section 4.2.2)
  - M.2 Connector (Section 4.2.3)
  - USB Ports, Memory & Storage (Section 4.2.4)
  - DisplayPort Support (Section 4.2.5)
  - Real-time Clock (Section 4.2.6)
  - System Power Control & Monitoring (Section 4.2.7)
  - Sync Port & Reset (Section 4.2.8)
- UEIPAC Intel Ports & LEDs (Section 4.3)

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4.1 UEIPAC Intel CPU / Power Core Module Overview

The CPU / POWER core module on UEI systems is a two-board module with one board dedicated to CPU functions and the other board dedicated to power management.

- The CPU board is based on the quad-core Intel x6425RE 64-bit CPU and uses on-board programmable logic to communicate with the rest of the UEI modules (I/O boards) in the chassis.
- The POWER board is a dedicated DC/DC source and control system. For RACK-based UEIPACs, there is an additional power module (in slot 1 of UEIPAC 1200R RACKtangle enclosures or at the rear of UEIPAC 400R FLATRACK enclosures).

1. RACK-based CPU / POWER module (DNR-CPU-INTEL) shown;

Note RACKtangle-based systems include an additional power module (DNR-POWER in slot 1), which is not shown

Figure 4-1. UEIPAC Intel CPU / POWER Core Module (RACK)

4.2 Intel CPU / POWER Module Components

This section describes the major components of the UEIPAC Intel CPU / POWER module. The module communicates via the 32-bit 66 MHz bus.

Components are shown in the functional block diagram in **Figure 4-2** and described in Section 4.2.1 through Section 4.2.8.

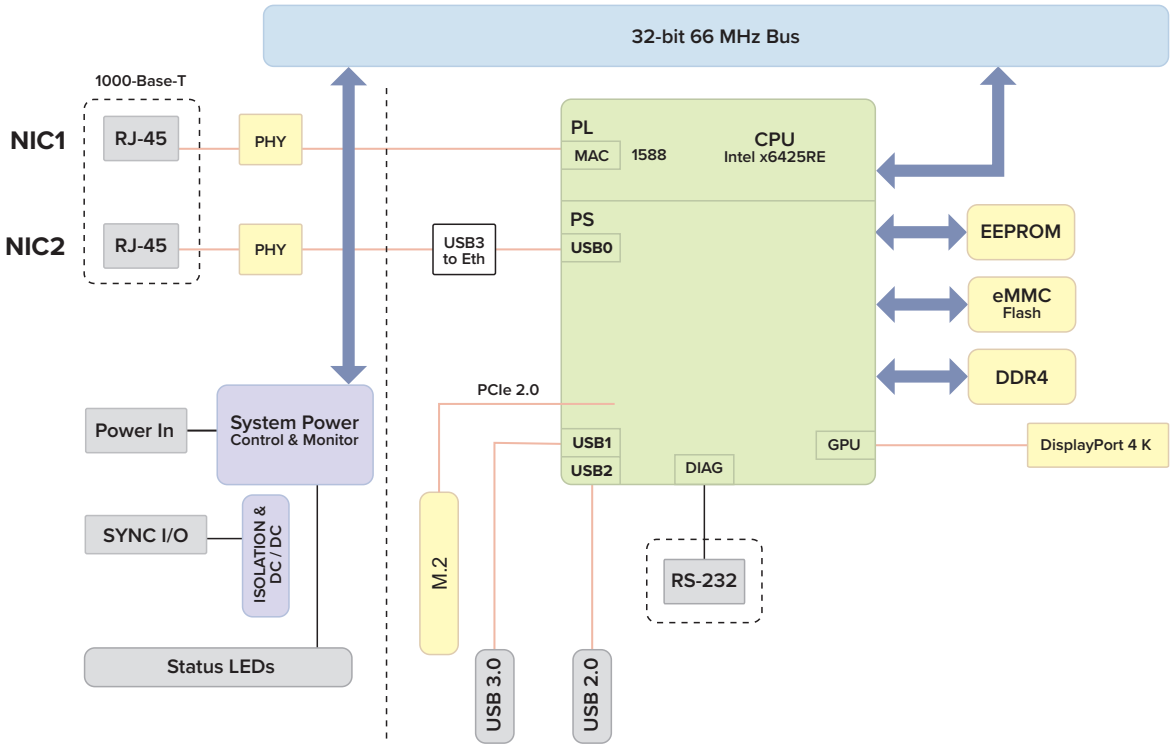

Figure 4-2. Block Diagram of CPU / Power Core Module

The location of user-accessible ports and other key features of the CPU/Power module are shown in Figure 4-3. Note that the M.2 connector is located on the underside of the CPU board and is not shown in the figure.

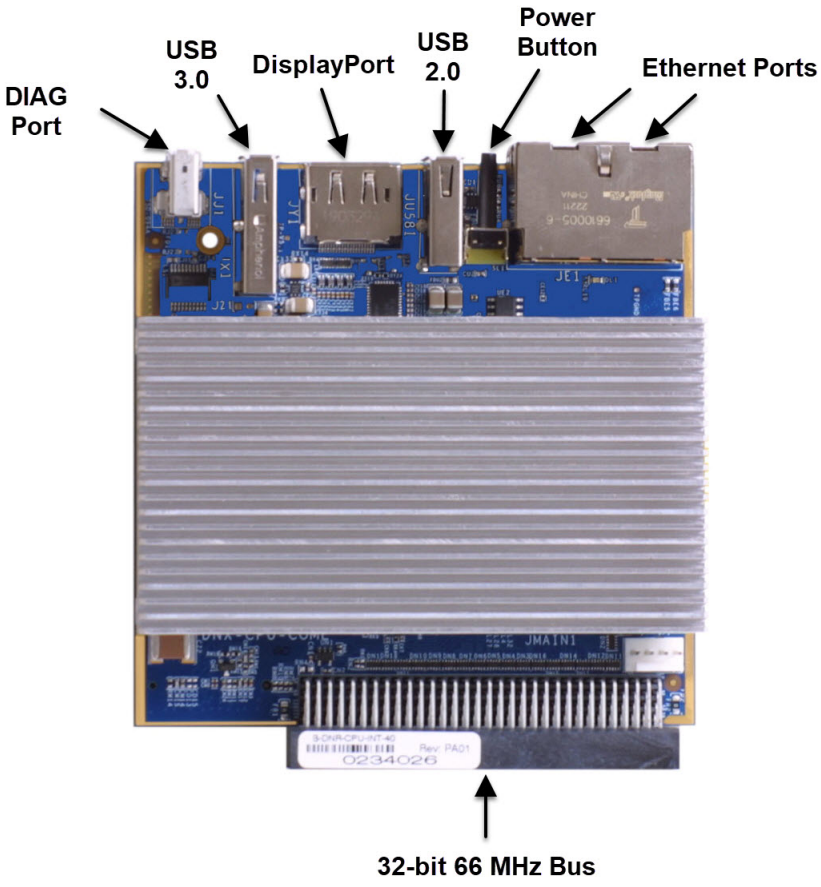

Figure 4-3. UEIPAC Intel CPU Components

4.2.1 Ethernet Ports

The UEIPAC Intel provides two independent NIC ports for communication between the UEIPAC Intel and a LAN network.

The NIC ports connect through RJ-45 connectors and feature Physical Layer (PHY) transceivers that support 10BASE-Te, 100BASE-TX and 1000BASE-T Ethernet protocols for implementation of 10/100/1000 Mbps Ethernet LANs.

The NIC1 Ethernet connection additionally supports precision clock synchronization and provides IEEE 1588 hardware time stamp support. Refer to the *PowerDNx 1PPS Sync Interface Manual* for more information about synchronization support.

Additionally, NIC1 supports TSN, and TCC (for Linux deployments). IEEE 1588, TSN, and TCC are not supported on NIC2.

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Note that for Windows deployments, the network adapter name for NIC1 will typically be “Ethernet 2” and the network adapter name for NIC2 will typically be “Ethernet”. This can be confirmed in Windows Settings by selecting an Ethernet adapter in “Settings > Network & internet” and viewing the device name (Description).

- NIC1 will be connected to “Intel E1000R”.
- NIC2 will be connected to “LAN7800 USB3”.

For Linux deployments, the logical names of the Ethernet interfaces for NIC1 and NIC2 can be obtained by issuing the `lshw -c network` command.

4.2.2 CPU Processor

The central processing of the UEIPAC Intel is the quad-core Intel Atom x6425RE 64-bit CPU. The UEIPAC Intel runs at a maximum of 1.9 GHz. It features an Intel UHD 400 MHz, 60 Hz GPU with DisplayPort. Support for TSN and Intel TCC (for Linux deployments) is also provided.

4.2.3 M.2 Connector

The M.2 connector on the UEIPAC Intel CPU board is a key M connector that can be used to connect add-in cards such as an additional NVMe SSD drive. Sizes of 2242, 2260, or 2280 are supported. Industrial pSLC drives up to 320 GB and TLC drives up to 2 TB are supported.

4.2.4 USB Ports, Memory & Storage

The UEIPAC Intel CPU board provides a USB 3.0 port and a USB 2.0 port. Refer to the **Table 4-1** for more information about the USB ports, DDR4 SDRAM, and storage capabilities.

Table 4-1 USB Port, Memory, and Storage Components in UEIPAC Intel

Item	Description
USB 2.0 and USB 3.0 Ports	The external USB ports connect to the CPU.
RAM (DDR4)	8 GB of SDRAM
eMMC Flash Memory	32 GB flash for OS and/or user application storage
Solid State Hard Drive	Optional solid state hard drive(s) (refer to Section 4.2.3 for locations) • Optional SSD installed via M.2 connector

4.2.5 DisplayPort Support

DisplayPort (DP) support is provided in UEIPAC Intel systems. See Section 5.3.1.3 for information on connecting to the UEIPAC Intel using a DisplayPort connection. Once the OS finishes booting, enter a username and password. The default username and password are `root`.

4.2.6 Real-time Clock

The real-time clock (RTC) for the UEIPAC Intel system stores persistent date and time information. The UEIPAC G6 Intel uses the real-time clock provided by the Intel Atom x6425RE CPU.

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4.2.7 System Power Control & Monitoring

Control and monitoring of system power are provided by the DNx-POWER-1G board of the DNx-CPU CPU / POWER core module.

DNx-POWER-1G comprises an FPGA and other hardware to control and monitor system power, perform power conditioning on input power, control diagnostic LED states, isolate and direct synchronization I/O to the CPU board, and control fan operation. The UEIPAC Intel DNx-POWER-1G board is the lower board of the CPU module as shown in Figure 4-4. The components are listed in Table 4-2.

RACK-based CPU / POWER module shown;
For RACK-based systems, a second power module (not shown) additionally handles power control & monitoring

Figure 4-4. UEIPAC Intel CPU / POWER Core Module (RACK)

NOTE: For the UEIPAC 1200R (RACKtangle), there is an additional power module, DNR-POWER-DC, which is located in slot 1 of the chassis; for UEIPAC 400R (FLATRACK), an additional power module is located at the rear of the FLATRACK chassis

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Table 4-2 Components on UEIPAC Intel Power Board (DNx-Power-1G)

Item	Description
FPGA	FPGA to communicate with the CPU board and modules via the 32-bit 66 MHz bus
System Temperature & Power Monitoring	Monitoring via 24-bit ADC: 2.5 V source, 3.3 V source, 24 V source, Vin, 1.5 V source, 1.2 V source, 8 V FAN source, I_{in}, $I_{3.3V}$, $I_{1.5V}$, $I_{1.2V}$, I_{24V}, and system temperature
Power In[1]	External power connector. • **UEIPAC XXX-1G Cube chassis**: Power In is 4-pin Molex connector as shown in Figure 4-5. • **UEIPAC 1200R RACKtangle chassis**: The Power In Molex connector is provided on the DNR-POWER board that is installed in the first slot of the RACK. • **UEIPAC 400R FLATRACK chassis**: Power In is -AC or -DC, connected at the rear of the RACK.
Status LEDs	LEDs are described in Table 4-4 on page 36.

1. See Section 5.5 on page 46 for DIAG, sync, and power connector pinout diagrams.

4.2.8 Sync Port & Reset

The UEIPAC Intel CPU / POWER Core Module provides a recessed reset button adjacent to the synchronization port, labeled as “Reset/Sync” on the faceplate. Refer to Figure 4-5 on page 34 for location.

The “Sync” port connection consists of two TTL input lines (CLK and TRIGGER) and two TTL output lines (CLK and TRIGGER), along with +5 V power and isolated ground. Refer to Section 5.5 on page 46 for pinout.

The Sync port is used for high-speed system-to-system synchronization, which allows sharing triggers and clocks among multiple systems. Two systems may be connected together directly, and larger groups may use UEI’s SYNC STP panel to share timing signals among many chassis and systems.

- Trigger and clock inputs accept TTL signals in (3.3 V to 5 V). The inputs also have internal pull-up resistors to an internal 5 V supply, making the inputs also compatible with a low-side drive open-collector output.
- Trigger and clock outputs use 5 V logic levels. The sync connector’s ground and 5 V power connections are provided by its own isolated DC-DC converter.

The SYNC port is available for 1PPS synchronization. For more information, refer to the *PowerDNx 1PPS Sync Interface Manual,* which also describes IEEE 1588 PTP synchronization provided via Ethernet ports.

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4.3 UEIPAC Intel Ports & LEDs

This section describes the ports and LEDs on the UEIPAC Intel.

- “CPU / POWER Module Ports & LEDs” in Section 4.3.1
- “UEIPAC 1200R POWER-DC Module Ports & LEDs” in Section 4.3.2

4.3.1 CPU / POWER Module Ports & LEDs

The ports and LEDs of the CPU / POWER module are illustrated in Figure 4-5 and described in **Table 4-3**.

For UEIPAC 1200R RACKtangle-based systems only, additional LEDs are installed on the DNR-POWER-DC module. The ports and LEDs of the 1200R CPU / POWER module are illustrated in Figure 4-7 and described in Table 4-5.

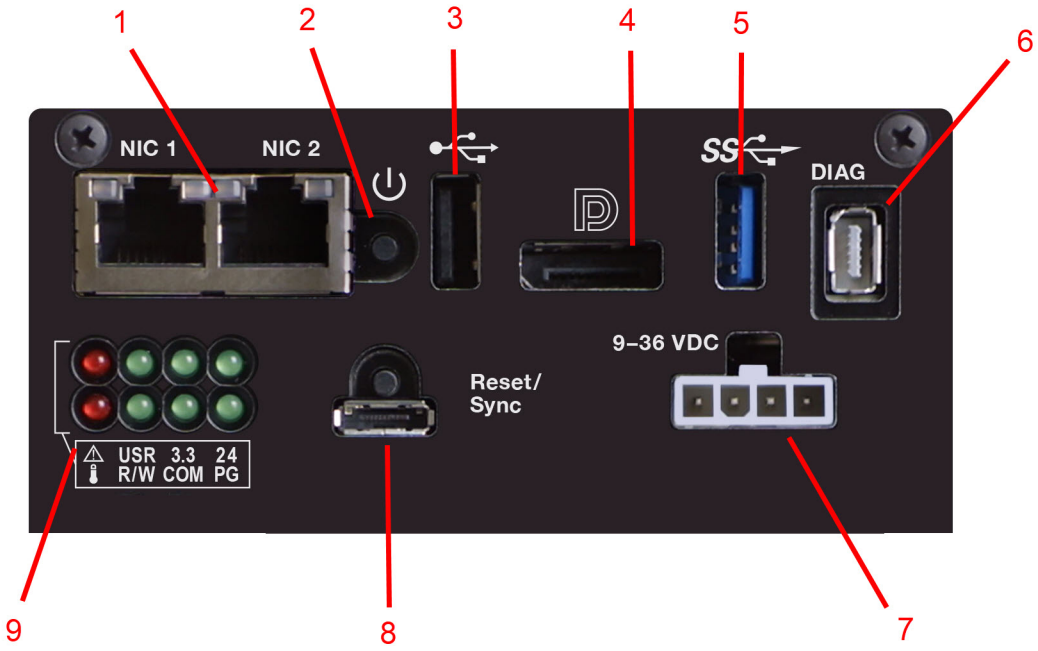

Figure 4-5. UEIPAC Intel Cube Front Panel Arrangement

Table 4-3 UEIPAC Intel Front Panel Descriptions

No.	Name	Description	Section
1	NIC1, NIC2	Ethernet ports: 10/100/1000Base-T connection. RJ-45 connector for NIC1 and NIC2	Section 4.2.1
2	Power	Recessed power button.	
3	USB 2.0	USB 2.0 port	Section 4.2.4
4	DisplayPort	Port for DisplayPort connection	Section 4.2.5
5	USB 3.0	USB 3.0 port	Section 4.2.4
6	DIAG port[1]	Reserved	
7	Power-In[1]	External power connector. **Cube**: Power In 4-pin Molex connector as shown in Figure 4-5: 9-36 VDC, DNA-PSU adapter included. **RACKtangle**: DC In Molex connector is included on the DNR-POWER-DC board (**Figure 4-7**) that is installed in the first slot of the RACK. **FLATRACK**: Power In is -AC or -DC, connected at the rear of the rack.	Section 4.2.7
8	Sync port[1,2]	High-speed, chassis-to-chassis connector for synchronizing multiple UEI systems.	Section 4.2.8
8	Reset	Recessed reset button.	Section 4.2.8
9	Status LEDs	See Figure 4-6 and Table 4-4 for LED descriptions.	Section 4.3.1

1. See Section 5.5 on page 46 for DIAG, sync, and power connector pinout diagrams.
2. Refer to the *PowerDNx 1PPS Synchronization Interface Manual* for more information about 1PPS or IEEE 1588 / PTP programming.

Status LEDs are displayed in Figure 4-6 and described in Table 4-4. LEDs are physically mounted on the POWER board of the CPU / POWER Core Module.

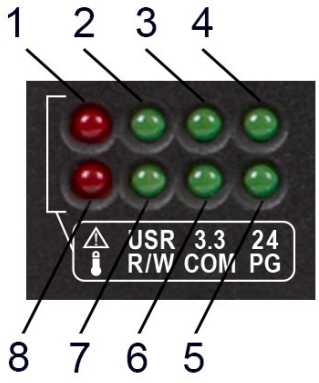

Figure 4-6. UEIPAC Intel Front Panel LEDs

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Table 4-4 System Status LED Descriptions

No.	Name	Description
1	ATT	Indicates system needs attention due to overrange condition: Error when red LED is ON
2	USR	Optionally controlled by user application[1]: OFF is default
3	3.3	Indicates status of internal 3.3 V supply: LED ON (OK) / OFF (ERROR)
4	24	Indicates status of internal 24 V supply: LED ON (OK) / OFF (ERROR)
5	PG	Indicates the presence of a valid power input: LED ON (OK) / OFF (ERROR)
6	COM	Indicates I/O communication active: Flashes once per second when communicating / OFF when not
7	R/W	Indicates bus activity: Flashes when bus is active / OFF when not
8	OverTemp	Indicates high temperature condition in module: LED ON (high temp) / OFF when not

1. For more information about how to read or set LEDs, please refer to `DqAdvDnxpSetConfig()` API described in the *PowerDNA API Reference Manual* and/or `SampleDiagnostics.c` example code included with your “PowerDNA Software Suite” installation.

4.3.2 UEIPAC 1200R POWER-DC Module Ports & LEDs

For UEIPAC 1200R RACKtangle-based systems only, additional LEDs are installed on a DNR-POWER-DC module.

The ports and LEDs of the DNR-POWER-DC module are illustrated in Figure 4-7 and described in **Table 4-5**.

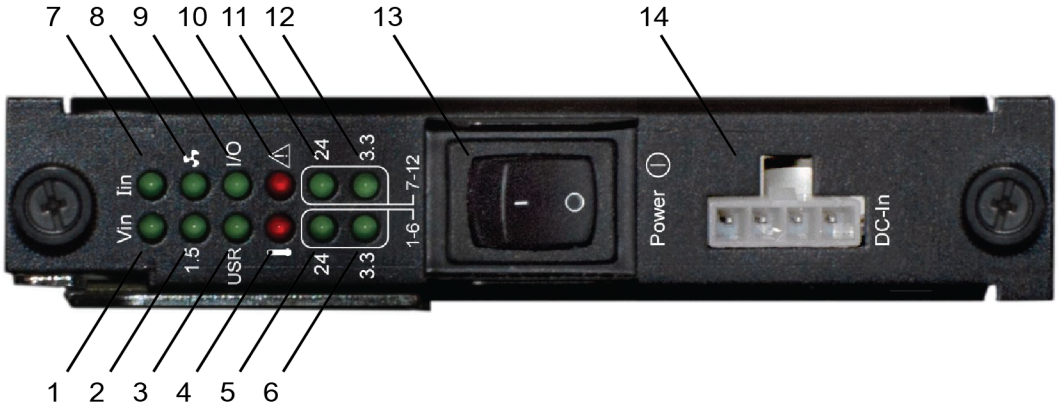

Figure 4-7. UEIPAC 1200R DNR-POWER-DC Front Panel Arrangement

Table 4-5 UEIPAC 1200R DNR-POWER-DC Front Panel Descriptions

No.	Name	Description
1	Vin LED	Indicates status of input voltage: LED ON (OK) / OFF (ERROR)
2	1.5 LED	Indicates status of 1.5 V onboard supply: LED ON (OK) / OFF (ERROR)
3	USR LED	Optionally controlled by user application[1]: OFF is default
4	Temperature LED	Indicates high temperature condition in module: LED ON (high temp) / OFF when not
5	24 LED	Indicates status of 24 V onboard supply for I/O boards 1 - 6: LED ON (OK) / OFF (ERROR)
6	3.3 LED	Indicates status of 3.3 V onboard supply for I/O boards 1 - 6: LED ON (OK) / OFF (ERROR)
7	Iin LED	Indicates status of input current: LED ON (OK) / OFF (ERROR)
8	Fans LED	Indicates state of fans: LED ON (ON) / OFF (OFF)
9	I/O LED	Indicates I/O circuitry operation: LED flashes 1/second
10	ATTN LED	Indicates system needs attention due to overrange condition: Error when red LED is ON
11	24 LED	Indicates status of 24 V onboard supply for I/O boards 7 - 12: LED ON (OK) / OFF (ERROR)

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No.	Name	Description
12	3.3 LED	Indicates status of 3.3 V onboard supply for I/O boards 7 - 12: LED ON (OK) / OFF (ERROR)
13	Power[2]	Chassis ON / OFF switch.
14	DC In	DC In 4-pin molex connector as shown in **Figure 4-7**: 9-36 VDC, DNA-PSU adapter included..

1. For more information about how to read or set LEDs, please refer to `DqAdvDnxpSetConfig()` API described in the *PowerDNA API Reference Manual* and/or `SampleDiagnostics.c` example code included with your “PowerDNA Software Suite” installation.
2. See Section 5.5 on page 46 for power connector pinout diagrams.

Chapter 5 Installation and Configuration

This chapter provides getting started instructions for working with your UEIPAC Intel for initial communication. Detailed installation, configuration, and usage instructions are provided in the *UEIPAC Intel Software Manual*.

The following installation and configuration topics are included in this chapter:

- Shipment Contents (Section 5.1)
- Installing UEIPAC Intel Development Software (Section 5.2)
- UEIPAC Intel Configuration (Section 5.3)
  - Accessing the UEIPAC Intel System (Section 5.3.1)
  - Interrogating the UEIPAC Intel System (Section 5.3.2)
  - Updating IP Addresses (Section 5.3.3)
- Mounting and Field Connections (Section 5.4)
- Pinout Diagrams (Section 5.5)
- Wiring I/O Boards (Section 5.6)
- Repairing (and Upgrading) a UEIPAC System (Section 5.7)
- Removing and Replacing I/O Boards (Section 5.8)

5.1 Shipment Contents

The contents of the shipping package for a standard UEIPAC Intel system include the following:

- A Cube or RACK enclosure.
  Preinstalled with a CPU / POWER module, blank filler panels (if specified), plus your selection of I/O boards.
  - UEIPAC 400R and 1200R RACK-based systems also include a DNR-POWER module
  - UEIPAC 1200R systems also include a DNR-BUFFER-F module.
- A DNA-PSU-XXX universal power supply.
- Cat5e Ethernet cable, 7 ft.

5.2 Installing UEIPAC Intel Development Software

Refer to the *UEIPAC Intel Software Manual* for instructions on how to setup Windows and Linux-based development systems.

5.3 UEIPAC Intel Configuration

The following subsections provide basic information on configuration of a UEIPAC Intel system. As applicable, differences between Windows and Linux deployments will be noted.

5.3.1 Accessing the UEIPAC Intel System

A UEIPAC Intel system can run as a standalone or hosted system, pre-configured with either Windows 11 IoT Enterprise or Rocky Linux. The following sections provide instructions for accessing a Windows UEIPAC Intel system using one of these methods:

You can access a UEIPAC Intel system using the following methods:

- Remote Desktop (Windows) (Section 5.3.1.1)
- SSH (Section 5.3.1.2)
- Connecting Directly using DisplayPort (Section 5.3.1.3)

5.3.1.1 Remote Desktop (Windows)

On Windows deployments, a Remote Desktop connection allows you to pass files by copy-paste between the UEIPAC Intel and a Windows host and provides seamless access to the Windows 11 Graphical User Interface via the host computer.

STEP 1: Power up the UEIPAC.
Connect the DC output of the power supply (24 VDC) to the Power In connector on the UEIPAC Intel and connect the AC input on the power supply to the AC power source.

STEP 2: Connect the Ethernet port on the UEIPAC Intel to the Ethernet port on the host via the included cable.

STEP 3: From the Windows Host, find the Remote Desktop application using the Search bar.

STEP 4: Once Remote Desktop is open (Figure 5-1), enter the IP address of the UEIPAC Intel into the entry box for “Computer”. Remember, the factory default IP for NIC1 is 192.168.100.2 and for NIC2 is 192.168.101.2. Make sure that the host Ethernet address falls within the same subnet for the NIC that is connected.

STEP 5: Enter the “User name” (factory default user is “root”), then click “Open”.

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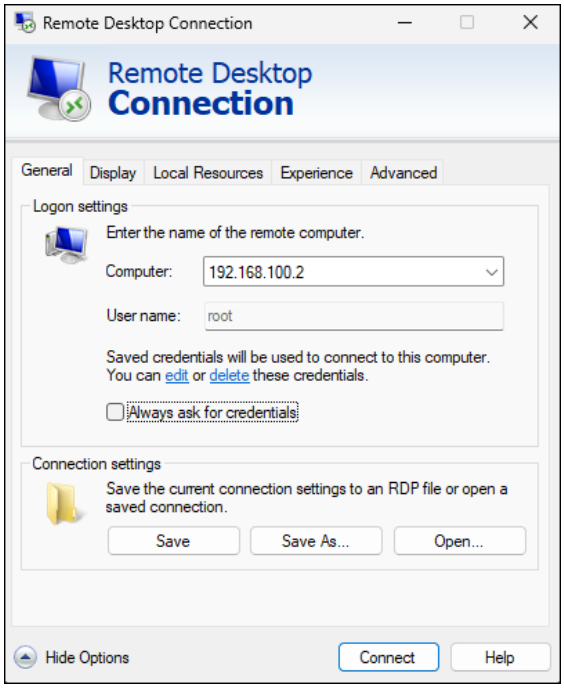

Figure 5-1 Remote Desktop Connection

STEP 6: When prompted, enter the password for default user “root” (Figure 5-2). The default password when shipped is “root”. Press “OK”.

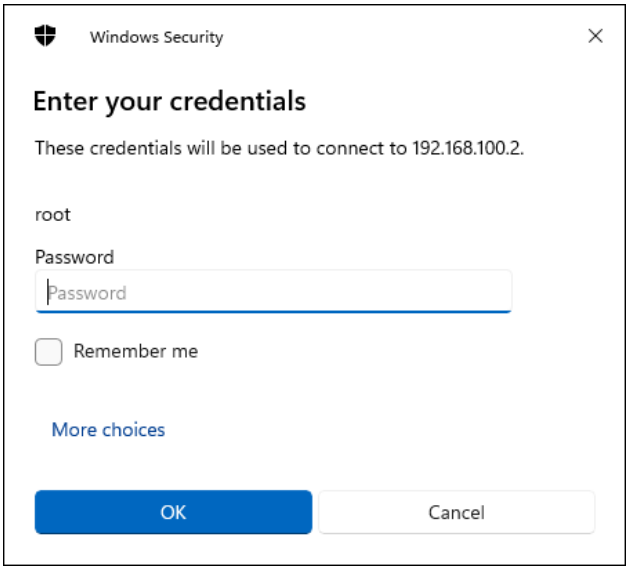

Figure 5-2 Enter Credentials

5.3.1.2 SSH

The SSH (Secure Shell) protocol can be used to access a UEIPAC Intel system as follows:

STEP 1: Power up the UEIPAC.
Connect the DC output of the power supply (24 VDC) to the Power In connector on the UEIPAC Intel and connect the AC input on the power supply to the AC power source.

STEP 2: Connect the Ethernet port on the UEIPAC Intel to the Ethernet port on the host via the included cable.

STEP 3: Open a terminal window and type:

```
ssh <username>@<IP address>
```

Remember, the factory default user is “root” and the default IP address is 192.168.100.2 for NIC1 and 192.168.101.2 for NIC2.

STEP 4: When prompted for a password, enter the password for the user. The factory default user’s password is “root”. This will give access to a Windows or Linux command prompt.

5.3.1.3 Connecting Directly using DisplayPort

Use the following steps to connect directly to the UEIPAC Intel with a DisplayPort monitor connected to the DisplayPort connector on the UEIPAC Intel and a USB keyboard and mouse connected to one of the two USB ports.

STEP 1: Power up the UEIPAC.
Connect the DC output of the power supply (24 VDC) to the Power In connector on the UEIPAC Intel and connect the AC input on the power supply to the AC power source.

STEP 2: Plug in the DisplayPort cable from the monitor into the DisplayPort connector on the CPU front panel.

STEP 3: Plug a USB keyboard/mouse pair into one of the USB ports near the DisplayPort connection. Use a USB hub if needed.

STEP 4: If it is your first time logging in, you will see a profile for the factory-configured default user “`root`”, which can be accessed with default password “`root`”.

STEP 5: Once logged in as “root”, you can create users and configure system settings as you desire using a terminal. Windows users will be able to use theWindows GUI.

5.3.1.4 Additional Information for Linux Users

For Rocky Linux users, UEI provides a non-root user account in the Rocky Linux distribution: (username `uei`, password `uei`).

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5.3.2 Interrogating the UEIPAC Intel System

To learn the version of UEIPAC drivers installed in your system and to display a table of system modules, you can use the `devtbl` command. See Figure 5-3 for an example of `devtbl` output.

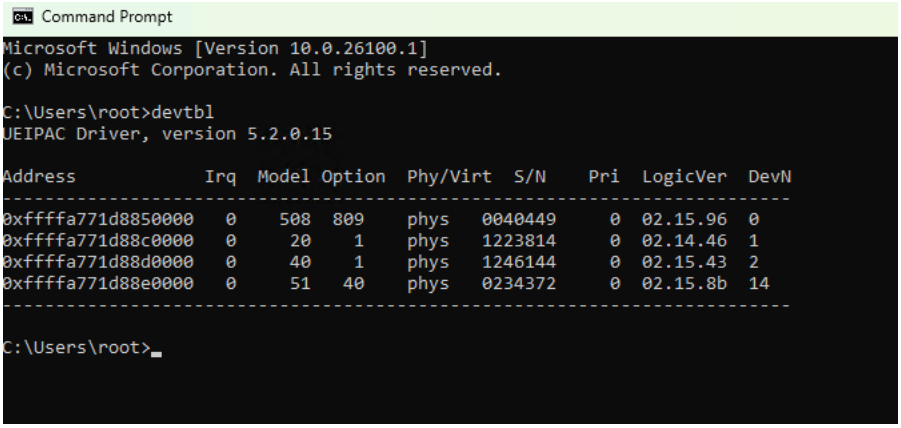

Figure 5-3 devtbl Output

In Figure 5-3:

- `Model` is the model number (I/O board, power board(s) or CPU board)
- `S/N` is the serial number
- `LogicVer` is the FPGA logic version
- `DevN` is the device order in the chassis: 0 corresponds to the I/O board in the first position, etc. (CPU and power boards use DevNs after I/O)

5.3.2.1 Additional Information for Linux Users

Enter `uname -a` for information about the kernel version.

You can use the `systemctl` command to interrogate what services are enabled in your UEIPAC, (e.g., `systemctl list-unit-files --all`).

You can use the `df` command to interrogate where devices are auto-mounted in your UEIPAC. As a reference, the following are used for storage device names:

- eMMC FLASH is device name `/dev/mmcblk0`
- USB devices (external and internal) are `/dev/sdxn`, where x is a for the first drive and b for the second drive. n is the partition number.
- M.2 SSD devices are `/dev/nvme*`

NOTE: Please refer to the *UEIPAC Intel Software Manual* for additional installation and configuration instructions and descriptions.

5.3.3 Updating IP Addresses

The UEIPAC Intel ships with a static IPv4 address for NIC1 and NIC2, which are pre-configured at the factory to 192.168.100.2 and 192.168.101.2, respectively. UEI provides scripts for setting a persistent IP address within a 255.255.255.0 network.

The IP addresses of the UEIPAC G6 Intel can be modified by using one of the following methods. For additional information on changing IP addresses, please refer to the *"UEIPAC Intel Software Manual*".

- Run Scripts over Ethernet (Section 5.3.3.1)
- Run Scripts using DisplayPort (Section 5.3.3.2)

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NOTE: When updating IP addresses, be sure to configure the Ethernet ports to be on different subnets. Configuring both Ethernet ports to be on the same subnet (for example, setting NIC to192.168.100.2 and NIC2 to 192.168.100.3) can cause errors with kernel packet routing.

5.3.3.1 Run Scripts over Ethernet

UEI provides scripts to update the IP Addresses of your UEIPAC Intel. The scripts can be run over an Ethernet connection as follows:

STEP 1: Connect a PC directly to the NIC1 port of your UEIPAC Intel using an Ethernet cable.

STEP 2: Record the current IP address of the PC network adapter.

STEP 3: Configure the PC network adapter IP address to 192.168.100.x. Note that x can be 1 to 254 but x cannot be 2 since that is the default.

STEP 4: At a command prompt, enter "`ssh 192.168.100.2`".

STEP 5: For Linux, enter "`setipeth0 <new IP address>`" to change the IP address for NIC1.
For Windows, use "`setip1 <new IP address>`" to change the IP address for NIC1.

STEP 6: Configure the PC network adapter IP address to its former IP address.

STEP 7: At a command prompt, use the `ssh` command with the newly assigned IP address for the UEIPAC Intel.

NOTE: The instructions above can also be used to change the IP address of NIC2. NIC2 comes with a default IP address of 192.168.101.2.
For Linux, use `setipeth1` to change the IP address for NIC2.
For Windows, use `setip2` to change the IP address for NIC2.

5.3.3.2 Run Scripts using DisplayPort

To run the scripts for updating the IP Addresses of your UEIPAC Intel using a DisplayPort (DP) connection, perform the following steps.

STEP 1: Connect a DP monitor to the DP port and a USB keyboard and mouse through a USB hub to the USB port (refer to Section 5.3.1.3).

STEP 2: For Linux users, enter "`setipeth0 <new IP address>`" at a command prompt to change the IP address for NIC1. Use `setipeth1` to change the IP address for NIC2.
For Windows users, enter "`setip1 <new IP address>`" at a command prompt to change the IP address for NIC1. Use `setip2` to change the IP address for NIC2.

5.3.3.3 Additional Information for Windows Users

Windows users can also use command prompt utilities such as `netsh` and `ipconfig`, or use the Windows GUI by navigating to Settings > Network & internet > Ethernet and selecting the Edit button next to "IP assignment" to edit the IPv4 address.

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5.4 Mounting and Field Connections

This section provides mounting and field connection descriptions for each of the UEIPAC Intel chassis types:

UEIPAC XXX-1G:

The UEIPAC XXX-1G (Cube) mounting options include the following:

- For horizontal surface mounting, use a flange accessory and secure the case directly to the surface.
- For mounting on a vertical wall surface, use a 19RACKW accessory with DIN rail and attach the assembly to a standard 19-inch rack with screws.

UEIPAC 1200R:
The UEIPAC 1200R (RACKtangle) mounting options include the following.

- For horizontal surface mounting, use the rubber feet supplied with the standard enclosure or bolt the case directly to the surface.
- For mounting on a vertical wall surface, attach flanges to both ends of the enclosure with the flanges aligned flush with the rear of the enclosure; then fasten the flanges to the surface with screws or bolts.
- For mounting in a standard 19-inch rack, attach flanges to both ends of the enclosure with the flanges aligned flush with the front of the enclosure. Then attach the flanges to the rack with bolts.

Note that the flanges are included with the purchase of the UEIPAC Intel racks. If you need more clearance from the rack front panel, refer to the DNR-EXT-BRACKET-4 which provides 3.625 inches of clearance.

UEIPAC 400R:
The UEIPAC 400R (FLATRACK) can be mounted in a standard 19-inch rack using the included rack mount brackets or on a horizontal surface using the base mount brackets.

- For mounting in a standard 19-inch rack, attach flanges to both ends of the enclosure with the flanges aligned flush with the front of the enclosure. Then attach the flanges to the rack with bolts.

If you need technical drawings, please contact UEI support at uei.support@ametek.com.

5.4.1 Physical Dimensions

The housing used in each of the UEIPAC chassis types is as follows:

- UEIPAC XXX-1G Cube consists of an extruded aluminum box with slotted guides plus a faceplate and rear cover.
- UEIPAC 400R (FLATRACK) is compatible with Specification EIA-310-C for 19” Rack Mounting Equipment and is designed to occupy 1U unit of vertical space (where 1U is 1.75”).
- UEIPAC 1200R (RACKtangle) systems are also compatible with Specification EIA-310-C for 19” Rack Mounting Equipment and is designed to occupy 3U units of vertical space.

The physical dimensions of the standard UEIPAC Intel versions (including cooling fans) are listed in Table 5-1:

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Table 5-1 UEIPAC Dimensions

Version	Dimensions[1]	I/O Slots
UEINET-PAC	4.1” x 4.0” x 2.7”	slot for 1 I/O board
UEIPAC 300-1G	4.1” x 5.0” x 4.0”	slots for up to 3 I/O boards
UEIPAC 600-1G	4.1” x 5.0” x 5.8”	slots for up to 6 I/O boards
UEIPAC 700-1G	4.1” x 5.0” x 6.6”	slots for up to 7 I/O boards
UEIPAC 400R	16.75” x 7.2” x 1.75”	slots for up to 4 I/O boards
UEIPAC 1200R	17.5” x 6.2” x 5.25”	slots for up to 12 I/O boards

1.Dimensions are given as $width_{base} \times depth_{base} \times height$.

5.5 Pinout Diagrams

Pinout diagrams for the Molex power connector, synchronization (SYNC) port, and DIAG port connectors are shown in Figure 5-4.

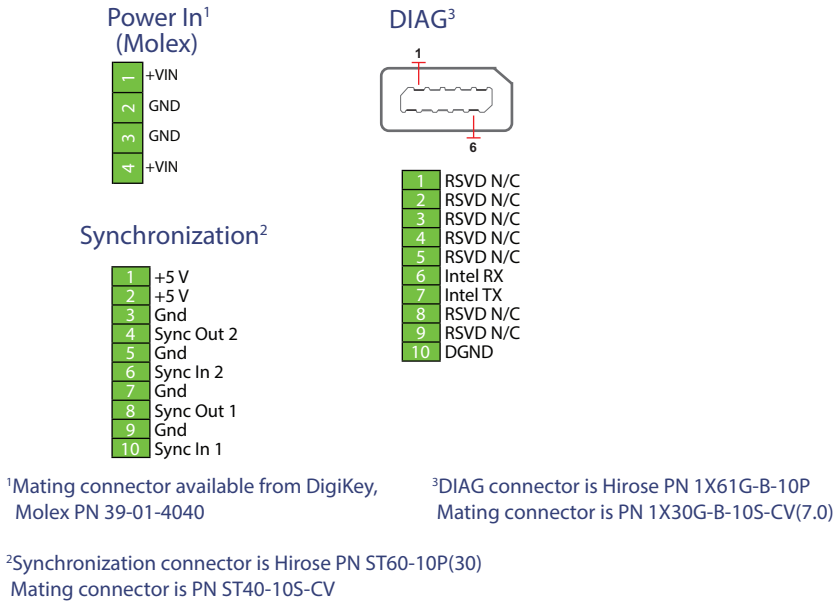

Figure 5-4 UEIPAC Intel Pinout Diagrams

5.6 Wiring I/O Boards

Refer to the applicable I/O board manuals and datasheets for pinouts and proper wiring to boards.

Datasheets and manuals are provided on our website at www.ueidaq.com.

5.7 Repairing (and Upgrading) a UEIPAC System

UEIPAC Intel systems come from the factory calibrated and pre-configured with either Windows 11 IoT Enterprise or Rocky Linux 9.6 and UEI drivers loaded in memory.

If you encounter a problem with a UEIPAC Intel system, note that individual modules are designed for field replacement and are not suited for field repairs.

If you want to remove and replace individual boards or other system modules, you can do that in the field once you power-down your system. You can also rearrange the locations of boards within the enclosure at any time. However, note that you may need to reprogram I/O board locations in your application. Refer to Section 5.8 for more information.

No Hot Swapping

Always turn POWER OFF before performing maintenance on a UEI system. Failure to observe this warning may result in damage to the equipment and possible injury to personnel.

If you want to enhance, repair, or otherwise modify a specific I/O board, you must send the module back to the factory or to your local distributor.

This process requires that you request an RMA number from UEI before shipping. To do so, contact uei.support@ametek.com and provide the following information:

1. Model Number of the unit, (e.g., DNR-AI-217)
2. Serial Number of the unit
3. Reason for return, (e.g., faulty channel, needs calibration, etc.)

UEI will process the request and issue an RMA number.

5.8 Removing and Replacing I/O Boards

For all chassis types, individual boards can be removed and replaced in the field once power is removed from the chassis.

No Hot Swapping

Always turn POWER OFF before performing maintenance on a UEI system. Failure to observe this warning may result in damage to the equipment and possible injury to personnel.

You can rearrange the locations of boards within the enclosure at any time. However, note that when installing I/O boards in a Cube chassis, you may need to move jumpers on the I/O board(s).

Removing and Replacing I/O Boards in a Cube Chassis

Each Cube I/O board includes a jumper block that identifies the physical position of the I/O board in the stack. If you change the order of your I/O boards in your Cube or install a new board, you may need to adjust corresponding hardware jumpers. This is only applicable in Cube systems (jumpers are not used in DNR or DNF I/O boards for installation in a UEIPAC 400R or UEIPAC 1200R).

Refer to the *PowerDNA Field Installation Guide* for more information about installing I/O boards and setting jumper positions in Cubes.

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NOTE: For additional maintenance procedures, please refer to the *DNA Maintenance Manual* for Cube-based chassis and the *DNR Maintenance Manual* for RACK-based chassis.

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Chapter 6 PowerDNA Explorer Application

PowerDNA Explorer is a GUI-based application for communicating with your UEI systems.

This chapter provides an overview of PowerDNA Explorer capabilities:

- Overview of PowerDNA Explorer (Section 6.1)
- Launching PowerDNA Explorer (Section 6.2)
- Displaying Diagnostic Data for CPU / Power Module (Section 6.3)
- Obtaining a Hardware Report (Section 6.4)
- Interacting with Input / Output Boards (Section 6.5)
- Displaying Wiring Diagrams for I/O Boards (Section 6.6)
- Interacting with Other UEIPACs and UEI Systems (Section 6.7)

NOTE: The UEIPAC Intel includes an embedded version of PowerDNA Explorer, pre-installed with the system. PowerDNA Explorer can also be run from a Windows or Linux host.

6.1 Overview of PowerDNA Explorer

PowerDNA Explorer provides a platform for the following:

- Displays diagnostic data on CPU / Power module (temperatures, voltage supply measurements, error conditions)
- Reports serial numbers and version information about the CPU / Power module and I/O boards
- Provides hardware report of CPU / Power modules and all I/O boards
- Acquires input data from input channels
- Sets output values for output channels
- Reads diagnostic data from I/O boards that provide diagnostic data
- Resets circuit breakers on I/O boards that provide circuit breakers
- Allows users to configure initial and shutdown output levels on supported boards
- Provides users an alternate application to communicate with I/O boards to help troubleshoot issues when first bringing up their application
- Discovers and interacts with other UEI systems on a range of user-defined IP addresses on a network

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6.2 Launching PowerDNA Explorer

For Windows systems, the default location of “PowerDNA Explorer.exe” is:

```
C:\Program Files (x86)\UEI\PowerDNA\Applications
```

6.2.1 Startup GUI

When PowerDNA Explorer is first launched, the application initializes the range of IP addresses to scan to the local loop-back address (127.0.0.1) and scans the network for addresses in that range.

The GUI opens and displays any UEI systems discovered (Figure 6-1 shows UEIPAC Intel is the only UEI system discovered):

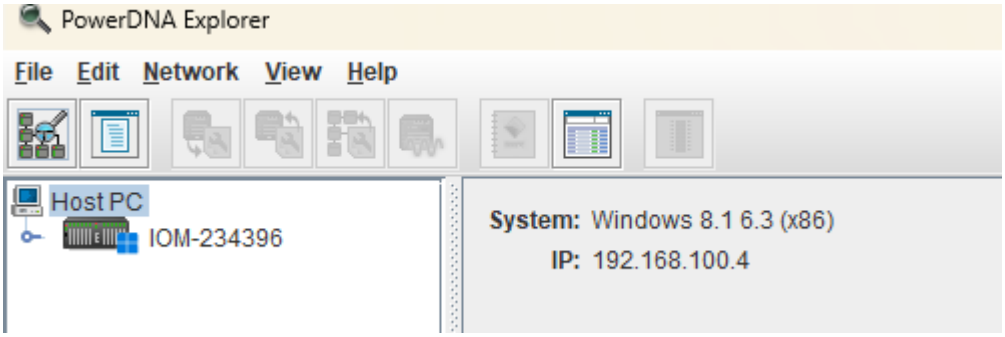

Figure 6-1. Initial Screen of PowerDNA Explorer

To discover other UEI systems on your network you can set the range by selecting *Network >> Address Ranges*, and then rescan by selecting *Network >> Scan Network.*

After a scan, the device tree is populated with all central controllers, UEI systems (racks and cubes), and device boards accessible from the network, as filtered through the range defined in *Network >> Address Ranges* dialog.

Refer to Section 6.7 on page 67 for more information about modifying the IP address range.

6.2.2 Interacting with UEI Systems

All discovered UEI systems display in the Device Tree panel on the left.

For example, in Figure 6-1, the UEIPAC Intel displays as the `IOM-234396` name (which is in the format of `IOM-<serial number>`). An OS-specific logo will be displayed to indicate if the UEIPAC Intel is running Windows, Rocky Linux, or RedHawk Linux.

To display CPU / Power diagnostics and a list of installed I/O boards, double-click the name in Device Tree panel on the left of the display (see Figure 6-2).

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6.3 Displaying Diagnostic Data for CPU / Power Module

When you click the name of a the CPU / POWER module or the name of an I/O board, the settings panel (to the right) populates with data and control settings available for that board.

The screenshot in Figure 6-2 shows the data for the CPU and POWER modules. The displayed data is described in Table 6-1.

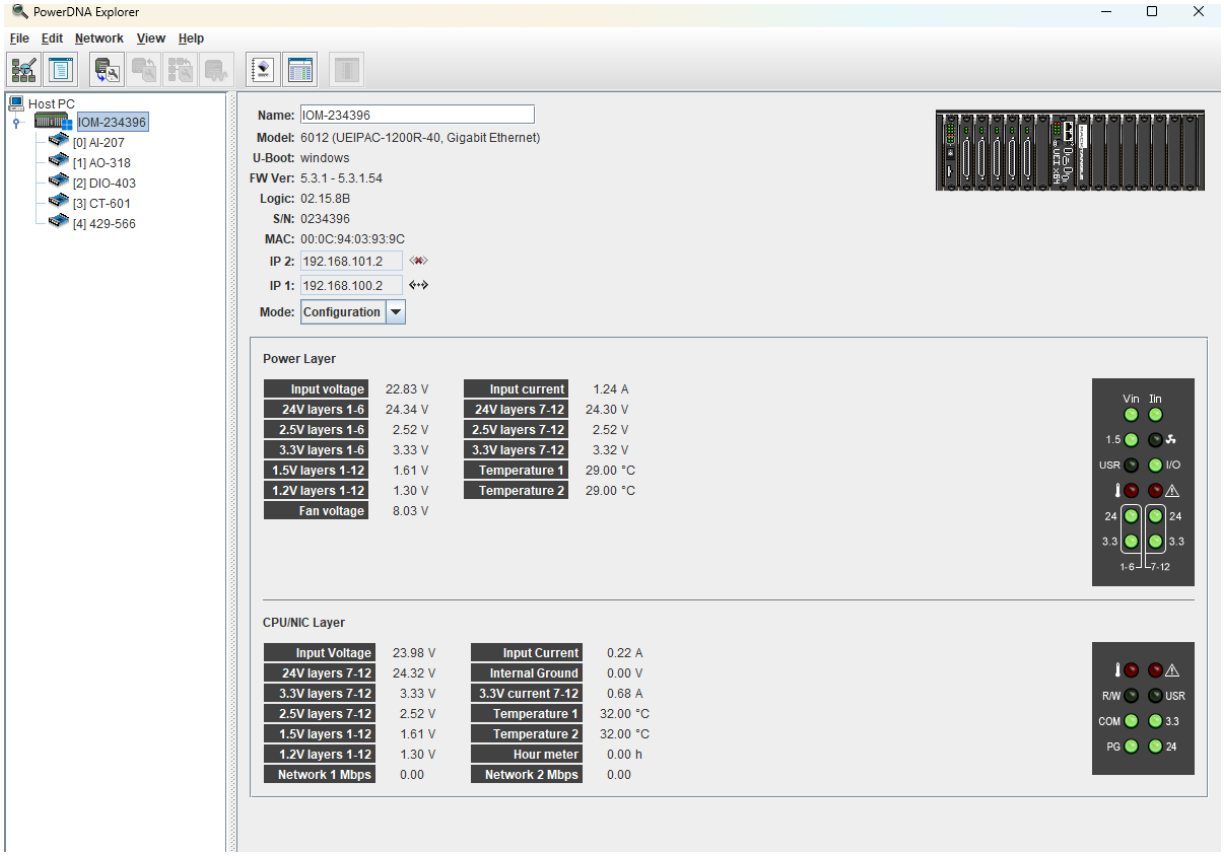

Figure 6-2. Example of CPU / Power Panel for UEIPAC 1200R

Table 6-1 Fields and Descriptions for CPU / POWER Settings Panel

Field	Description
Name	Read/write UEI system name. Users can customize To change: Edit field, and then click *Network >> Store Config*
Model	Displays the model number
FW Ver	Displays the version of the firmware installed on the system
S/N	Displays the serial number of the system
MAC	Displays the MAC address

Table 6-1 Fields and Descriptions for CPU / POWER Settings Panel (Cont.)

Field	Description
IP n	Displays the IP address of NIC1 and NIC2 You cannot change UEIPAC NIC1 or NIC2 IP addresses using PowerDNA Explorer. See Section 5.3.3 for instructions on changing IP addresses for the UEIPAC Intel.
Mode	Displays the current mode of the system: *Initialization*, *Configuration*, *Operation*, or *Shutdown*.

The rest of the panel displays voltage, current, and temperature values as well as other diagnostic information. See Section 4.3 on page 34 for a description of LED states.

This is a RACK-based system so the Power Layer portion of the display shows diagnostic data for the POWER-DC board. Note that UEIPAC XXX-1G Cube-based systems do not have this board and will not show the Power Layer information.
Refer to **Chapter 4** for more information.

6.4 Obtaining a Hardware Report

The hardware report provides diagnostic data, version information, POST results, and more for your UEI system, CPU / POWER board(s), and all installed I/O boards.

To obtain a hardware report, select *View >> Show Hardware Report*. .An example of a hardware report is shown in Figure 6-3.

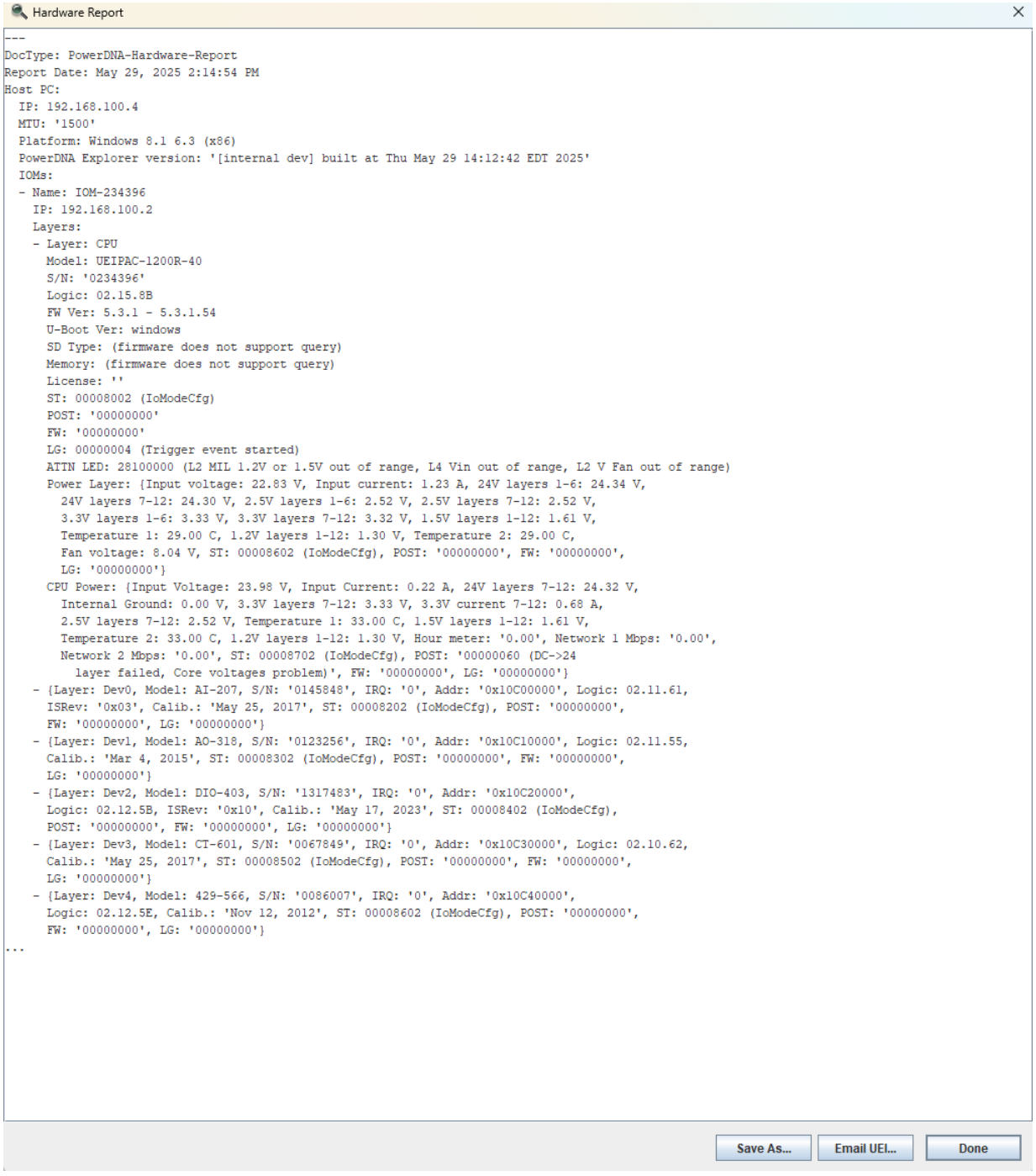

Figure 6-3. Example of a Hardware Report

6.5 Interacting with Input / Output Boards

You can interact with I/O boards to become familiar with their capabilities, verify calibration and manufacturing dates, verify logic versions and device location, and additionally to troubleshoot your application (PowerDNA Explorer can be used to isolate hardware vs programming issues).

Settings available through PowerDNA Explorer will be dependent on the settings specific to each board type.

NOTE: Examples in this section are an introduction to PowerDNA Explorer capabilities; please note PowerDNA Explorer provides a communication link with all types of UEI I/O boards, not just the board-types listed in this section.

6.5.1 Reading Analog Input Channels

This section provides an overview of PowerDNA Explorer settings for analog input boards. Each type of analog input board will have displays specific to the features offered with that board[1]. In this section, we use the AI-207 as an example.

To read analog input data, do the following:

1. Select the name of the analog input board in the Device Tree panel on the left.
2. Click *Network* >> *Start Reading Input Data* (or the **Start Reading Data** button).

After starting the data read, the acquired values for inputs update in the display, as shown in the Voltage column in Figure 6-4. In this example, the AI-207 is connected to a test adapter that drives +7.5 V and -7.5 V on even and odd channels respectively.

1. Refer to board-specific datasheets and manuals to learn more about the capabilities of a particular I/O board.

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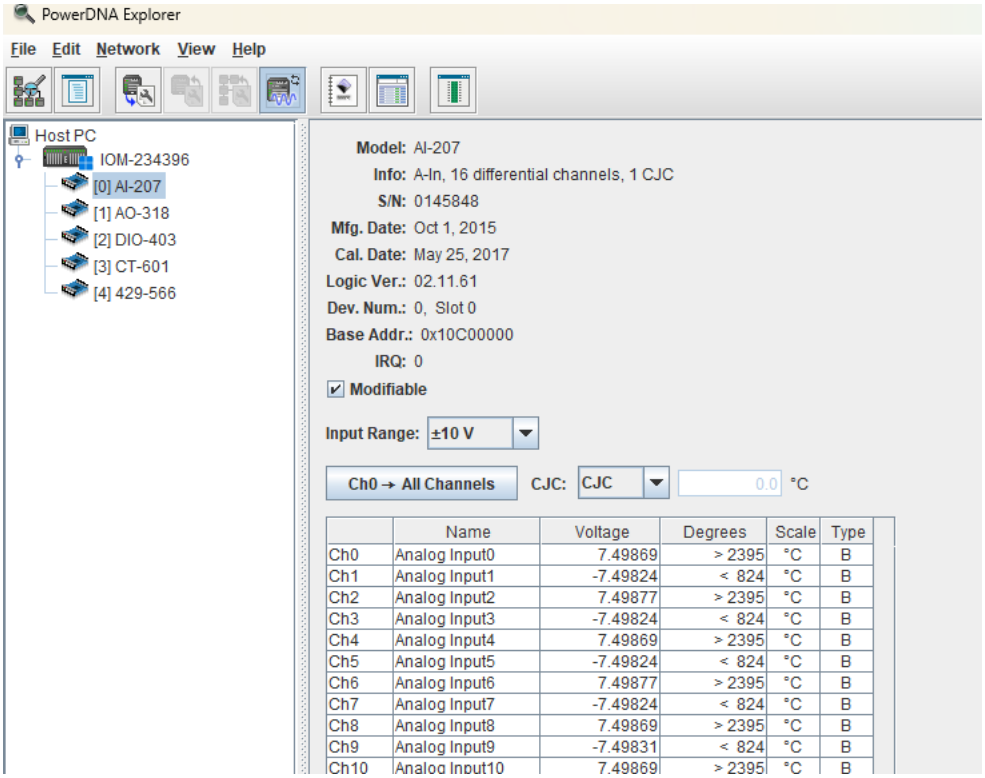

Figure 6-4. Example of Reading Analog Input Data

Each board includes settings unique to its functionality; in the AI-207 example above, users can also configure the input range and select and configure CJC. Refer to board-specific manuals for descriptions of capabilities.

Also in the settings panel, you can add or edit channel names. After editing names, you can choose *Network* >> *Store Config* to save changes to the board. This is true for all boards.

Additionally, if you have changed a configuration value, but have not chosen *Network* >> *Store Config* to save them, previous values can be re-read from the board, using *Network* >> *Reload Config*.

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6.5.2 Writing to Analog Output Channels

This section provides an overview of PowerDNA Explorer settings for analog output boards. Each type of analog output board will have displays specific to the features offered with that board[1]. In this section, we use the AO-318 as an example.

To set analog output levels on an AO-318 channel, do the following:

1. Select the name of the analog output board in the Device Tree panel on the left.
2. Click the **Output** tab (Figure 6-5).
3. Adjust value for the corresponding channel.

NOTE: Use *Network >> Store Config* to save values to the board.

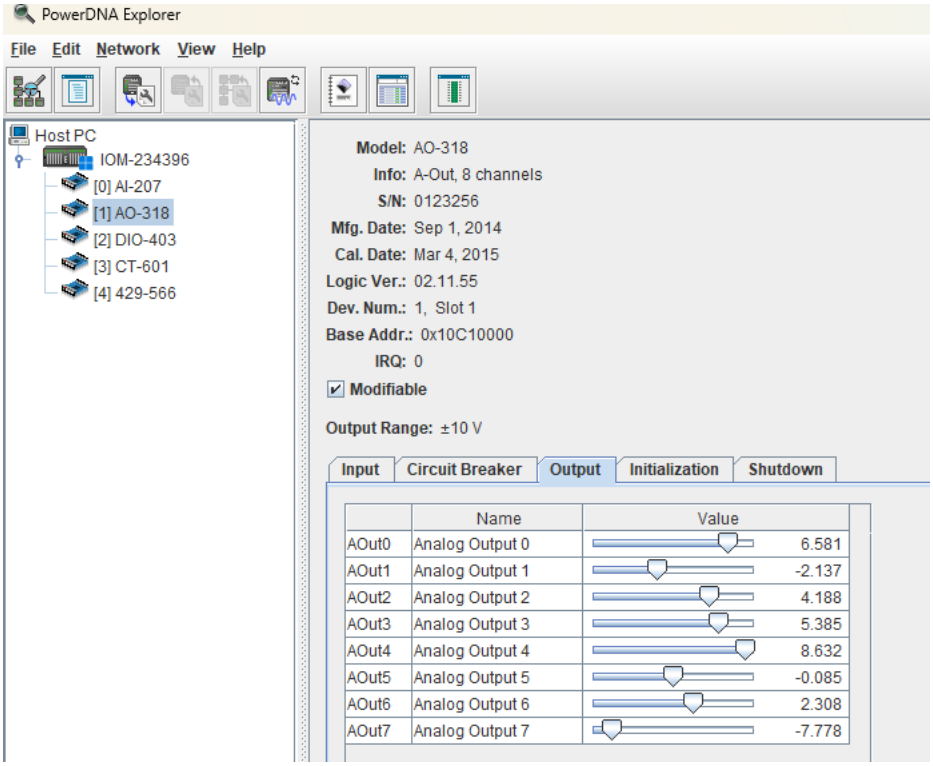

Figure 6-5. Example Writing Output Data using AO-318 Board

The AO-318 PowerDNA Explorer display provides controls for the following:

- Reading diagnostic data (**Input**) (similar to reading input data described in Section 6.5.1)
- Monitoring and controlling circuit breakers (described in Section 6.5.3)
- Changing output levels (**Output** is described above)
- Changing output levels on powerup or shutdown in non-volatile memory (described in Section 6.5.4)

You can then choose *Network >> Store Config* to apply all changes to the board.

1. Refer to board-specific datasheets and manuals to learn more about the capabilities of a particular I/O board.

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6.5.3 Monitoring & Controlling Circuit Breakers

Several of UEI's I/O boards provide circuit breaker functionality[1].

For I/O boards that support circuit breakers on output channels, PowerDNA Explorer allows you to monitor the status of the circuit breakers, configure them, and/or reset them, if needed. In this section, we use the AO-318 as an example.

To monitor the status of circuit breakers on AO-318 channels, do the following:

1. Select the name of the analog output board in the Device Tree panel on the left.
2. Click the **Circuit Breaker** tab (Figure 6-6).

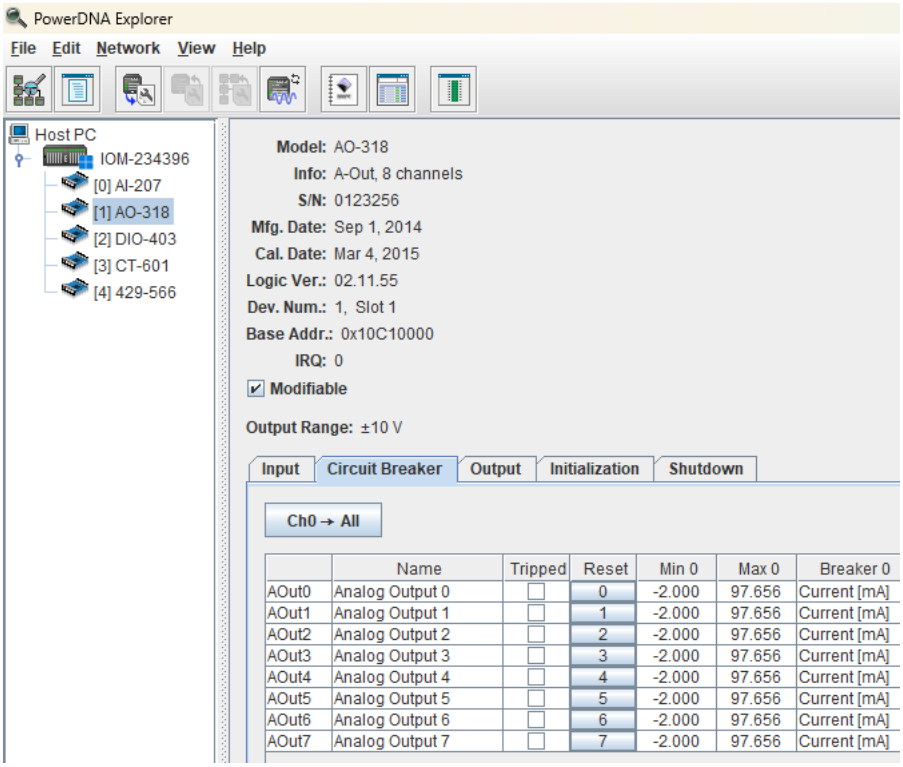

Figure 6-6. Monitoring Circuit Breakers on AO-318 Channels

A tripped breaker displays in the **Tripped** field of the corresponding channel. Once the trip condition is resolved in your hardware setup, users can reset the breaker by clicking the corresponding button in the **Reset** field (circuit breakers are resettable in software via UEI API, as well).

For the AO-318, users can also adjust the trip criteria (current, voltage, temperature, or disabled) and adjust the minimum and maximum trip limits.

1. Refer to board-specific datasheets and manuals to learn more about the capabilities of a particular I/O board.

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6.5.4 Configuring Power-up & Shutdown Output Levels

Default power up and shutdown levels for UEI output boards are configured by UEI at the factory and stored in non-volatile memory[1].

PowerDNA Explorer allows you to change these values and store updates in non-volatile memory, if needed. In this section, we use the AO-318 as an example. Refer to Figure 6-7.

To update initial output voltage on power-up on an AO-318 channel, do the following:

1. Select the name of the analog output board in the Device Tree panel on the left.
2. Click the **Initialization** tab.
3. Adjust the levels in the **Value** field for corresponding channels as needed.
4. Click **Store Configuration** to store values in non-volatile memory.

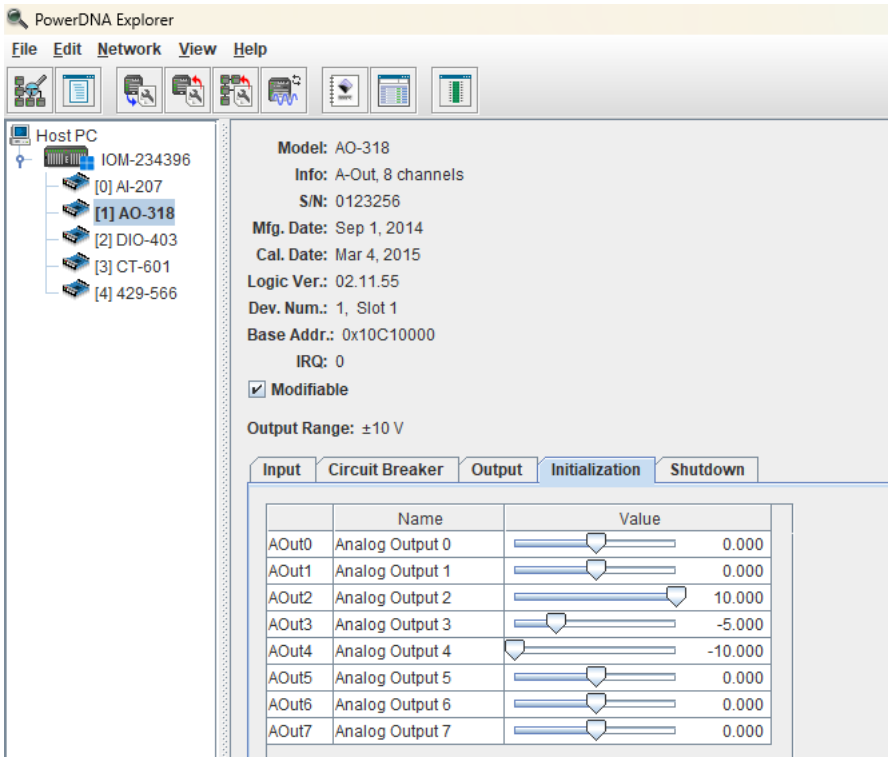

Figure 6-7. Updating Initial Output Level on AO-318 Channels

To update the shutdown values, click the **Shutdown** tab and repeat steps 3 and 4 listed above.

1. Refer to board-specific datasheets and manuals to learn more about the capabilities of a particular I/O board.

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6.5.5 Reading / Writing Digital Input / Output Channels

This section provides an overview of PowerDNA Explorer settings for digital input / output boards. Each type of I/O board will have displays specific to the features offered with that board[1]. In this section, we use the DIO-403 as an example. Refer to Figure 6-8.

The DIO-403 board is a 48-bit DIO board. It is different from other digital I/O boards because it groups 8 DIO pins at a time into 8-bit ports, where six ports are configured to access the 48 DIO pins.

This means that bit 0 in port 0 corresponds to DIO pin 0; bit 1 in port 1 corresponds to DIO pin 9; bit 2 in port 2 corresponds to DIO pin 18, etc.

For the sake of abstraction in PowerDNA Explorer, we'll refer to all ports as channels.

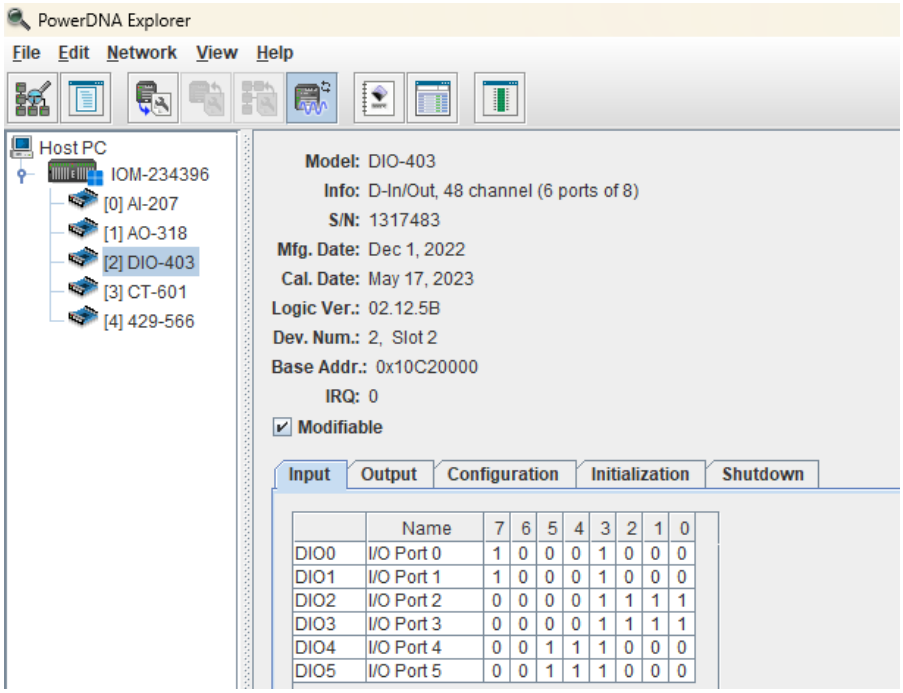

Figure 6-8. Example DIO-403 Inputs

Input/Output/Configuration/Initialization/Shutdown tabs switch between displaying DIO pin reading of input state data, setting DIO output state, configuring DIO as output or input, and settings for initial and shutdown states.

The Input tabs contain the following columns:

- **Name** is the channel (port) name, or a user-defined string.
- **7:0** Input Values consist of 0 or 1 as read from the input pin.

NOTE: Use *Network >> Start Reading Input Data* to see immediate input values in Input tabs.

1. Refer to board-specific datasheets and manuals to learn more about the capabilities of a particular I/O board.

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Use the **Output** tab to set the output value driven from the pin.

The Output tab contains the following columns:

- **Name** is the channel (port) name, or a user-defined string.
- **7:0** Output values consist of the output state to be driven from the I/O pin: select 0 (unchecked) or 1 (checked).

The settings in Figure 6-9 will cause output high values on DIO pin 3, pin 7, pins 24 through 27, and pins 43 through 45. The settings will cause output low values on DIO pins 0 through 2, pins 4 through 6, pins 28 through 31, and pins 40 through 42, and pins 46 and 47.

The rest of the pins are configured as inputs; input vs output configuration is set on the **Configuration** tab.

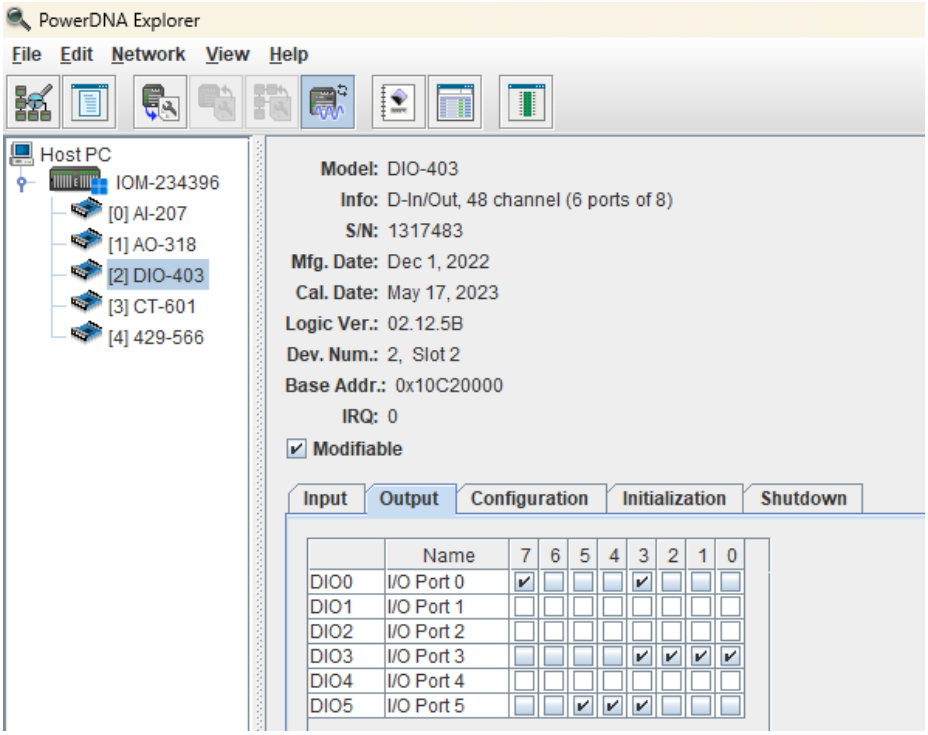

Figure 6-9. Example DIO-403 Outputs

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The **Configuration** tab (Figure 6-10) gets/sets the current input/output directions per port. It contains the following columns:

- **Name** is the channel (port) name, or a user-defined string.
- **In/Out** configures DIO 8-bit ports as inputs or outputs.

Initialization/Shutdown tabs allow you to set initialization and shutdown states on pins, as well as operation mode configuration. They contain the following columns:

- **Name** is the channel (port) name, or a user-defined string.
- **Mode** specifies whether the channel is input or output.
- **7 through 0** contain the values 0 or 1. They are check marks for output channels that allow you to select 0 (cleared) or 1 (selected).

Refer to Section 6.5.4 on page 58 for more information about configuring initialization and shutdown values in non-volatile memory.

NOTE: Use *Network* >> *Store Config* to save values to the board.

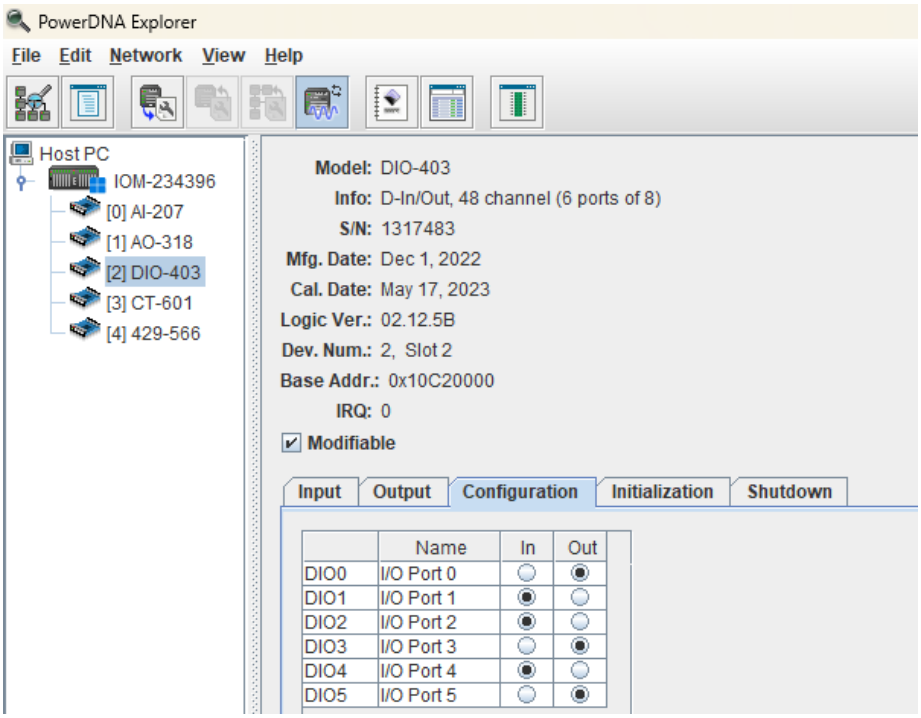

Figure 6-10. Example of DIO-403 Configuration

6.5.6 Configuring & Reading Counter / Timer Board

This section provides an overview of PowerDNA Explorer settings for counter/timer boards. Each type of I/O board will have displays specific to the features offered with that board[1]. In this section, we use the CT-601 as an example. See Figure 6-11

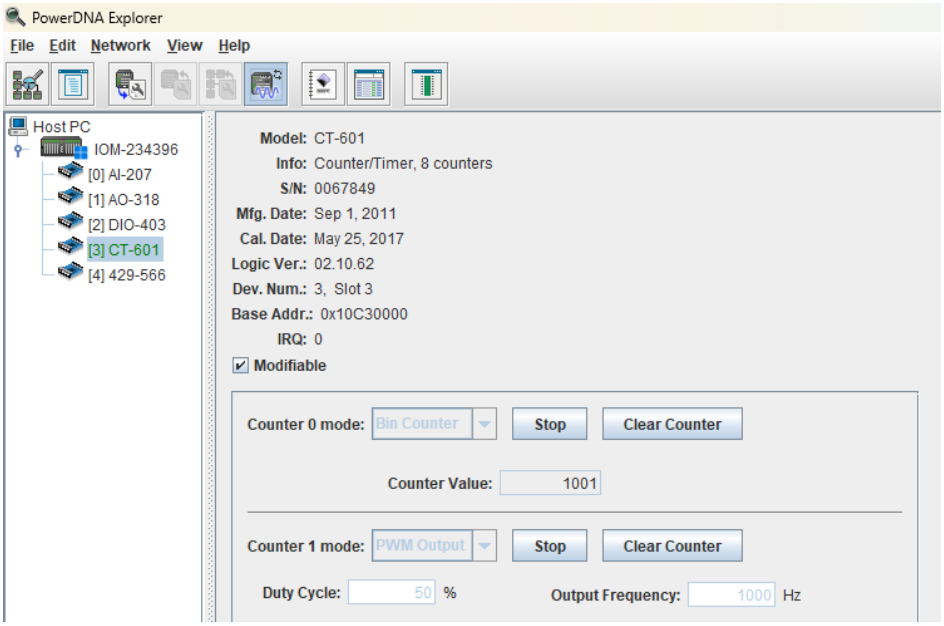

Figure 6-11. Example CT-601 Module

The CT-601 board has 8 counters. Each counter can be set to one of the different modes: Quadrature, Bin Counter, Pulse Width Modulation (PWM), Pulse Period, or Frequency.

When you change the mode of a counter using the mode pulldown menu, the controls for that counter will change to those appropriate for the mode.

After setting the configuration for a counter, you can choose *Network >> Store Config* to store the settings on the device. Clicking the **Start** button will also write your configuration to the board.

Clicking the **Start** button for a counter will start that counter on the board. After clicked, the **Start** button will turn into a **Stop** button, and the other controls for that counter will become disabled until you click **Stop**.

1. Refer to board-specific datasheets and manuals to learn more about the capabilities of a particular I/O board.

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6.5.7 Reading / Writing Messages to / from Serial Boards

For serial I/O boards, PowerDNA Explorer provides the ability transmit serial messages on TX channels (ports) and display serial messages received on RX channels (ports)[1]. This section provides an example of configuring an ARINC 429 board, monitoring receiver input messages, and scheduling transmit output messages.

6.5.7.1 Configuring ARINC RX / TX Ports

You can configure the ARINC 429 board by setting the baud rate and Even/Odd parity under the **Configuration** tab. You can also configure RX filtering by providing a Filter List of labels to accept (only those will display) and specifying an SDI to filter on (only the specified SDI will display). Refer to Figure 6-12.

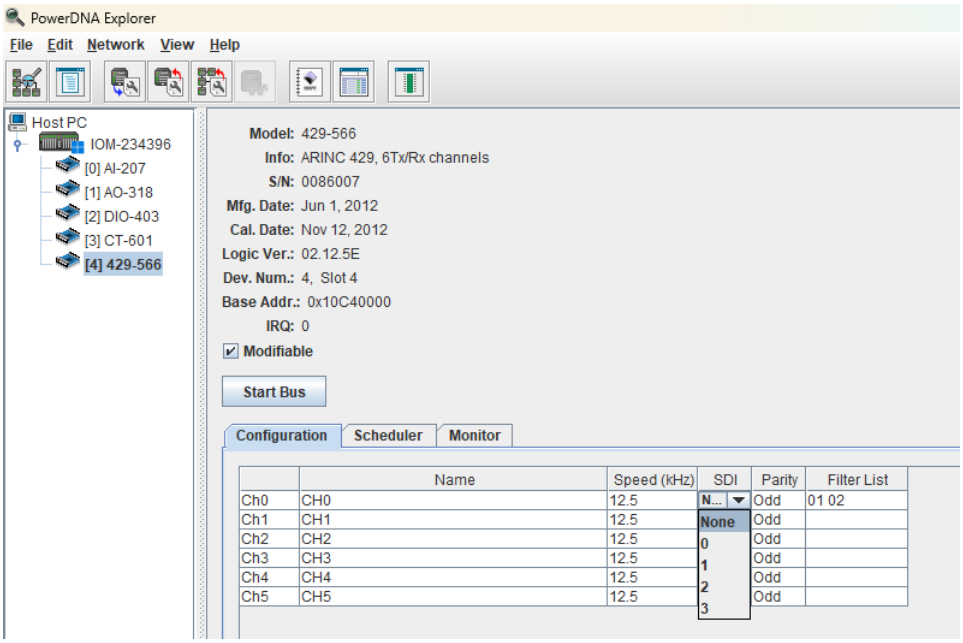

Figure 6-12. Configuring ARINC 429 RX/TX Messages

Note that for this board, the **Configuration** tab is used to set both RX and TX configuration.

1. Refer to board-specific datasheets and manuals to learn more about the capabilities of a particular I/O board.

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6.5.7.2 Receiving ARINC-429 Messages

For reading ARINC RX messages on UEI ARINC 429 boards using PowerDNA Explorer, select the **Monitor** tab as shown in Figure 6-13.

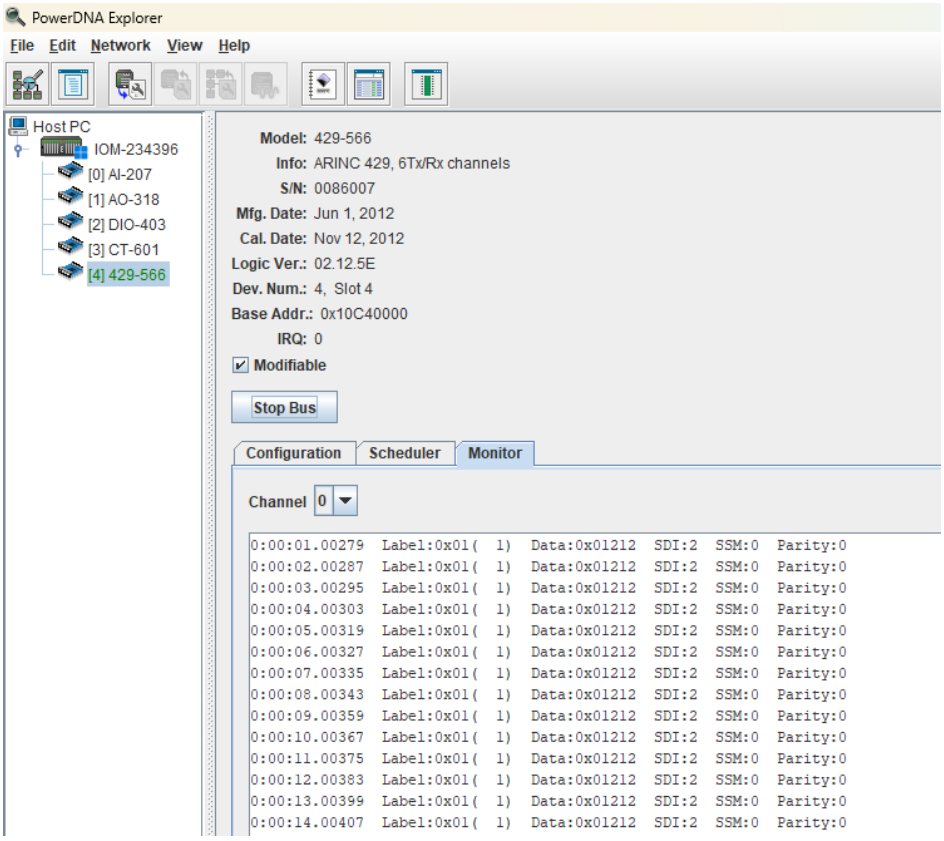

Figure 6-13. Reading ARINC 429 RX Messages

To read RX messages, do the following:

1. Select the name of the ARINC board in the Device Tree panel on the left.
2. Click the **Monitor** tab.
3. Select which Channel (receiver port) you want to read.
4. Click **Start Bus** to start capturing messages, and click **Stop Bus** to stop.

For the ARINC 429-566 board, messages display with a timestamp followed by the ARINC label, data payload, SDI, SSM and parity.

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6.5.7.3 Transmitting ARINC-429 Messages

For scheduling transmit messages over UEI ARINC 429 TX ports, select the Scheduler tab, as shown in Figure 6-14.

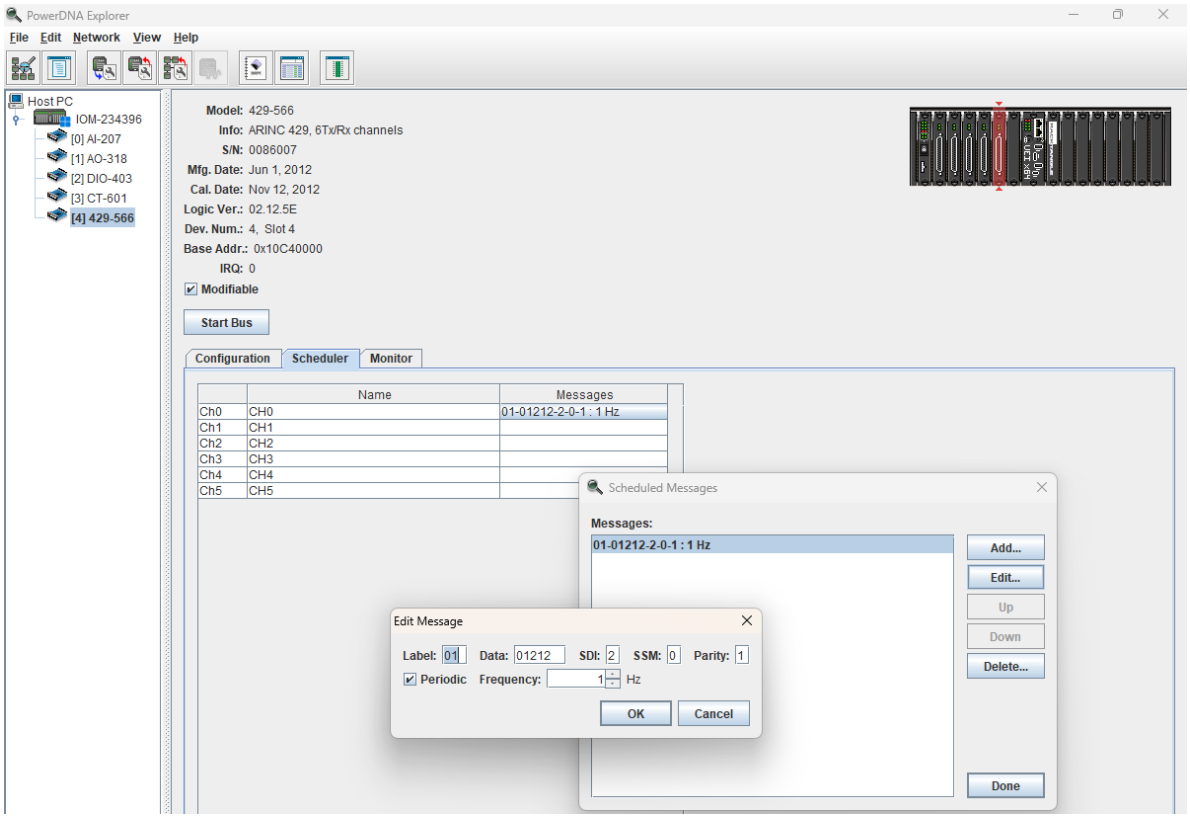

Figure 6-14. Scheduling ARINC 429 TX Messages

To schedule transmit messages, do the following:

1. Select the name of the ARINC board in the Device Tree panel on the left.
2. Click the **Scheduler** tab in the settings panel.
3. Select which channel (transmit port) you want to schedule a message.
4. Double-click the corresponding **Messages** field. A Scheduled Messages window will open.
5. Click **Add** to schedule a new message, or click **Edit** to edit an existing message. An Add/Edit Message window will open.
6. Enter message fields: **Label**, **Data**, **SDI**, **SSM**, **Parity**. Click **Periodic** and enter the **Frequency** to periodically send message (otherwise it will be sent once).
7. Click **OK**, and **Done**.

To start sending messages, click **Start Bus**, and click **Stop Bus** to stop.

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6.6 Displaying Wiring Diagrams for I/O Boards

I/O board pinouts are provided in board-specific manuals and datasheets. Additionally, if you need to probe an output or rewire an I/O board connection, you can directly access the pinout of the I/O board using PowerDNA Explorer.

To view the pinout, do the following:

1. Select the name of the IO board in the Device Tree panel on the left.
2. Select *View* >> *Show Wiring Diagram* (or click the **Show Wiring Diagram** button).

All boards have this feature. The AI-207 wiring diagram is displayed in Figure 6-15 as an example. The wiring diagrams in PowerDNA Explorer match the wiring diagrams in the board-specific datasheets and user manuals.

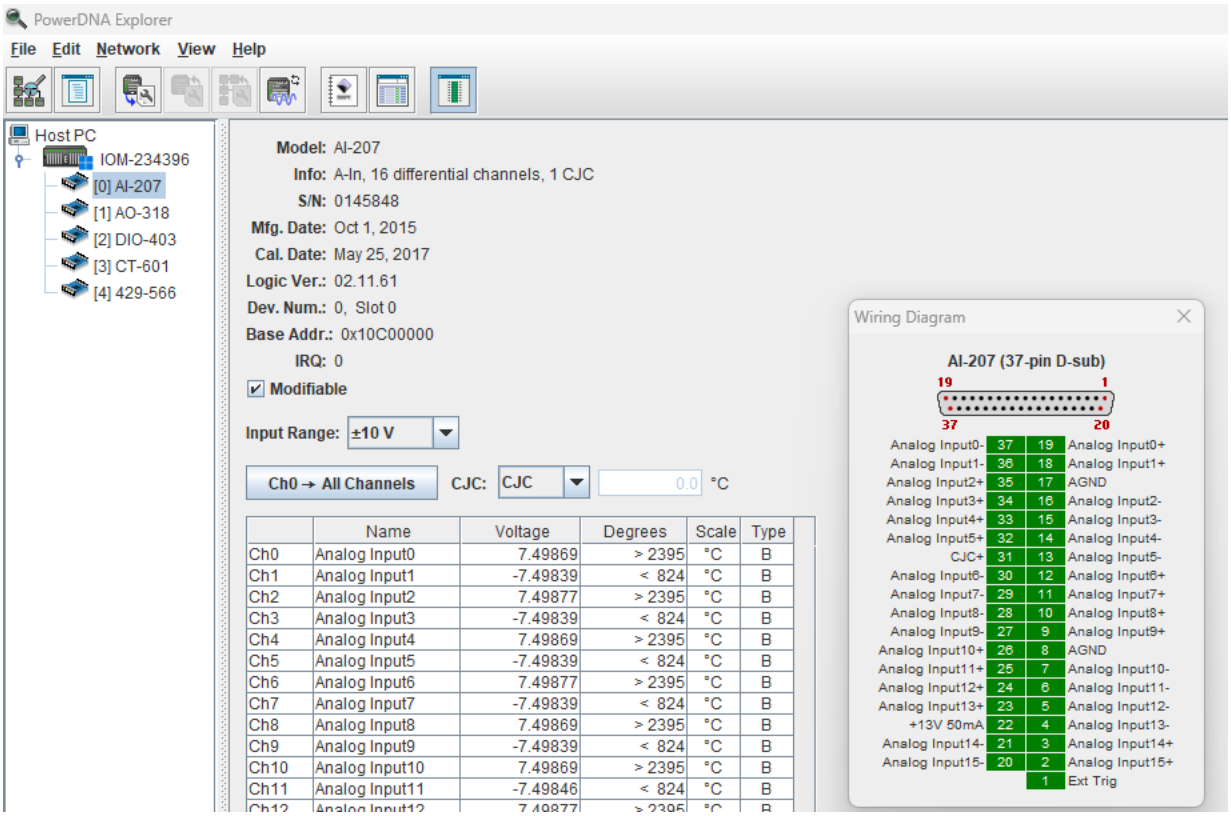

Figure 6-15. Example of a Wiring Diagram Display

6.7 Interacting with Other UEIPACs and UEI Systems

PowerDNA Explorer has the capability of discovering and interacting with other UEI systems (RACKs or Cubes) on a selected network.

Using PowerDNA Explorer, you scan the network, and discovered systems are listed in the left-hand panel (device tree) of the display

In Figure 6-16, the IOM-234396 system is UEIPAC Intel running PowerDNA Explorer. The FV-55 system is an additional UEIPAC system that was discovered during the network scan.

.

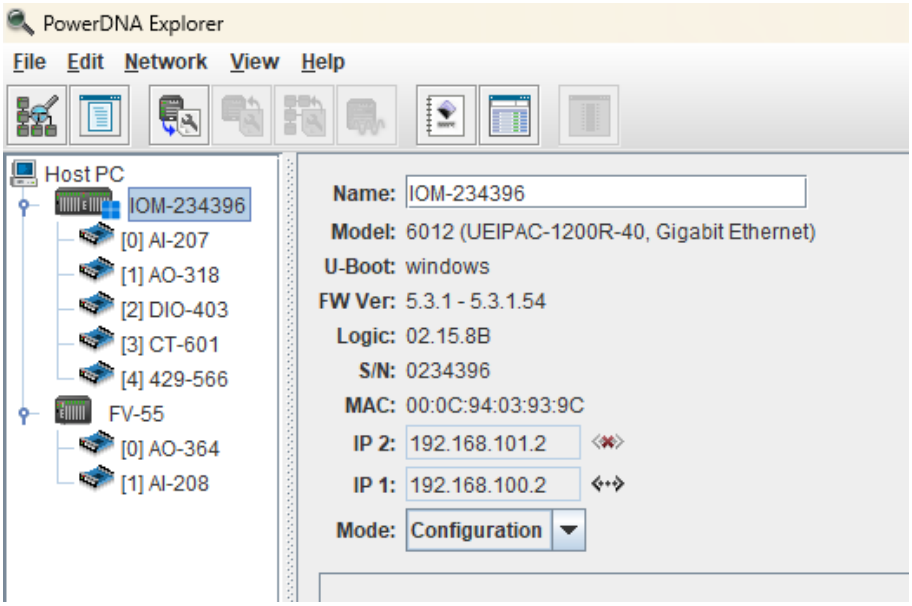

Figure 6-16. Example of Interacting with Multiple UEI Systems

To interact with multiple UEI systems with PowerDNA Explorer, do the following:

1. Select *Network* >> *Address Ranges* to open the Address Ranges dialog (Figure 6-17).

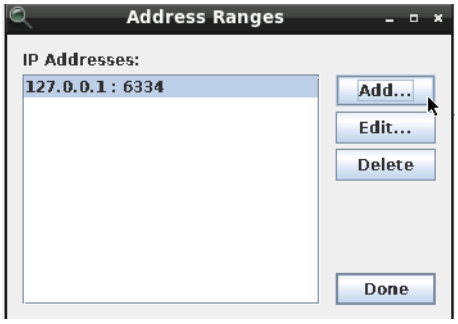

Figure 6-17. Address Ranges Dialog Box

2. Click **Add** to add a new subnet or range or **Edit** to modify an existing range (see Figure 6-18).

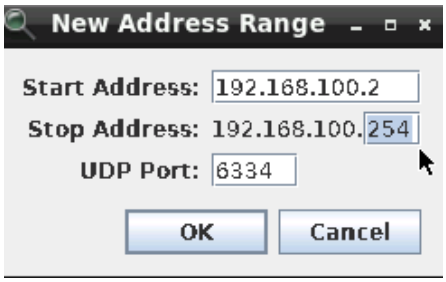

Figure 6-18. Edit Address Ranges Dialog Box

3. Enter range information and click **OK** in the Edit Address Range dialog, and **Done** in the Address Ranges dialog.
4. Scan the network for UEI systems in the newly specified range either by selecting *Network* >> *Scan Network* or clicking the **Scan Network** button (Figure 6-16).

To display pertinent hardware and firmware information about any of the discovered systems, click the system name shown in the Device Tree panel on the left.

To display pertinent information about an I/O board in the system, you can click the I/O board of a specific system and then manipulate its inputs or outputs in the settings panel.

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Appendix A

Field Replacement of Fuses on DNA and DNR Boards

Some boards used in UEI DAQ IO systems require field replacement of fuses when unexpected overloads occur. Locations of these fuses are shown in **Figure A-1** through **Figure A-3**. Part numbers for the replacement fuses are listed **Table A-1**.

Table A-1 DNA/DNR Replacement Fuses

UEI Fuse ID (Board)	Rating	UEI Part No.	Description	Mfr.	Mfr P/N
F1	5A	925-5125	FUSE 5A 125V SLO SMD SILVER T/R	Littlefuse	0454005.MR
F2	5A	925-5125	FUSE 5A 125V SLO SMD SILVER T/R	Littlefuse	0454005.MR
F3 (DC)	5A	925-5125	FUSE 5A 125V SLO SMD SILVER T/R	Littlefuse	0454005.MR
F3 (1GB)	10A	925-1125	FUSE 10A 125V FAST NAN02 SMD	Littlefuse	0451010.MRL
F4	5A	925-5125	FUSE 5A 125V SLO SMD SILVER T/R	Littlefuse	0454005.MR

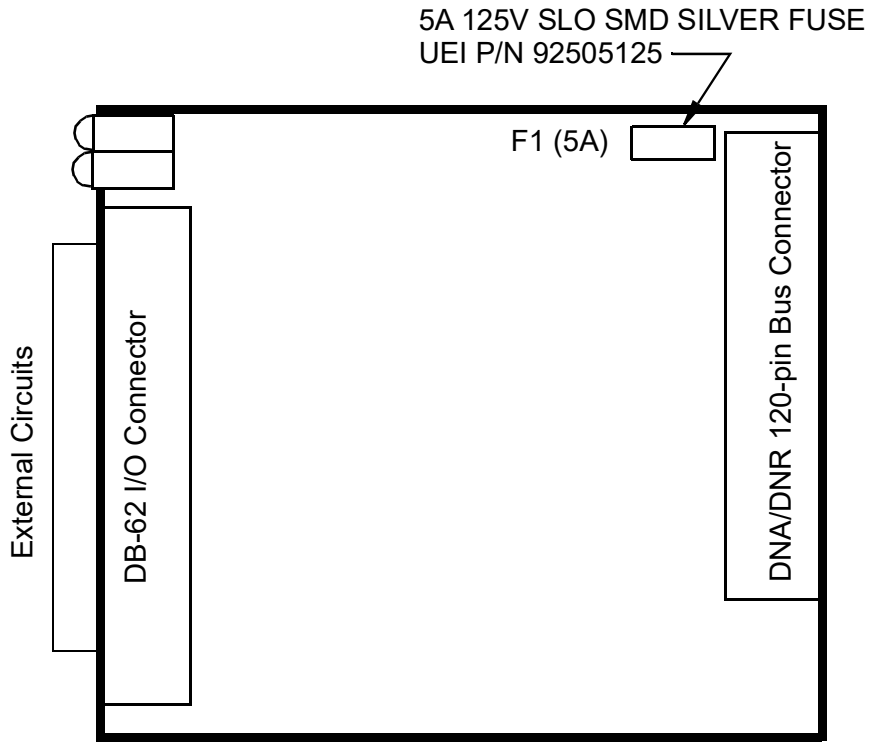

Figure A-1. Location of Fuse for Base Boards Equipped with a Fuse

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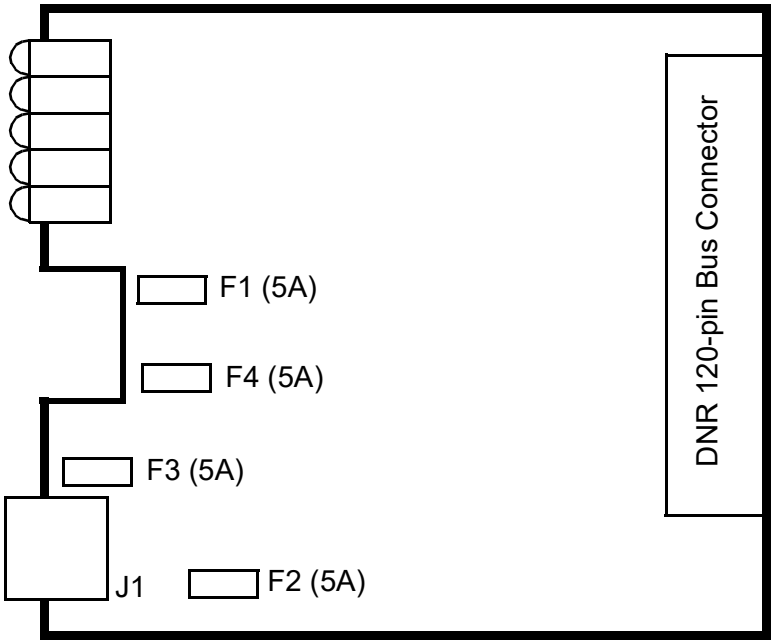

Figure A-2. Location of Fuses for DNR-POWER-DC Board

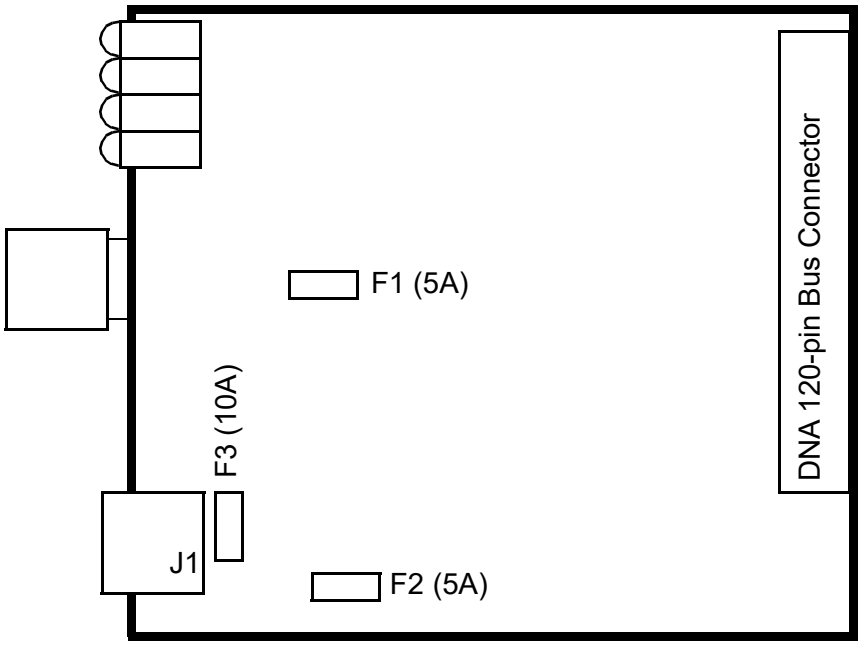

Figure A-3. Location of Fuses for DNx-POWER-1GB Board

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