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Value Written to D/A

# Application Note

TenAsys / INtime plus  
UEI / PowerDNA :  
The perfect match  
for Real Time Simulation

Value Written to D/A

Output Voltage

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Ideal Output

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Value Written to D/A

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**United  
Electronic  
Industries**

Shaping the Future of Computer-Based I/O™

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## Application Note **TenAsys / INtime plus UEI / PowerDNA :** **The perfect match for Real Time Simulation**

Imagine that you are an engineer working for a company, and your job is to develop a UAV. You assemble the parts, program the software, and begin testing the UAV before handing it over to the customer.

Testing the full UAV could be done by a single UAV- operator, who will take a control unit to the airfield and remotely put the UAV into action, fly it, and give you feedback.

Until few years ago, this was the standard practice, but gradually, the maturing UAV industry realized the evident drawbacks of that initial approach: there was always some level of uncertainty whether the tests were complete enough to cover all the situations.

The industry, the developers and the customers demanded a more extensive set of tests prior to the actual tests in the field.

The added tests should give answer to the following:

- The behavior of the UAV under extreme environmental and climate parameters: rain, high temperatures, and wind in varying speeds.
- How does the UAV recover from various fault after fault conditions, how well and how fast the recovery phase is performed?
- How much time the engineering cycle time will take : understanding what was wrong, fixing the design, and rerunning the tests.

Every outdoor test demanded more follow up equipment, cameras, and another flying platform to take the pictures, so added tests in the lab meant significantly reducing the cost of running outdoors.

A new method was invented. It is called HIL — Hardware In the Loop.

In brief: the developed Electronic Control Unit (of the UAV as an example) , that is shown on the right side of figure 1 - is connected in the LAB to an HIL system ( the blue elements on the left of figure 1). These blue parts create a simulated real time environment to the UAV. The UAV sits on the LAB table , connected to the HIL equipment , and the Real Time Processor gives the electronic control unit (in this case of an UAV) the “feeling” that it is flying : The GPS ,the Acceleration ,The Wind and temperature effect – all simulated in Real Time .



Figure 1 : HIL system components

### Building the HIL system

There are few Real Time operating systems which can implement the RT processor on one platform , and there are few Non Real Time Operating systems to implement the operator interface on another platform .

We will describe here a way to partition a single platform to do both. The software is called **INtime for Windows** and is produced by **TenAsys Corporation**.

There are also Various I/O options to connect to the RT system – many vendors, each with its special way of connecting to the RT system and different API “philosophy” to access the specific I/O.

We will describe here an I/O system that supplies all the needed interfaces to the Electronic Unit via one (Ethernet) connection to the RT system, and with a unified Driver “philosophy”. The I/O equipment is called **PowerDNA**, and is produced by **UEI Corporation**.

The overall system architecture described in figure 2.

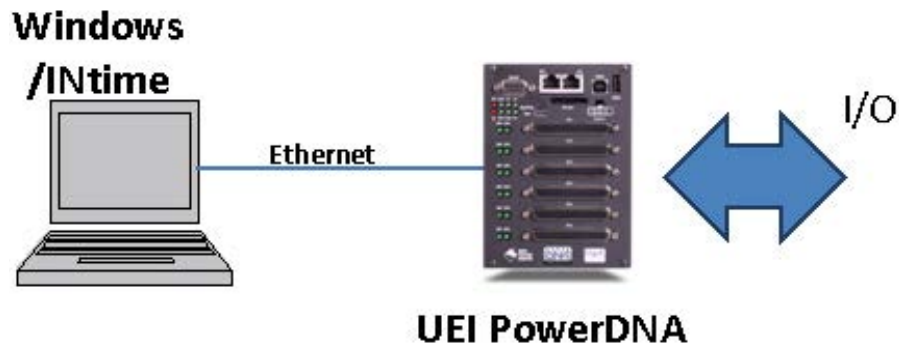


Figure 2: Implementing the HIL system with Windows INtime and PowerDNA

## TenAsys and UEI

TenAsys Corporation ([www.TenAsys.com](http://www.TenAsys.com)) specializes in operating system software for the embedded computer industry, designed and optimized for the Intel x86 platforms. It uses Microsoft Visual Studio as its development environment.

Since 1980, customers worldwide have entrusted TenAsys RTOS products to provide reliable deterministic control in a wide array of mission-critical applications including: medical, telecom, industrial control, robotics, test and measurement, and military applications.

UEI ([www.ueidaq.com](http://www.ueidaq.com)) is a leader in the Ethernet data acquisition and control systems, Data Logger/Recorder, Programmable Automation Controller (PAC) and Modbus TCP for Aerospace, Simulation and Industrial Control markets. The revolutionary PowerDNA/DNR in a “Cube” or “DNR” form factor provides a platform that can also be a compact, rugged that is ideal for applications in the automotive, aerospace, petroleum/refining, simulation, semiconductor manufacturing, medical, HVAC, and power generation fields – and more.

### TenAsys INtime contribution to HIL systems

INtime is a 30 years mature RTOS that works on any X 86 platforms. You can partition the platform between Windows and INtime according to the expected load of each partition. For Example, in a four core platform you can assign one, two or even all four cores to run INtime, each core is loaded with a full RTOS, communicating via very fast and low overhead mechanism with the other cores.

The case where all four cores are assigned to INtime is reserved to cases where maximum Real Time processing performance is needed, or when the operator interface needs to be located remotely from the RT processor. In these cases the operator Interface will run on another Windows-Only platform connected via LAN.

INtime for Windows is accepted widely among HIL builders because of the following reasons:

1. Windows is definitely the most appropriate choice for an operator Interface. Utilizing the same platform for doing also the Real Time portion – make it extremely convenient during development and can lower the cost of the produced system. It is preferred to use one platform rather than two.
2. HIL Simulation is often implemented by several (up to 6) Degrees of freedom algorithm. The typical cycle time of the algorithm is about 1 millisecond, and thus demands very high performance CPU to finish a calculation within one millisecond. The highest end of CPU performance in a PC platform can reach today the mind-boggling number of 40,000 MIPs (Mega Instructions Per Second) and is by far the best cost/performance platform available. On the other hand, you are not always forced to choose the highest performance platform – you can match the jitter and performance needs (depending on your cycle time, and algorithm efficiency) and choose among thousands of lower cost platforms that will match your other needs also: cost, Watt power, physical size etc. INtime is optimized to the X 86 processor family and the PC platform, and can gain from the wealth of choices available as a platform.
3. When developing the Windows portion of the application and the Real Time portion on INtime, the programmer use the same platform and tools to create / debug the application. The major debugging tool is Visual Studio (all versions possible up to VS 2013). There is also possibility to copy/paste code in C or C++ between the two systems' parts, or import external Windows code to INtime - including parts which involve calling to OS API (INtime has also an API compatible with Windows to allow for this ability). The overall development environment is displayed in Figure 3.

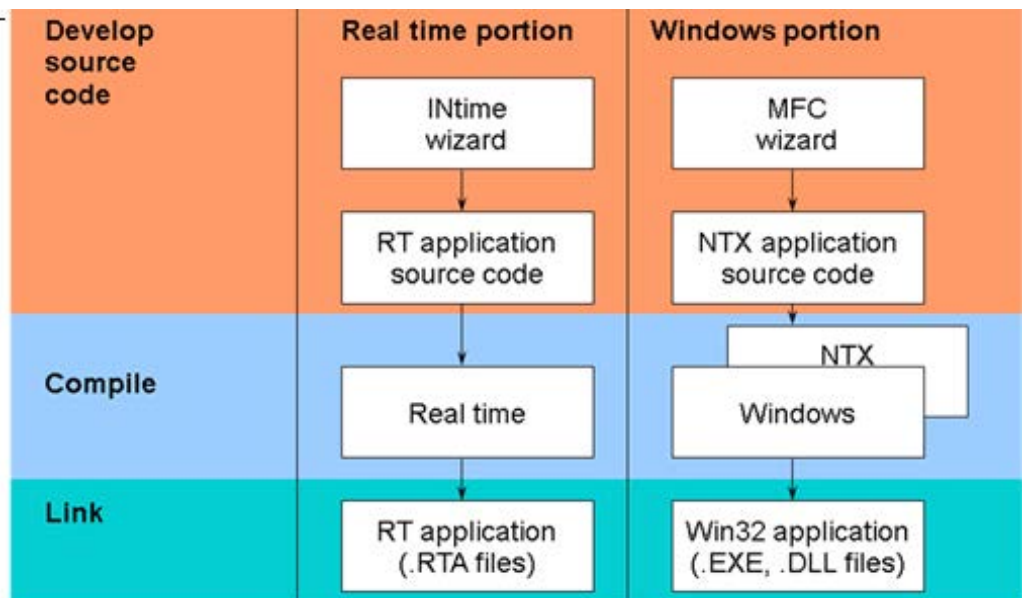


Figure 3 : INtime / Windows development environment

4. During runtime, the designer can balance the two parts of the system by selecting the appropriate number of cores assigned to the real time and non real time parts of the application.
5. Unlike the situation when the two parts of the system reside on a different platform, INtime supply communication speed of hundreds of megabytes per second. This allow advanced graphic updates or fast event log collected - between the two parts



6. There are plenty code examples and documentation supplied with INtime that makes life of the programmer easy. There is also a self training book available for few \$ on Amazon – on Electronic format (<http://www.amazon.com/Real-Time-Development-Theory-Practice-Liming-ebook/dp/B007T2BMH2>)
7. INtime comes with a platform evaluating tool, and Platform Jitter measurement program. Both programs assist the designer to change systems' parameters to minimize jitter, and also make jitter measurements which are displayed as a histogram. Controlling jitter is a key requirement when building a real time system.
8. INtime comes with few advanced debug tools above Visual Studio. The most important tool is a graphic profiler which can display various system events along the Time Axis : Process and thread handles, C language calls , RTOS API calls, and even markers that the programmer can "plant" into his code.
9. UEI equipment is connected via 1 Giga Bit LAN interface (10/100/1000 baseT) to the INtime platform. INtime IP stack is extremely advanced based on BSD Network 7 stack. A Unique feature of INtime stack is its ability to run on each core in parallel to other cores that do the same. Moreover, INtime can work on a Platform without Windows – allowing a Windows operator residing on another platform. Thus multiple configurations are possible based on specific system's requirements. Between INtime nodes themselves, and between INtime and Windows there are few communication mechanisms possible to transfer data , and synchronize events. It is possible to communicate via special objects like shared memory of message queues, or alternatively be parts on the Virtual LAN connection where each core can communicate to its neighbor INtime or Windows core(s) as if they were connected through a physical LAN.

### UEI contribution for HIL system builders

It is obvious that INtime based HIL system can use individual I/O card types to the Electronic Unit under test. However –using UEI Power DNA for I/O gives the designer some unique advantages. Figure 4 shows a 6 slot PowerDNA unit. It is comprised of a base card which runs an RTOS and connects on its one end via Ethernet to the Host (two connections possible), and on its other end it can be connected to 6 Interface cards- each implements a specific protocol. The interfaces are routed through a 37 pin female D-Type connector on the card.



Figure 4 : PowerDNA/DNR ( 6 slot in this example) , and an example of a card (4 Synchronous serial ports)

The possible interfaces (more than 50) are:

- Analog Input
- Analog Output
- Digital I/O
- Communications: Avionics: MIL-1553, ARINC-429, ARINC-708
- Serial: RS-232, RS-422/485 (baud rates up to 4 Mb)
- CAN-Bus
- WIFI and GSM for the UEIPAC
- Counters and Timers
- Frequency generation and measurement
- PWM input and output
- Quadrature encoder inputs
- Power Conversion

Working with PoweDNA , the interface with the Host is done via UDP based protocol (in various “flavors”). The packets are translated into specific I/O commands understood by the PowerDNA.

On the Host - all the remote interfaces look very similar, thus when you are accustomed to work with one interface, it is very easy to learn how to work with all other interfaces.

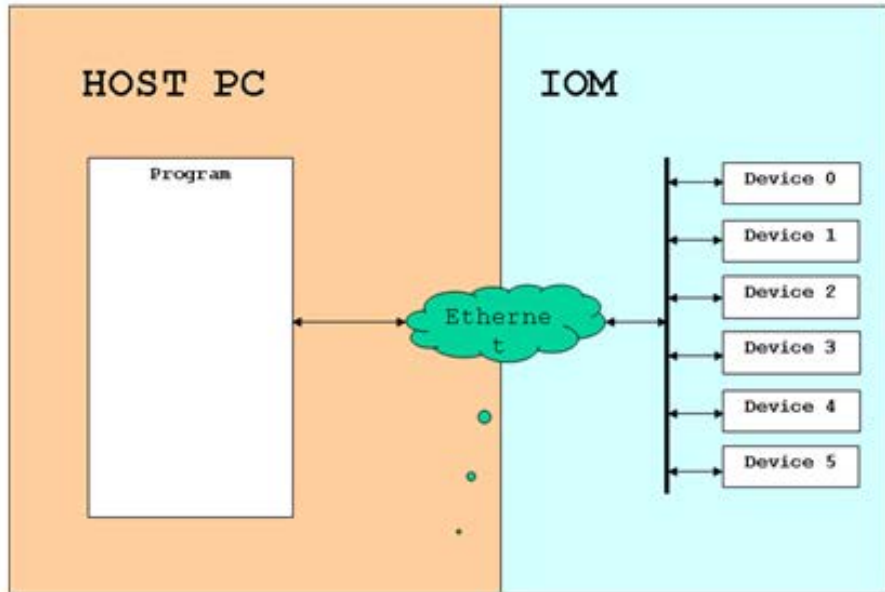
As mentioned before – in order to achieve the maximum efficiency (in term of cycle speed , latency ,and jitter) – few modes of operations are offered .

The list of modes is :

- Immediate I/O
- RTDMap –
- RTVMap –
- Asynchronous
- DqEngine + ACB
- DqEngine + Dmap
- DqEngine + Messaging

It is out of the scope of this article to explain the subtleties of each mode of operation, and where it is best suited. Figure 5 sketches two of the more popular modes for RTOS usage: DMAP—Fixed mapping the PowerDNA into the Host memory and VMAP—Variable length mapping of the PowerDNA into FIFO on the Host.

# RTDMAP



# RTVMap

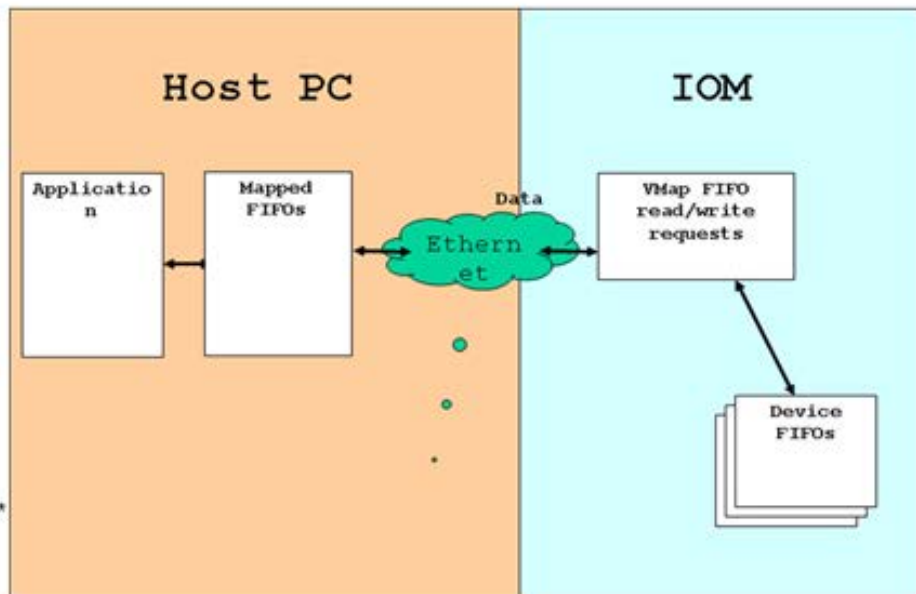


Figure 5 : DMAP and VMAP

The modes differ in the way the UDP based communication is happening to update each side (the Host side and the PowerDNA side) .

The API to access the specific interface is very similar or even identical among Modes of Operation.

Choosing the PowerDNA to implement the I/O portion of the HIL system gives the designer the following advantages:

- For all RTOS drivers, and also for INtime rivers – the coverage interface types by PowerDNA is the most complete. If later into the project you realize that you need to add a new type of interface– you are most likely be able to continue using PowerDNA with a new card type.
- In the conventional Interface cards on the host you have to purchase an appropriate PC platform with the proper number of Slots and proper Interrupts assignments because it is required that RTOS and Windows won't share an interrupt . Not all of Motherboard/BIOS manufacturers can meet the interrupt assignment requirement. When you use PowerDNA – you only need a single Ethernet connection which is always available and its interrupt is typically an MSI interrupt that is not shared. The INtime Ethernet driver is supplied with the product.
- Unlike the case where you work with various PCI card interface manufacturers - Writing application software that work with several interfaces is much easier with the PowerDNA. There are source code examples for every card and every mode of operation.
- UEI is committed to support the Hardware and software for 10 years after an- nouncement of End of Life. This is much better than working with various vendors who often change the design of a board or declare End Of life of a board very short time after you purchased the board. Working mainly with the Military and industrial markets, UEI acknowledges the need for this level of support while the alternative manufacturers who have the right card and right driver are often centralized in the commercial market, and are not “built” for long term support.
- Being very active in the military market – all PowerDNA components are supplied in a ruggedized version. This reduces the cost of adapting an existing design to be use in field or flight tests. Choosing UEI equipment makes your LAB solution be more reliable.
- When using both PowerDNA and INtime - you can expand the HIL solution in many directions :
  - o Choose a bigger UEI chassis with more slots for interface cards. There are chassis for 3,6 or 12 I/O slots.
  - o On a multicore CPU, INtime can run its IP stack on each core, and inter- face to the “world” via another Ethernet port. This way you can work with several PowerDNA boxes – each connected to another Ethernet connec- tion. The interaction of the software between cores can be done up to tens of Megabytes per second via Virtual Ethernet Ports, or choose INtime Message Queue or shared memory connection if the speed approaches hundreds of megabytes per seconds. Some of the possible configurations are shown in Figure 6.





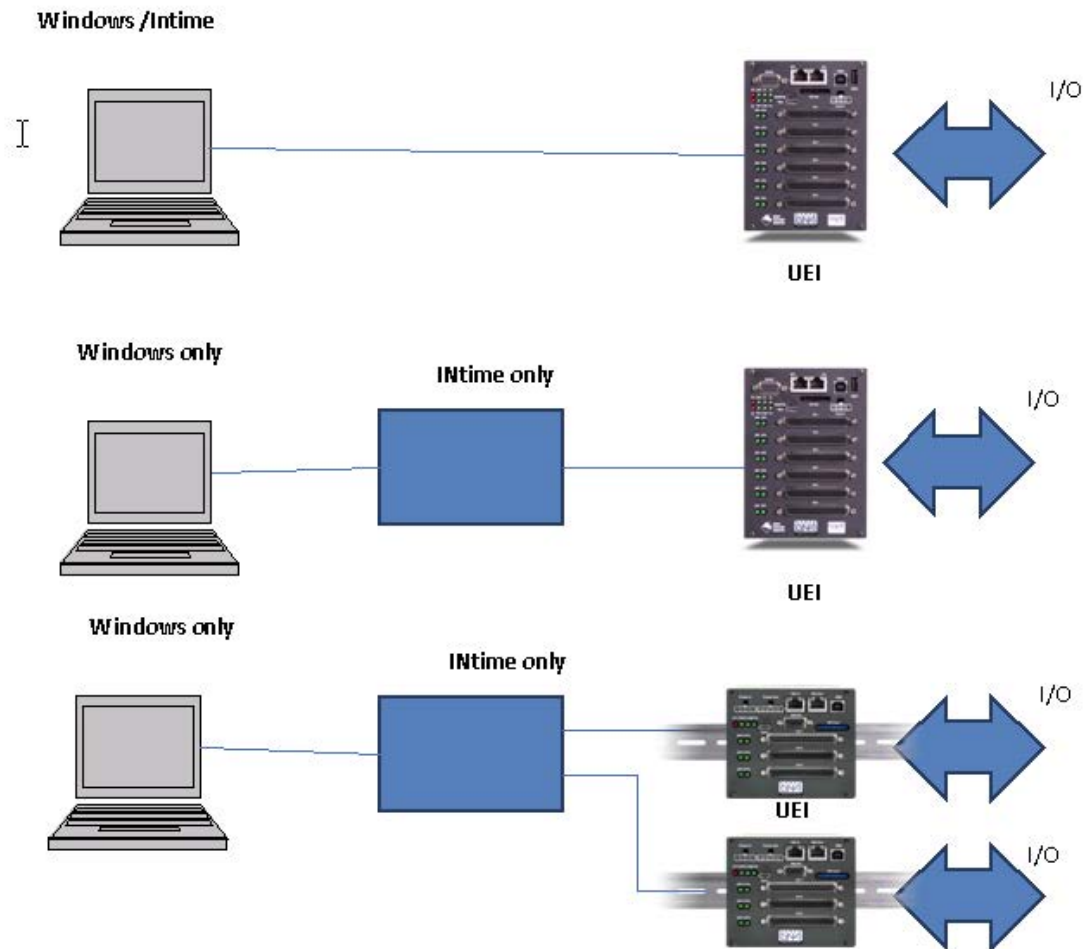


Figure 6 : Some possible INtime / PowerDNA configurations

## Summary

It is often the case when two vendors excel in their own market, but when they combine their solutions they excel even more. This is the case for PowerDNA/INtime solution. INtime IPstack is superior among other RTOS, and the fact that PowerDNA is heavily dependent on the Host Stack makes the combined solution “shine” even more.

We saw few cases where HIL developers previously worked with other RTOS and moved to INtime after acknowledging its superiority. These customers started using individual Interface cards for that solution. However some of them were convinced to replace their individual card solutions and started to work with Power DNA .We approached them and they summarized their experience as “extremely satisfied – easy programming, reliable solution and high functionality for all interfaces”.

These statements are very true for the HIL system market – but are also true elsewhere where similar requirements from the developed product apply.