



DNA-PPCx-1G & UEINet PowerDNA® Gigabit Ethernet I/O Cube User Manual

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PN Man-DNA-PPCx-1G

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Contacting United Electronic Industries

Mailing Address:

27 Renmar Avenue
Walpole, MA 02081
U.S.A.

For a list of our distributors and partners in the US and around the world, please contact a member of our support team:

Support:

Telephone: (508) 921-4600

Fax: (508) 668-2350

Also see the FAQs and online “Live Help” feature on our web site.

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Chapter 1 Introduction

This document describes the features, performance specifications, and operating functions of the PowerDNA[®] DNA-PPCx-1G Gigabit Ethernet Cube data acquisition systems:

- UEINet[™] (single I/O board system)
- DNA-PPC5-1G (up to 3 I/O board system)
- DNA-PPC8-1G (up to 6 I/O board system)
- DNA-PPC9-1G (up to 7 I/O board system)

All systems are designed for use with a Gigabit Ethernet 1000Base-T communication network.

This chapter provides the following information:

- Organization of This Manual (Section 1.1)
- Manual Conventions (Section 1.2)
- Product Versions (Section 1.3)

1.1 Organization of This Manual

This *DNA-PPCx-1G User Manual* is organized as follows:

- **Chapter 1 – Introduction**
This chapter describes the organization of the document and the conventions used throughout the manual.
- **Chapter 2 – PowerDNA 1G Cube System Description**
This chapter provides an overview of our 1G Cube systems (DNA-PPCx-1G / UEINet), component modules, features, accessories, and a list of all items you need for initial operation.
- **Chapter 3 – Installation and Configuration**
This chapter summarizes the recommended procedures for installing, configuring, starting up, and troubleshooting a PPCx-1G system.
- **Chapter 4 – PowerDNA Explorer for the PPCx-1G**
This chapter provides an introduction to the menus and screens of UEI's GUI-based communication application, PowerDNA Explorer.
- **Chapter 5 – Programming CPU Board-specific Parameters**
This chapter describes tools and facilities used for reading and writing CPU board parameters.
- **Appendix A – Configuring Additional Ethernet Cards**
This appendix describes procedures for installing and configuring Ethernet cards for use with Windows operating systems.
- **Appendix B – Field Replacement of Fuses**
- **Index**
This is an alphabetical listing of topics covered in the manual, identified by page number.



1.2 Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:



Tips are designed to highlight quick ways to get the job done, or reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.



CAUTION! *advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

Text formatted in **bold** typeface generally represents text that should be entered verbatim. For instance, it can represent a filename, as in the following example: “You can instruct users how to run setup using **setup.exe** executable.”

Bold typeface will also represent button names, as in “Click **Scan Network**.”

Text formatted in `fixed` typeface generally represents commands, source code, or other text that should be entered verbatim into the source code, initialization, or other file or at a command prompt.

Before you begin:



Before plugging any I/O connector into the Cube or Board, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

Usage of Terms



Throughout this manual, the term “Cube” and/or “DNA-PPCx-1G” refers to all PowerDNA Gigabit Ethernet Cube products:

- UEINet (-00/-01), DNA-PPC5-1G, DNA-PPC8-1G, DNA-PPC9-1G
- UEINet-02, DNA-PPC5-1G-02, DNA-PPC8-1G-02, DNA-PPC9-1G-02
- UEINet-03, DNA-PPC5-1G-03, DNA-PPC8-1G-03, DNA-PPC9-1G-03

Differences between product versions are noted on the following page.

Note that the -02 Cube version is a fully compatible upgrade of the -00/-01 Cube version.



1.3 Product Versions

This user manual provides documentation for the following product versions of the PowerDNA Gigabit Ethernet Cube:

- Cube with 1 I/O board: UEINet, UEINet-02, UEINet-03
- up to 3 I/O boards: DNA-PPC5-1G, DNA-PPC5-1G-02, DNA-PPC5-1G-03
- up to 6 I/O boards: DNA-PPC8-1G, DNA-PPC8-1G-02, DNA-PPC8-1G-03
- up to 7 I/O boards: DNA-PPC9-1G, DNA-PPC9-1G-02, DNA-PPC9-1G-03

Differences in -00/-01, -02, and -03 Cube versions are summarized in **Table 1-1**. Refer to the following chapters in this manual for detailed descriptions.

Item	Summary of Features
DNA-PPCx-1G UEINet (-00/-01)	<ul style="list-style-type: none">• 10/100/1000Base-T Ethernet interface• Freescale MPC8347 CPU• 1PPS synchronization support¹• 128 MB RAM²• 32 MB flash memory²
DNA-PPCx-1G-02 UEINet-02	<ul style="list-style-type: none">• 10/100/1000Base-T Ethernet interface• Freescale MPC8347 CPU• 1PPS/IEEE-1588 synchronization support¹• Optional solid-state hard drives³• 256 MB RAM²• 32 MB flash memory²
DNA-PPCx-1G-03 UEINet-03	<ul style="list-style-type: none">• 10/100/1000Base-T Ethernet interface• Freescale MPC8347E CPU, (encryption-ready / IPSec support pending)• 1PPS/IEEE-1588 synchronization support¹• Optional solid-state hard drives³• 256 MB RAM²• 128 MB flash memory²

Table 1-1 Summary of DNA-PPCx-1G / UEINet CPU Versions

1. 1PPS and IEEE-1588 synchronization support is described in the *PowerDNx 1PPS Sync Interface Manual*.

2. RAM and flash memory are not user-accessible for PowerDNA applications (hosted deployment). Portions of RAM and flash are available for UEIPAC-based systems (stand-alone deployment). See UEIPAC documentation for more information.

3. On UEIPAC-based systems (stand-alone deployment), solid state drives are used for data and/or root file system storage. See UEIPAC documentation for more information.

NOTE: The -02 version of the CPU board is a fully compatible upgrade of the -00/-01 CPU board version.



Chapter 2 The PowerDNA DNA-PPCx-1G Cube System Description

This chapter provides the following information about the PowerDNA DNA-PPCx-1G and UEINet systems:

- PowerDNA Gigabit Ethernet Cube Overview (Section 2.1)
- Specifications (Section 2.2)
- Key Features (Section 2.3)
- PowerDNA DNA-PPCx-1G Cube Enclosure (Section 2.4)
- Front Panel Ports, Connections & LEDs (Section 2.5)
- PowerDNA CPU/POWER Core Module (Section 2.6)
- PowerDNA I/O Boards (Section 2.7)

2.1 PowerDNA Gigabit Ethernet Cube Overview

The UEI PowerDNA DNA-PPCx-1G and UEINet Cube products are Gigabit Ethernet Cube versions of our Ethernet-based data acquisition systems. Each DNA-PPCx-1G and UEINet Cube houses a data acquisition system in a Cube chassis that can accept a set of user-selected I/O boards:

- UEINet accepts 1 user-selected I/O board
- DNA-PPC5-1G accepts up to 3 user-selected I/O boards
- DNA-PPC8-1G accepts up to 6 user-selected I/O boards
- DNA-PPC9-1G accepts up to 7 user-selected I/O boards

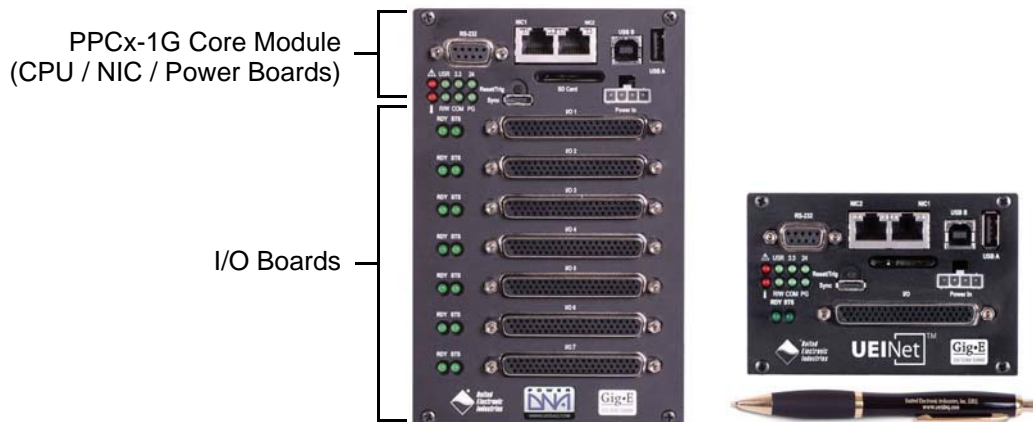


Figure 2-1. UEI PowerDNA DNA-PPC9-1G & UEINet Systems

NOTE: As an option for rackmount solutions, up to 4 Cube systems can be mounted in UEI's DNA-19RACKW accessory assembly.



A standard PowerDNA Cube consists of the following modules:

- One Cube enclosure (UEINet or DNA-PPC5-1G, DNA-PPC8-1G, DNA-PPC9-1G)
- One DNA-PPC-1GB CPU module (top slot)
- One DNA-POWER-1GB DC power module (second slot)
- Selection of DNA I/O boards
- DNA-IO-FILLER panels (one for each unused I/O slot)
- DNA-PSU-24-100 100-Watt, 120/230 VAC to +24VDC External Power Supply with cable and Molex connector

To configure a complete data acquisition system, specify up to 7 DNA I/O boards for installation into your Cube enclosure. I/O boards may be specified in any combination of UEI's DNA I/O boards.

NOTE: For detailed descriptions of all I/O boards and accessories available for DNA-PPCx-1G and UEINet Cubes, refer to www.ueidaq.com.



UEI stand-alone systems (UEIPAC, UEISIM, UEIModbus, and UEIOPCUA deployments) are also available for use with PowerDNA Gigabit Cube systems:

- UEIPAC XXX-1G - Programmable Automation Controller
- UEISIM XXX-1G - Simulink / Simulink Coder Target
- UEIModbus XXX-1G - Modbus TCP-based Controller
- UEIOPCUA XXX-1G - OPC-UA Server, accessed by any OPC-UA client



2.2 Specifications

Figure 2-2 lists the technical specifications for the DNA-PPCx-1G cubes.

Standard Interfaces	
Gigabit Ethernet	Two independent 1000/100/10Base-T interfaces, each with a unique IP address (connected via standard RJ-45 connectors)
USB 2.0	not supported in DNA-PPCx-1G Cubes
Config/General	RS-232, 9-pin "D"
Sync	Custom cable to sync multiple cubes
I/O Slots Available	
UEINet	1 slot (4.0" x 4.1" x 2.7")
DNA-PPC5-1G	3 slots (4.0" x 4.1" x 4.0")
DNA-PPC8-1G	6 slots (4.0" x 4.1" x 5.8")
DNA-PPC9-1G	7 slots (4.0" x 4.1" x 6.6")
Host Communications	
Distance from host	100 meters max, CAT5+ cable
Ethernet data transfer rate	20 megabyte per second
Analog data transfer rate	>6 megasample per second. Capable of sustained transfer of any cube configuration
DMAPI I/O mode	update 1000 I/O channels (analog and/or digital) in less than 1 millisecond, guaranteed
Processor	
CPU	Freescale 8347 series, 400 MHz, 32-bit (8347E optional)
Memory	128 MB (not including on-board Flash)
Status LEDs	Attention, Read/Write, Power, Communications Active
Environmental	
Temp (operating)	Tested to -40 °C to 70 °C
Temp (storage)	-40 °C to 85 °C
Humidity	0 to 95%, non-condensing
Vibration	
(IEC 60068-2-64)	10–500 Hz, 3 g (rms), Broad-band random
(IEC 60068-2-6)	10–500 Hz, 3 g, Sinusoidal
Shock	
(IEC 60068-2-27)	100 g, 3 ms half sine, 18 shocks at 6 orientations; 30 g, 11 ms half sine, 18 shocks at 6 orientations
Altitude	70,000 feet, maximum
MTBF	160,000 hours
Power Requirements	
Voltage	9 - 36 VDC (AC adaptor included)
Power Dissipation	8 W at 24 VDC (not including I/O boards)

Figure 2-2. Technical Specifications



2.3 Key Features

The following table is a list of key features of the DNA-PPCx-1G cubes.

<p>Easy to configure and deploy</p> <ul style="list-style-type: none"> ● Over 70 different I/O boards available ● Built-in signal conditioning ● Gigabit Ethernet based (100/10Base-T compatible) ● Flange kit for mounting to wall/flat surface ● DIN rail and Rack Mount kits ● Standard "Off-the-shelf" products and delivery <p>True Real-time Performance</p> <ul style="list-style-type: none"> ● 1 msec updates guaranteed with 1000 I/O ● Up to 6 million samples per second ● Use QNX, RTX, VxWorks <p>Flexible Connectivity</p> <ul style="list-style-type: none"> ● Dual 1000Base-T Gigabit Ethernet ports with independent IPs ● Dual USB 2.0 controller ports (not supported in PowerDNA deployments) ● 10/100Base-FX Fiber interface available (see DNA-FPPC family) ● Supports WIFI / GSM / Cell networks <p>Compact Size:</p> <ul style="list-style-type: none"> ● 4.1" x 4" x 6.6" Cube holds 7 I/O boards ● 4.1" x 4" x 5.8" Cube holds 6 I/O boards ● 4.1" x 4" x 4.0" Cube holds 3 I/O boards ● 4.1" x 4" x 2.7" Cube holds 1 I/O board ● up to 175 analog inputs per cube ● up to 224 analog outputs per cube ● up to 336 digital I/O bits per cube <p>Rugged and Industrial:</p> <ul style="list-style-type: none"> ● All Aluminum construction ● Operation tested from -40°C to 70°C ● Vibration tested to 3 g, (operating) ● Shock tested to 100 g, (operating) ● All I/O isolated from Cube and host PC ● Operation to 70,000 feet <p>Outstanding Software support</p> <ul style="list-style-type: none"> ● Windows, Linux, RTX, VxWorks and QNX operating systems ● VB, VB .NET, C, C#, C++ ● MATLAB, LabVIEW, OPC, ActiveX support
--

Figure 2-3. Product Features



2.4 PowerDNA DNA-PPCx-1G Cube Enclosure

The cube enclosure is a rigid, extruded aluminum, mechanical structure with complete EMI shielding. Unused slots are filled with blank filler panels.

The DNA-PPCx-1G cube enclosure houses the following components:

- One DNA-PPC-1GB CPU module (slot 1)
- A DNA-POWER-1GB DC/DC power module (slot 2)
- PowerDNA I/O boards (slot 3 through slot 9, where the number of supported boards depends on the product version)
- Blank filler panels for unused slots
- Up to two 8-volt cooling fans mounted on the rear cover of the cube

Behind the faceplate, the Power / CPU / IO board stack is positioned in the cube chassis on grooved guides.

The DC power module provides output voltages of 24, 3.3, 2.5, 1.5, and 1.2 VDC for the logic/CPU and 8 VDC to power the cooling fans.

2.4.1 Fans & Air Flow

Figure 2-4 shows a representation of air flow through the PowerDNA cube.

Air is drawn into the rear of the enclosure, routed forward over the electronic circuit boards, up to the top of the enclosure, and then out the top rear of the enclosure. The system is designed to maintain positive pressure cooling within the enclosure at all times.

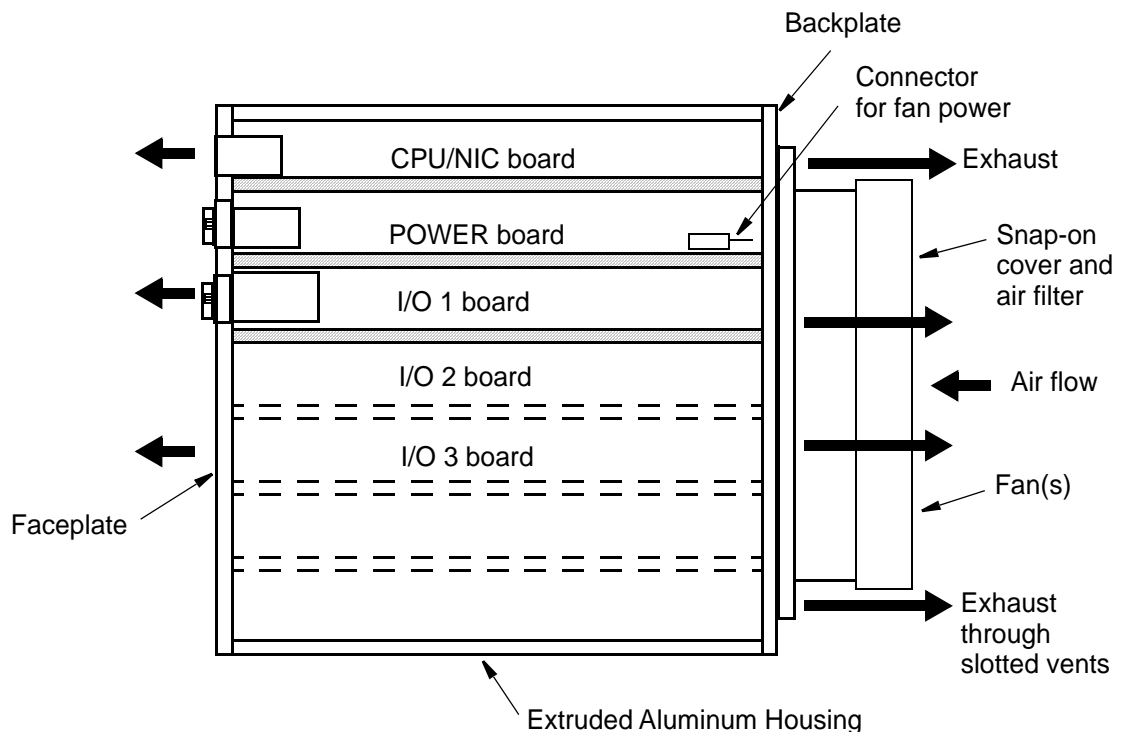


Figure 2-4. Air Flow through PowerDNA Cube

A temperature sensor mounted on the POWER board above the CPU monitors temperature within the cube. The system turns on the fan(s) if the temperature exceeds 45° C and shuts down power to the cube if a high limit is exceeded.



2.5 Front Panel Ports, Connections & LEDs

The ports and LEDs of the CPU / Power core module are illustrated in Figure 2-5 and described in **Table 2-1**.

A block diagram of the DNA-PPCx-1G core and additional descriptions of CPU / Power components are provided in Section 2.6 on page 11.

Note that the USB ports and the SD card are not supported in PowerDNA (hosted) deployments (USB ports and the SD card are supported in our UEIPAC-based systems, which are embedded, stand-alone products).

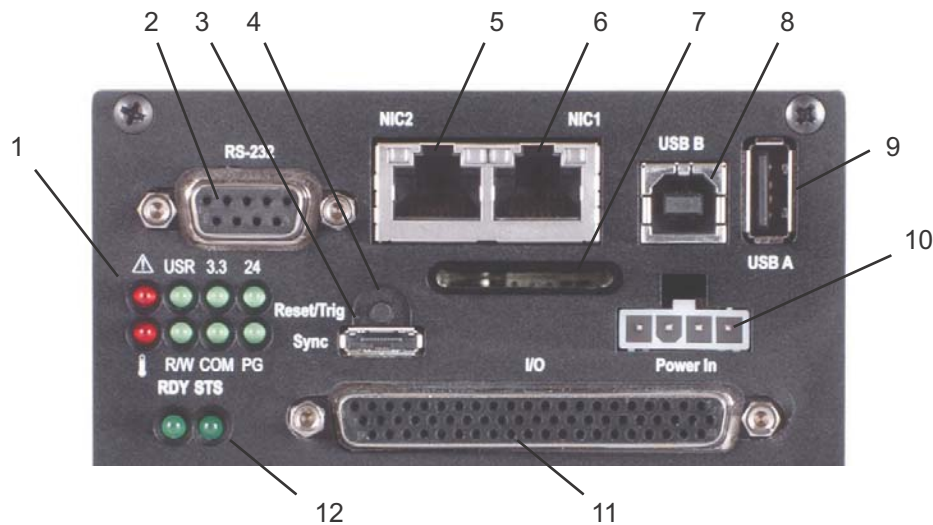


Figure 2-5. PowerDNA 1G Cube Front Panel Arrangement

No.	Name	Description
1	Status LEDs	See Figure 2-6 and Table 2-2 for LED descriptions
2	RS-232 port ¹	DB-9 serial connector for configuration or troubleshooting. Connection runs at 57,000 bps, 8 bits, no parity, 1 stop
3	Sync port ^{1,2}	High-speed, Cube-to-Cube connector for multi-cube synchronization
4	Reset	Recessed reset button
5	NIC2	Diagnostic Ethernet port: NIC2 1000/100/10Base-T connection
6	NIC1	Primary Ethernet port: NIC1 1000/100/10Base-T connection
7	SD card slot	SD card slot (for use with UEIPAC-based (embedded, stand-alone) systems, not supported on PowerDNA deployments)
8	USB B	USB B controller port (not user-accessible on PowerDNA deployments)
9	USB A	USB A slave port (not user-accessible on PowerDNA deployments)

Table 2-1. PowerDNA 1G Cube Front Panel Descriptions

No.	Name	Description
10	Power-In ¹	Power In 4-pin molex connector: 9-36 VDC, DNA-PSU adapter included
11	I/O board connector(s)	DB-37 or DB-62 connection(s) to I/O board(s) (See I/O board manuals for pinout diagrams)
12	I/O board LEDs	I/O board LEDs: RDY (ready), STS (active)

Table 2-1. PowerDNA 1G Cube Front Panel Descriptions (Cont.)

1. See Section 3.7.2 on page 38 for RS-232, sync, and power connector pinout diagrams.
2. Refer to the *PowerDNx 1PPS Synchronization Interface Manual* for more information about 1PPS or IEEE-1588 / PTP programming.

Status LEDs are displayed in **Figure 2-6** and described in **Table 2-2**. LEDs are physically mounted on the POWER module.



Figure 2-6. DNA-PPCx-1G Front Panel LEDs

No.	Name	Description
1	ATT	Indicates system needs attention: Error when red LED is ON
2	USR	Optionally controlled by user application: OFF is default
3	3.3	Indicates status of internal 3.3 V supply: LED ON (OK) / OFF (ERROR)
4	24	Indicates status of internal 24 V supply: LED ON (OK) / OFF (ERROR)
5	PG	Indicates the presense of a valid power input: LED ON (OK) / OFF (ERROR)
6	COM	Indicates I/O communication active: Flashes once/second when communicating / OFF when not
7	R/W	Indicates bus activity: Flashes when bus is active / OFF when not
8	OverTemp	Indicates high temperature condition in module: LED ON (high temp) / OFF when not

Table 2-2. System Status LED Descriptions

2.6 PowerDNA CPU/POWER Core Module

The DNA-PPCx-1G core is a 2-board module that consists of a CPU/NIC board and a POWER board. It is assembled in the upper two slots a PPCx-1G cube.

- The CPU/NIC board contains a Freescale PowerPC 8347 400 MHz, 32-bit CPU and associated Network Interface Control (NIC) logic that controls all Ethernet communication.
- The DNA-POWER-1GB board uses a dedicated DC/DC source to provide power to the PowerDNA PPCx-1G cube.

DNA-PPCx-1G core components are shown in the functional block diagram in **Figure 2-7** below and described in **Table 2-3**.

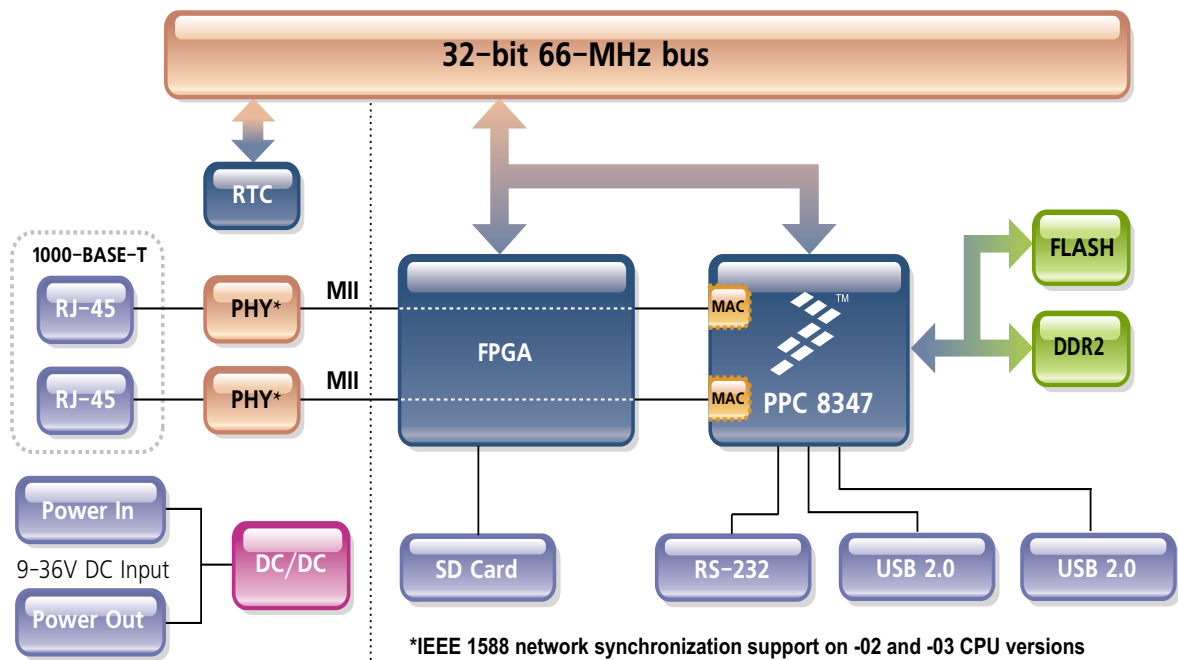


Figure 2-7. Functional Block Diagram of DNA-PPCx-1G Core Module (2 Boards)

Table 2-3 Components in PowerDNA Core Module (DNA-PPCx-1GB Series)

Item	Description
NIC1	The NIC1 port provides communication between the Cube system and the primary LAN network.
NIC2	The NIC2 port provides the ability to monitor the Cube system health during operation, using a separate diagnostic port. This port may also be assigned as the primary Ethernet port if NIC1 is not available for use.
RS-232 Port ¹	The RS-232 port provides a serial communication link between the Cube system and a standard RS-232 terminal.
USB 2.0 Dual Ports (Controller and Slave)	The USB A and B ports are not supported on DNA-PPCx-1G (hosted) systems (only supported on UEIPAC, UEISIM, UEIModbus, and UEIOPC-UA deployments).



Table 2-3 Components in PowerDNA Core Module (DNA-PPC-1GB Series)

Item	Description
32 MB or 128 MB Flash Memory	DNA-PPCx-1G / UEINet (-00/-01) systems provide 32 MB of flash memory. DNA-PPCx-1G-02 / UEINet-02 systems provide 32 MB of flash memory. DNA-PPCx-1G-03 / UEINet-03 systems provide 128 MB of flash memory. (Flash is only user-accessible on UEIPAC-based deployments)
128 MB or 256 MB of SDRAM	DNA-PPCx-1G / UEINet (-00/-01) systems provide 128 MB of RAM. DNA-PPCx-1G-02 / UEINet-02 systems provide 256 MB of RAM. DNA-PPCx-1G-03 / UEINet-03 systems provide 256 MB of RAM. (SDRAM is only user-accessible on UEIPAC-based deployments)
SYNC Port ^{1,2}	<p>A high-speed system-to-system synchronization connector permits triggers and/or clocks to be shared among multiple systems. Two systems may be connected together directly and larger groups may use the SYNC interface to share timing signals among many cubes and systems.</p> <p>The trigger and clock inputs will accept signals from standard digital logic that is powered in the range of 3.3V to 5V. The inputs also have internal pull-up resistors to an internal 5V supply, making the inputs also compatible with a low-side drive open-collector output. The Sync and trigger outputs have 5V logic levels. The sync connector's ground and 5V power connections are provided by its own isolated DC-DC converter.</p>
IEEE-1588 Synchronization Support ²	DNA-PPCx-1G-02 / UEINet-02 and DNA-PPCx-1G-03 / UEINet-03 systems support IEEE-1588 synchronization in hardware.
SD Card	<p>A slot for inserting a Secure Digital card.</p> <p>SD cards are not supported on DNA-PPCx-1G systems.</p> <p>(SD cards are only supported on UEIPAC, UEISIM, UEIModbus, and UEIOPC-UA deployments; uses EXT3 as filesystem for the system partition and optionally FAT32 for one or more data partitions on the UEIPAC-based stand-alone systems only).</p>
Solid State Hard Drive	Optional solid state hard drive (only supported on UEIPAC, UEISIM, UEIModbus, and UEIOPC-UA deployments).
LEDs	The operating conditions indicated by the front panel LEDs are described in Figure 2-6 on page 10.

1. See Section 3.7.2 on page 38 for sync and RS-232 port pinout diagrams.

2. 1PPS and IEEE-1588 synchronization support is described in the *PowerDNx 1PPS Sync Interface Manual*.



2.6.1 Key Features of the DNA-POWER-1GB Board

The DNA-POWER-1GB board provides a non-isolated side (NIS) logic that complies with full common logic interface (CLI) implementation.

The key features of the unit are:

- Input power — 9-36 VDC 80 W maximum, protected by resettable fuses and EMI chokes
- Output power sources (all with greater than 90% efficiency)
 - 24 V, 1 A (24 W)
 - 3.3 V, 5 A (16.5 W, including the 2.5 V derived voltage)
 - 2.5 V, 3 A (derived from 3.3 V source)
 - 1.5 V, 5 A, (7.5 W, including the 1.2 V derived voltage)
 - 8 V, 0.5 A (4 W for fans)
- DC/DC for 24 V, 3.3 V, and 1.5 V are synchronized from the single spread- spectrum clock source in the CPU/NIC Core Module for low EMI noise level
- Fan control (Forced ON) and status ON/OFF
- Monitoring and LED indicators (1% accuracy, 0.25Hz update rate) for
 - All output voltages
 - Input current for the 9-36 VDC for the DNA cube housing
 - All voltages from the NIC/Power Module (24 V, 3.3 V, 2.5 V)
 - Temperature of the DNA-PPCx cube housing and boards
- Provides 9-36 VDC for all modules from an external power source



2.6.2 DC Power Thresholds Table 2-4 lists the DC power threshold specifications for PPCx-1G cubes.

Table 2-4. DC Power Thresholds for DNA-PPCx-1G Cubes

	Backplane Power Rail Voltages	Turn-on Voltage, V ¹	Reset Voltage, V	Turn-off Voltage, V ²	Notes
Logic power supply	+3.3V, +2.5V, +1.5V, +1.2V	7.5	7.2 ³	7.0	Supplies power to all CPUs and FPGAs
Analog power supply	+24V	8.5	-	7.8	Analog power supply is used as a regulated source for on-layer DC/DCs on most boards
Fan power supply	+12V	8.5	-	8.4	
On-layer DC/DCs that use input power	+Vin	7.8-8.8	-	7.5-8.5	Varies with I/O board type

1. Turn-on, V: The value of Vin at which the corresponding DC/DCs are turned on.
2. Turn-off, V: The value of Vin at which the corresponding DC/DCs are turned off.
3. Reset V: When Vin is below 7.2 V, a voltage reset puts all boards into reset mode.

NOTE: A DNA-PPCx-1GB core module consumes 70 mW when Vin is below 7 V.



2.7 PowerDNA I/O Boards

DNA-PPCx-1G I/O boards are identified with a DNA- prefix.

Your selection of I/O boards can include

- Analog input boards to measure voltage, current, strain gages, thermocouples and more
- Analog output boards with outputs to ± 40 V or ± 50 mA
- Digital I/O interfaces for logic and “real-world” signal levels
- Counters and timers, quadrature encoder inputs
- Communications interfaces for RS-232, RS-422/485, ARINC 429/453/708, AFDX, MIL-STD-1553, CAN bus, and more
- And more

I/O boards are populated into your Cube chassis in the order you specify.

Refer to the I/O board data sheets and user manuals for detailed electrical specifications, board descriptions, and user instructions. These documents are available on the UEI website at www.ueidaq.com.

I/O Board Stack Sequence in a Cube



Individual boards can be removed and replaced in the field. You can also rearrange the locations of boards within the cube enclosure at any time; however, note that you may need to move jumpers on the I/O board(s).

Each Cube I/O board includes a jumper block that identifies the I/O board position in the stack. If you change the order of your I/O boards in your Cube or install a new board, you may need to adjust corresponding hardware jumpers. This is only applicable in Cube systems (jumpers are not used in DNR or DNF I/O boards for installation in a RACKtangle or FLATRACK chassis.)

Refer to the *PowerDNA Field Installation Guide* for more information about installing I/O boards and setting jumper positions in cubes.



Chapter 3 Installation and Configuration

The following installation and configuration topics are included in this chapter:

- Initial Installation Guide (Section 3.1)
- Initial Boot-up (Section 3.2)
- IP Address Overview & Update Procedures (Section 3.3)
- Network Configuration (Section 3.4)
- Troubleshooting (Section 3.5)
- Updating Firmware (Section 3.6)
- Mounting and Field Connections (Section 3.7)
- Wiring I/O Boards (Section 3.8)
- Repairing / Upgrading a Cube System (Section 3.9)
- Configuring a NIC Port for Diagnostic Mode (Section 3.10)
- Disabling Writes to Flash/EEPROM (NVRAM) (Section 3.11)

3.1 Initial Installation Guide

This section describes the recommended procedure for initially setting up your hardware and software when you first receive a DNA-PPCx-1G system:

- Verify shipment contents, Section 3.1.1
- Install software, Section 3.1.2
- Verify communication over serial port (optionally) / initial boot up, Section 3.2
- Configure IP addresses (if needed), Section 3.3
- Connect your PowerDNA Cube to your host PC or network switch, Section 3.4 and Section 3.7 (optionally)

3.1.1 Inspect Package

With a standard DNA-PPCx-1G system, the shipping package should include the following:

- A DNA-PPCx-1G enclosure, preinstalled with a NIC/CPU module POWER module, blank filler panels (if needed), plus your selection of I/O boards
- A DNA-PSU-24-100 100-watt¹ universal powerline brick that plugs into an AC outlet and provides 24 VDC output. The supply comes with a power cord for the mains and an adapter cable ending in a Molex connector
- A DB-9 serial cable for initial hardware configuration and firmware downloading (DNA-DB9MF-CBL)
- A Cat5e Ethernet cable, 7 foot (DNA-CAT5E-CBL)
- CD-ROM with support software

1. A larger power supply may be required for some configurations. Refer to UEI.



3.1.2 Install Software

This section describes how to load the PowerDNA software suite onto a Windows- or Linux-based computer (i.e. host PC) and run some initial tests.

The latest support software is online at www.ueidaq.com/download; a copy is also on the PowerDNA Software Suite CD.

A. Software Install: Windows

The PowerDNA CD provides one installer that combines the UEI low-level driver and UEIDAQ Framework.



Be sure to install third-party applications (such as LabVIEW, MATLAB, or Visual Studio) **before** installing the PowerDNA Software Suite. The installer automatically searches for third-party IDE and testing suites, and adds them as tools to the suites found.

To install PowerDNA software, do the following:

STEP 1: Open the PowerDNA Software Suite installer as an administrator.

You can run the installer from the provided PowerDNA Software Suite CD or from a downloaded installation from our website.

- To run the installer from the PowerDNA Software Suite CD, insert the CD into your CD-ROM drive. Windows should automatically start the PowerDNA Setup program.

An installer with the UEI logo will open, and then the PowerDNA Welcome screen should appear.

If this does not happen, run `setup.exe` from the CD drive:

Start >> Run >> d:\setup.exe >> OK

- To run from a recently downloaded executable from www.ueidaq.com, right-click the filename, and run as administrator.

STEP 2: Follow the prompts, and then choose a PowerDNA Software Suite Setup Type.

Unless you are an expert user and have specific requirements, select *Typical Installation* and accept the default configuration.

The Software Suite installer automatically installs any required tools and plugins.

If 32-bit Java VM is not detected on the system, Java JRE 1.6.5 for Windows XP will automatically be installed for PowerDNA Explorer. As an alternative, use the *Custom* option to display and ensure that all of the necessary packages are installed.

- Companion Documentation:
Quick Start Guide, Configuration and Core Module,
I/O Board Manuals, API Programming Guide
- SDK: includes/lib for C/Java, examples, and JRE;
(The SDK is not the UeiDaq Framework)
- PowerDNA Apps: PowerDNA Explorer, MTTTY
- PowerDNA Components (incl. DLL files)
- PowerDNA Firmware

STEP 3: Click **Next** to continue through the dialogs.



STEP 4: Click **Finish** to complete the installation.

The Software Suite installs tools needed in later steps, such as MTTTY, PowerDNA Explorer, and the low-level driver.

UEIDAQ Framework is also included in the installation and provides the structure for developing applications under C/C++, C#, VB.NET, ActiveX, MATLAB, LabVIEW, LabWindows/CVI, OPC, and other programming languages.

STEP 5: Restart the computer.

NOTE: Because the installation process modifies your Windows registry, you should always install or uninstall the software using the appropriate utilities. Never remove PowerDNA software from your PC directly by deleting individual files; always use the Windows Control Panel Add/Remove Programs utility.

B. Software Install: Linux

The PowerDNA_*.tgz file in the CD\Linux folder contains the software package for Linux. To extract the file to a local directory:

```
tar -xjvf <Path to file>/PowerDNA*.tgz
```

Follow the instructions in the readme.txt file provided in the tar file.



3.2 Initial Boot-up Perform an initial boot in preparation for configuring the network using the following procedure:

- STEP 1:** Familiarize yourself with the layout of your DNA-PPCx-1G system front panel. Refer to Figure 2-5 on page 9 for board placement.
- STEP 2:** Optionally, set up communication over the serial port by attaching the serial cable between the host PC and to the RS-232 port on the front panel of the DNA-PPCx-1G:
- Run a serial terminal-emulation program (e.g., MTTTY) on the PC. Any terminal-emulation program, except HyperTerminal, may be used (MTTTY, Minicom, TeraTerm, PuTTY, etc.).
 - Verify that COM parameters are set at: 57600 baud, 8 bits, no parity, 1 stop bit.
 - Click **Connect** in MTTTY, or use the commands on one of the other terminal-emulation programs to establish communication with the DNA-PPCx-1G system.
- STEP 3:** Connect power to the system via the Molex connector at the front of the DNA-PPCx-1G chassis.

NOTE: As soon as the system powers up, it runs through a self-diagnostic mode and, if you have serial communications set up, generates output on the terminal program. A typical readout is shown below.

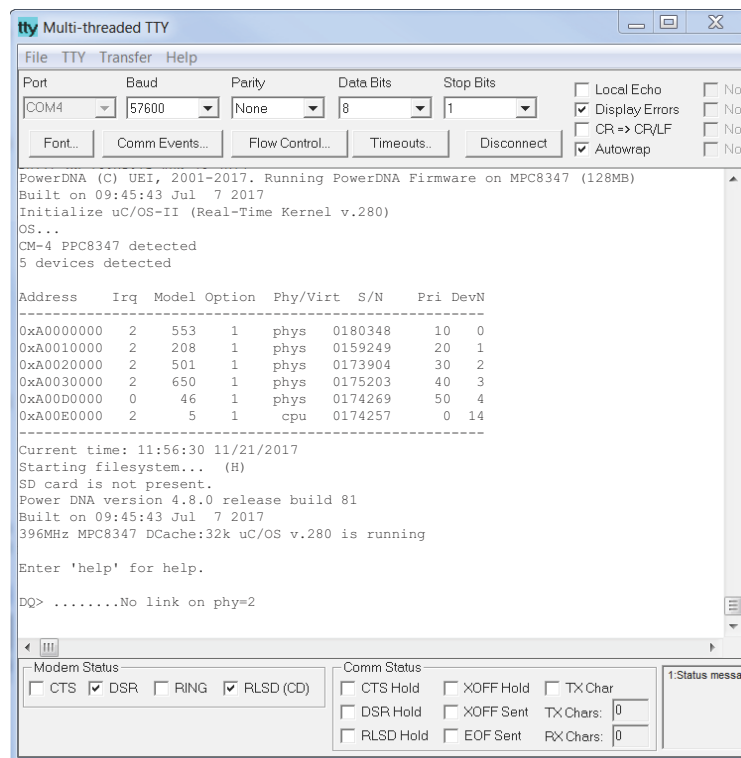


Figure 3-1. Typical MTTTY Screen after DNA-PPCx-1G Boot-up



The boot process displays the model, serial number, and slot positions of boards in the cube enclosure.

You can also type `show` <Return> at the `DQ>` serial prompt to display additional information about the system configuration:

```
DQ> show
```

```
      name: "IOM-174257"
      model: 3005
      serial: 0174257
      fwct: 1.2.0.0
      mac: 00:0C:94:02:A8:B1
      srv: 192.168.100.2
      ip: 192.168.100.2 (1Gbit)
      gateway: 192.168.100.1
      netmask: 255.255.255.0
      mac2: 00:0C:94:F2:A8:B1
      srv2: 192.168.100.102
      ip2: 192.168.100.102 (DOWN)
      gateway2: 192.168.100.1
      netmask2: 255.255.255.0
      udp: 6334
      license: ""
      Manufactured 4/6/2017
      Calibrated 4/6/2017
```

```
DQ>
```

Through the serial connection, all parameters can be changed, including the IP address, gateway, and subnet mask (netmask) system configuration.

The next section provides instructions for changing the IP address. You can also refer to **Chapter 5** for more information about changing the IP address and other parameters via the serial port.



3.3 IP Address Overview & Update Procedures

The DNA-PPCx-1G ships with pre-configured factory default IP addresses for NIC1 and NIC2 in nonvolatile memory (usually 192.168.100.2 for NIC1 and 192.168.100.102 for NIC2). These are static IP addresses; a hosted DNA-PPCx-1G system never retrieves its IP address from a DHCP server.

This section describes when and how to change the default IP addresses.

3.3.1 When Should You Change the IP Address?

You should change your IP address if you have multiple UEI chassis in your application or if your application has network addressing guidelines you must conform to.

Before connecting your DNA-PPCx-1G to a general-purpose (company domain) network, consider the following:

- High sampling rate measurements consume a lot of the available bandwidth.
- Some samples may be significantly delayed or entirely dropped (lost) due to network congestion, collisions or a slow switch.
- Whether a system will be accessed by multiple parties on a LAN.
- Whether multiple Cubes/RACKs/systems will operate (and interact) on the same network.

Alternatively, if you plan to use the system for high-speed measurements where high reliability is necessary, a direct connection between the host PC and the DNA-PPCx-1G NIC is recommended.

Refer to “Network Configuration” on page 24 for more information.



3.3.2 How to Change the Primary IP Address (NIC1)

You can use PowerDNA Explorer (a UEI-developed GUI application) or a serial terminal program to change the IP address.

The first step in changing the IP address is to consult your system or network administrator to obtain unused IP addresses.

You can change the IP address from the default using either of the following procedures:

- Section 3.3.2.1 (via PowerDNA Explorer, recommended)
- Section 3.3.2.2 (via the serial port)

3.3.2.1 Update IP Address via PowerDNA Explorer

PowerDNA Explorer provides an interface for communicating with your DNA-PPCx-1G cube over an Ethernet connection.

To use PowerDNA Explorer, you must first establish communication between your host PC and chassis. Refer to **Chapter 4** for additional information about how to open, set up and use PowerDNA Explorer, if needed.

To update your IP address, do the following in the PowerDNA Explorer window:

- STEP 1:** Click **Scan Network** to explore your system (refer to **Figure 3-2** below).
- STEP 2:** Click the DNA-PPCx-1G system that you want to update, (e.g., IOM-162491. DNA-PPCx-1G systems are listed in the left panel).
- STEP 3:** Enter the new IP address in the **IP 1** field.
- STEP 4:** Press <Return> on your keyboard.
- STEP 5:** Click **Store Configuration** to save your change, and reset the DNA-PPCx-1G.

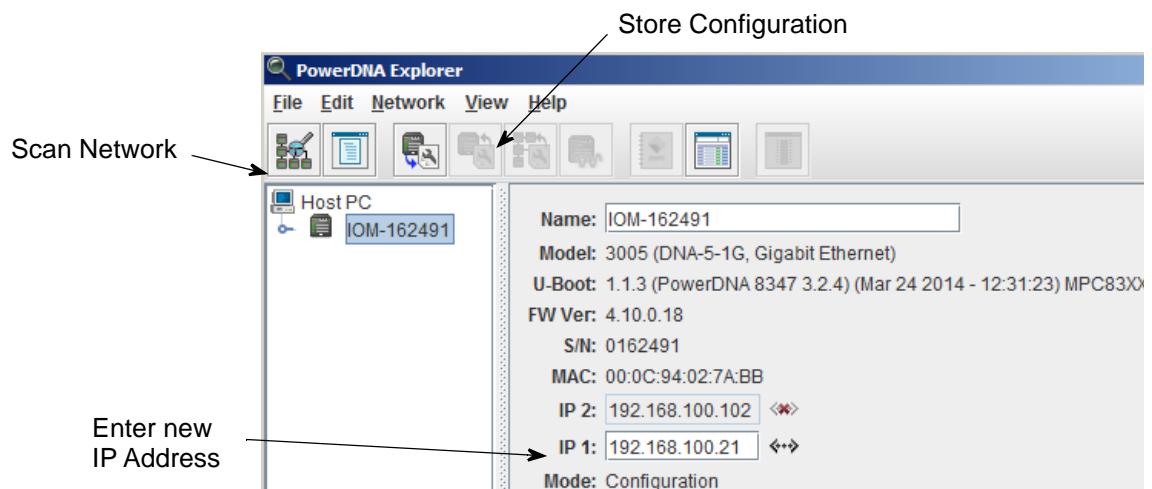


Figure 3-2. Using PowerDNA Explorer to Change IP Address

Storing the configuration downloads the new IP address into the system's non-volatile memory.

If needed, the gateway and network mask can be changed via the serial port. Refer to Section 5.4.3 on page 74 for instructions.



3.3.2.2 Update IP Address via Serial Port

To update the IP address on your DNA-PPCx-1G over the serial port, you must first establish serial communication between your host PC and chassis.

To set up communication over the serial port, do the following:

- Attach a serial cable between the host PC and the RS-232 port on the front panel of the DNA-PPCx-1G.
- Run a serial terminal-emulation program (e.g., MTTTY) on the PC. Any terminal-emulation program, except HyperTerminal, may be used (MTTTY, Minicom, TeraTerm, PuTTY, etc.).
- Verify that COM parameters are set at 57600 baud, 8 bits, no parity, 1 stop bit.
- Click **Connect** in MTTTY, or use the commands on one of the other terminal-emulation programs to establish communication with the DNA-PPCx-1G system.

NOTE: Once a connection is made, you will see a `DQ>` prompt when you press `<Enter>`.

To update the IP address on your DNA-PPCx-1G, enter the following commands in the serial terminal window:

```
DQ> set ip 192.168.200.65
Enter user password > powerdna

DQ> store
DQ> reset
```

Note that “192.168.200.65” is the new IP address in this example, the default password is “powerdna”, and `reset` reboots the system, which is required for the new IP address to take effect.

To verify the update, you can type `show` to display the new IP address.

NOTE: Refer to **Chapter 5** for more descriptions of commands you can issue via a serial connection, including descriptions of the `set` and `store` commands.

Once your IP address is configured, you can connect the DNA-PPCx-1G NIC to your host PC or to a switch for communication via a network connection.

3.3.3 How to Change the Secondary (Diagnostic) IP Address (NIC2)

To change the IP address of the secondary port (NIC2), you use a serial terminal program as with the primary port, but instead use the command:

```
set ip2 aaa.bbb.ccc.ddd
```

where `aaa.bbb.ccc.ddd` is the new IP address for the secondary port.

Then proceed the same as with the primary port. NIC2 IP addresses cannot be changed using PowerDNA Explorer. Refer to **Chapter 5** for more information.



3.4 Network Configuration

If you do not need to connect to a company LAN and have only a single DNA-PPCx-1G in your system, you can connect it directly to your host as shown in **Figure 3-3** below.

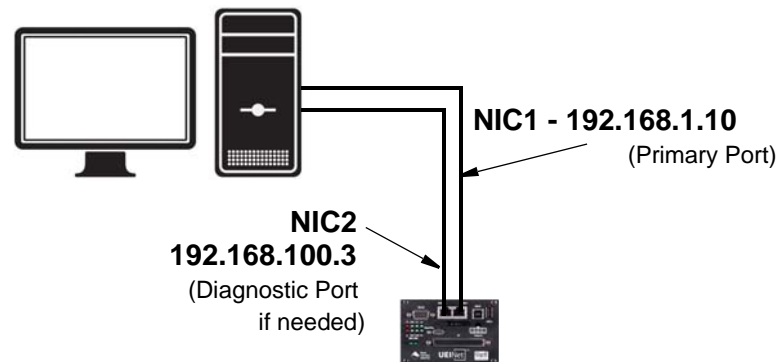


Figure 3-3. Single DNA-PPCx-1G Direct-Connected to Host without LAN Switch

When connecting to a network, to improve DNA-PPCx-1G network performance, we recommend that instead of connecting to a company-wide network, you use separate commercially available network interface controller (NIC) cards and, where possible, set up a single dedicated mini-network for cubes for both operation and diagnostics, as shown in **Figure 3-4** below.

Figure 3-4 shows a two-cube single network system with a LAN switch that performs both data acquisition and diagnostic functions.

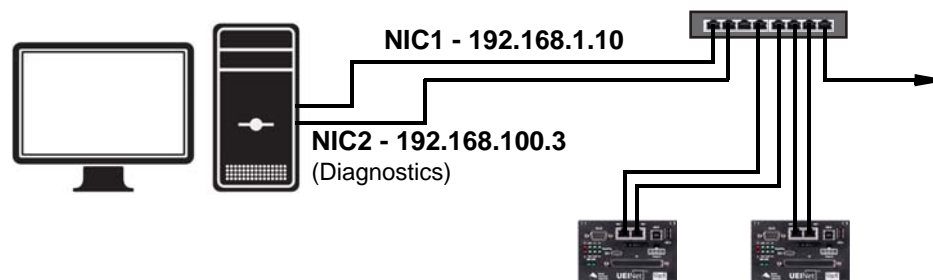
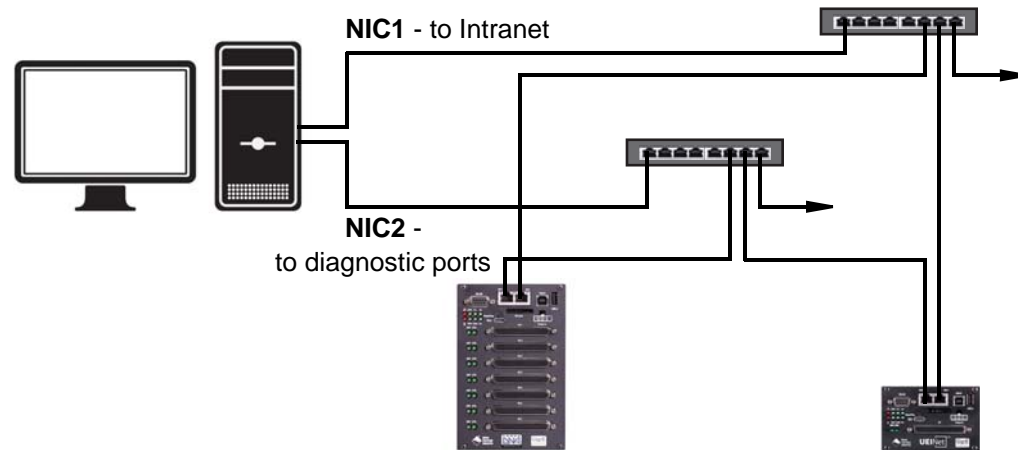


Figure 3-4. Single Network for Operation and Diagnostics Using Cubes and One LAN Switch

As an alternative, you can configure two separate networks, one for operation and one for diagnostic purposes, as shown in **Figure 3-5**.



Figure 3-5 shows a two-cube dual network system that performs both data acquisition and diagnostic functions and uses two LAN switches for routing.



**Figure 3-5. Separate Networks for Operation and Diagnostics:
Two Cubes & Two Switches**

3.4.1 Example of Configuring Network Settings

This section provides an example of configuring a separate network for diagnostics.

In this example, we assume that your office uses a Class C network (the class intended for small networks with fewer than 256 devices), and your host PC is configured with a static IP or via DHCP (Dynamic Host Configuration Protocol).

STEP 1: Obtain the networking configuration of your host PC:

- On Windows systems, open the command prompt and type `ipconfig` to display the configuration:
Start >> Programs >> (Accessories >>) Command Prompt

```
C:\> ipconfig
Ethernet adapter Local Area Connection:
    Connection-specific DNS Suffix  . : 
    IPv4 Address. . . . . : 192.168.1.10
    Subnet Mask . . . . . : 255.255.255.0
    Default Gateway . . . . . : 192.168.1.1
```

- On Linux systems, type `ifconfig` at the Linux prompt.

In the above example, the subnet mask of 255.255.255.0 uses the subnet range 192.168.1.0 through 192.168.1.255. Refer to the IP Addressing Side Note on the next page for more information about subnets.



IP Addressing Side Note:

The range of usable addresses is defined by the IP address and subnet mask.

- An IP address is a number that lies within the range of 0.0.0.0 and 255.255.255.255. In the `ipconfig` example shown in step 1, the IP address is 192.168.1.10.
- The subnet mask indicates where an address range starts and stops. For example, a subnet mask 255.255.255.240 has 15 usable addresses (255.255.255.255 – 255.255.255.240). In the `ipconfig` example shown in step 1, the subnet is 255.255.255.0, or 255 addresses.

The subnet limits from anything.anything.anything.0 up to the max.

- The usable range for 192.168.1.10/255.255.255.0 is 192.168.1.1 to 192.168.1.254 (192.168.1.0 and 192.168.1.255 are reserved for Router and Broadcast messages).
- The usable range for 192.168.100.2/255.255.255.0 is 192.168.100.1 to 192.168.100.254

Not every IP address from 0.0.0.0 to 255.255.255.255 is usable; however, these three ranges of IP addresses are guaranteed open for private use:

- 10.0.0.0 – 10.255.255.255
- 172.16.0.0 – 172.31.255.255
- 192.168.0.0 – 192.168.255.255

STEP 2: Install a secondary NIC card in your host PC, if needed.

STEP 3: Set up a secondary network that does not overlap the existing one:

In our example, the address space 192.168.1.0-192.168.1.255 is used by NIC1. The IP address block 192.168.100.1 to 192.168.100.255 is available and is in the private range.

We will choose 192.168.100.1-192.168.100.255 for the PC's secondary NIC and setup the port as follows:

IPv4 Address: 192.168.100.3
Subnet mask: 255.255.255.0
Default Gateway:192.168.100.3

- a. On your host PC, open the Network and Internet settings in the control panel:

Start >> Programs >> Control Panel >> Network and Internet >> View network status and tasks

- b. Click *Change adapter settings* in the left-sidebar, and then right-click the adapter to bring up the Properties window.
- c. Open the TCP/IPv4 properties of the adapter and edit to the network settings noted above.

NOTE: Refer to Appendix A for step-by-step instructions and screenshots on how to set up TCP/IPv4 properties.



- d. Open the Command Prompt:
Start >> Programs >> (Accessories >>) Command Prompt
- e. Type `ipconfig` at the command prompt to confirm the network configuration on the host PC:

```
C:\> ipconfig
```

<unused adapter settings are not shown in this example>

```
Ethernet adapter Local Area Connection:
    Connection-specific DNS Suffix  . : 
    IPv4 Address. . . . . : 192.168.1.10
    Subnet Mask . . . . . : 255.255.255.0
    Default Gateway . . . . . : 192.168.1.1
```

```
Ethernet adapter Local Area Connection 2:
    Connection-specific DNS Suffix  . : 
    IPv4 Address. . . . . : 192.168.100.3
    Subnet Mask . . . . . : 255.255.255.0
    Default Gateway . . . . . : 192.168.100.3
```

STEP 4: Use a serial terminal application (e.g. MTTTY) on the host to configure the DNA-PPCx-1G system to use the same subnet as the host PC. We'll set up the diagnostic port of the cube with the following:

```
Cube NIC2 IP: 192.168.100.2
Cube NIC2 Gateway:192.168.100.3
Cube NIC2 Netmask: 255.255.255.0
```

- a. Attach a serial cable between the host PC and the RS-232 port on the front panel of the DNA-PPCx-1G.
- b. Run a serial terminal-emulation program (e.g., MTTTY) on the PC. Any terminal-emulation program, except HyperTerminal, may be used (MTTTY, Minicom, TeraTerm, PuTTY, etc.).
- c. Verify that COM parameters are set at 57600 baud, 8 bits, no parity, 1 stop bit.
- d. Click **Connect** in MTTTY, or use the commands on one of the other terminal-emulation programs to establish communication with the DNA-PPCx-1G system.
- e. Enter the following commands when you see the DQ command prompt:

```
DQ> set ip2 192.168.100.2
DQ> set gateway2 192.168.100.3
DQ> set netmask2 255.255.255.0
DQ> store
DQ> reset
```

NOTE: The DNA-PPCx-1G cube in this example is changed to 192.168.100.2 in step 4 above (in the same subnet as your host PC's NIC2 at 192.168.100.3 which was set up in step 3). Note that this example assumes NIC1 is already configured on your DNA-PPCx-1G system.



STEP 5: Connect the DNA-PPCx-1G to your PC's second NIC using a CAT5 cable. The green LEDs on the DNA-PPCx-1G NIC2 should light up.

STEP 6: Ping the DNA-PPCx-1G system from the command prompt on the host PC to make sure that it is alive (the following shows a successful response):

```
C:\> ping -n 1 192.168.100.2
Pinging 192.168.100.2 with 32 bytes of data:

Reply from 192.168.100.2: bytes=32 time<1ms TTL=128
Ping statistics for 192.168.100.2:
    Packets: Sent = 1, Received = 1, Lost = 0 (0% loss),
```

NOTE: A "Request Timed Out" message indicates an error.

The system should now be configured as shown below..

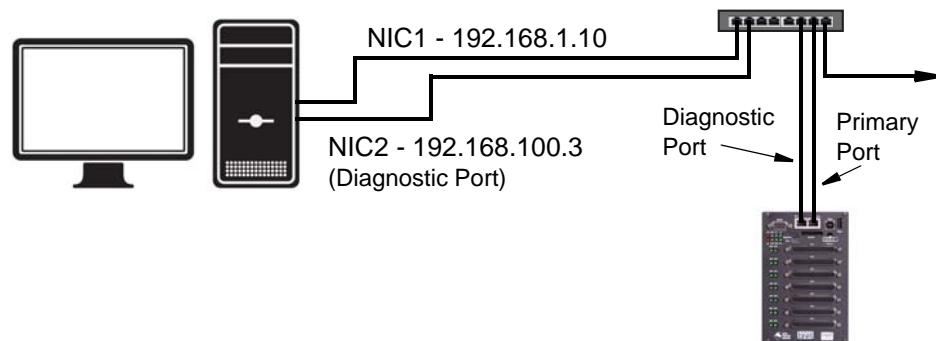


Figure 3-6. Typical Configuration for a Single DNA-PPCx-1G with a LAN Switch

STEP 7: You may now use PowerDNA Explorer to view system network settings and communicate with your cube.
(Refer to **Chapter 4** for more information about PowerDNA Explorer, if needed.)



3.5 Troubleshooting

The following sections provide suggestions when troubleshooting your system.

3.5.1 Troubleshooting System Communication

Use following checklist as a starting point.

- ☒ Verify the PG (Power Good) LED is ON:
This indicates power is applied to the chassis. (Refer to **Figure 2-6** on page 10 for LED locations)
- ☒ Verify the green LEDs on NIC ports are blinking:
This indicates the CAT5e cables are connected.
- ☒ Check communication over the Ethernet connection:
Use the command prompt to ping <system IP>.
(For example: `ping 192.168.100.2`)
If ping doesn't respond, check the following
 - Disable the firewall (temporarily) on the NIC.
 - Check the NIC's network settings.
 - Check the system's network settings.
- ☒ Check communication over the serial connection:
Connect a serial cable between your host PC and your DNA-PPCx-1G chassis, open a serial communication program (e.g., MTTTY), and click **Connect**:
 - Press [Enter] in the serial terminal window to display the `DQ>` prompt. (No prompt indicates that you are not connected).
 - If you cannot connect over the serial port, check the following:
 - Verify the settings: 57600 baud, no parity, 8 data bits, 1 stop bit.
 - Check the device manager on your PC to see which com port you are using. Enter that com port in your serial communications program, (e.g., COM1, COM2, COM3), click Connect and press <Enter>.
 - If you are able to connect over the serial port, check the following:
 - Type "show" the serial terminal window to verify the IP, Subnet Mask, and Gateway.
 - Note "show" results, and verify computers are on a valid subnet and have valid IPs.
 - Reboot the DNA-PPCx-1G system. The start-up screen should display upon restart.
- ☒ If you have questions, contact UEI support at support@ueidaq.com.



3.5.2 Troubleshooting Communication after Reset

After your Cube is set up and you reset the chassis, you may notice a situation where you can't see your Cube from a host computer immediately after reset. After up to two minutes, the connection shows up again.

This is caused by the operating system Address Resolution Protocol (ARP) implementation. When you try to contact an offline host that was previously online, the OS invalidates the Ethernet <-> IP address resolution protocol table until a timeout expires and it can be re-queried.

3.5.2.1 How to Find ARP Timeout Setting

To find how long the refresh timeout is on Windows machines, do the following:

STEP 1: Open a command window on your host computer.

STEP 2: Type `netsh interface ipv4 show interfaces` at the command prompt to find the index number of the interface connected to your cube, (e.g., 11 for the Local Area Connection):

```
C:\Windows\system32\cmd.exe

C:\Users>netsh interface ipv4 show interfaces

Idx      Met      MTU      State      Name
-----
1         50      4294967295 connected Loopback Pseudo-Interface 1
13        25       1500     connected Wireless Network Connection
14         5       1500     disconnected Wireless Network Connection 2
11         10      1500     connected Local Area Connection
16         20      1500     connected Local Area Connection 2
15         5       1500     disconnected Wireless Network Connection 3
```

Figure 3-7. Show Interfaces

STEP 3: Type `netsh interface ipv4 show interface <Idx #>` to learn the timeout and other interface parameters of a connection:

```
C:\Windows\system32\cmd.exe

C:\Users>netsh interface ipv4 show interface 11

Interface Local Area Connection Parameters
-----
IfLuid           : ethernet_6
IfIndex          : 11
State            : connected
Metric           : 10
Link MTU         : 1500 bytes
Reachable Time   : 24000 ms
Base Reachable Time : 30000 ms
Retransmission Interval : 1000 ms
DAD Transmits    : 3
Site Prefix Length : 64
Site Id          : 1
```

Figure 3-8. Show Interface Parameters

NOTE: In the above example, the timeout, or Base Reachable Time, is set to 30000 ms.



3.5.2.2 How to Speed Up ARP Timeout

To avoid waiting for the timeout, you can either force an immediate rebuild of the ARP cache or change the delay for subsequent timeout situations.

Both of the following must be entered as an administrator.

- To immediately reset, type the following at the command prompt: `arp -d *`
- To modify the Base Reachable Time, type the following to set the timeout to 5000 ms on interface 11:

```
netsh interface ipv4 set interface 11 basereachable=5000
```

3.6 Updating Firmware

This section provides the following information about updating the firmware for DNA-PPCx-1G cube systems:

- Determining Currently Installed Firmware Version (Section 3.6.1)
- Updating Firmware via PowerDNA Explorer (Section 3.6.2)
- Updating Firmware via Serial Interface (Section 3.6.3)

The CPU/NIC module in a DNA-PPCx-1G stores the system firmware.

Updated firmware is periodically released to introduce new features and to improve the performance of existing features. Updated firmware releases are bundled with the full PowerDNA Software Suite, available for download at any time from the UEI web site (www.ueidaq.com).

To locate the latest UEI firmware after installing the PowerDNA Software Suite, browse to the installation's Firmware directory, (e.g. *C:\Program Files (x86)\UEI\PowerDNA\Firmware*).

The directory contains the following:

- an MTTTY executable (serial terminal application)
- two sub-directories containing the firmware

Locate the firmware in the GigE system directory: this is the **Firmware_PPC_1G** subdirectory and the rom image file with extension MOT.



3.6.1 Determining Currently Installed Firmware Version

Before updating the firmware of a system, check the version to determine which update method to use.

PowerDNA Explorer, a GUI-based troubleshooting application provided with the installation, can be used to check the firmware version. Refer to **Chapter 4** if you need additional information about setting up and using PowerDNA Explorer.

To check the firmware version, do the following:

STEP 1: Connect power to the cube.

STEP 2: Connect an Ethernet cable between the NIC 1 port on the cube and the host PC or network (e.g., host PC Ethernet port, switch).

STEP 3: Start PowerDNA Explorer:

- From the Windows desktop menu, navigate to *Start >> Programs >> UEI >> PowerDNA >> PowerDNA Explorer*
- On Linux systems, access PowerDNA Explorer under the UEI installation directory (<PowerDNA-x.y.z>/explorer) by typing
`java -jar PowerDNAExplorer.jar`

STEP 4: In the PowerDNA Explorer window, click *Network >> Scan Network*.

STEP 5: Select the cube icon you wish to query (by clicking the icon).

Note the version that is given in the **FW Ver** field (Figure 3-9).

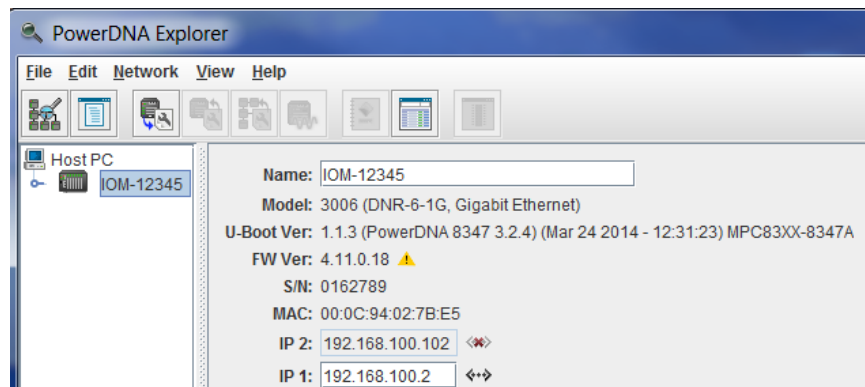


Figure 3-9. Displaying the Version of Your Firmware

Firmware Mismatch Indicator



If the **FW Ver** has a yellow triangle with an exclamation point next to it (see figure above), update your firmware.

The yellow triangle indicates that you have a mismatch between the firmware installed on your cube system and the software version on your host PC, which can cause operational errors.

If the **FW Ver** shows a version of 2.x.x.x, 3.x.x.x, or 4.x.x.x, follow the firmware update instructions on the following pages.

For older versions of firmware, (i.e. 1.x.x.x), refer to the user manual on the CD that accompanied your device when you purchased it.



3.6.2 Updating Firmware via PowerDNA Explorer

After installing a new release of UEI libraries and applications on your host PC, install the latest version of the firmware onto the CPU core module in your cube before using your system.

Instructions for updating the CPU core via PowerDNA Explorer (over Ethernet LAN line) are described below, and instructions for updating the CPU core via a serial interface (using MTTTY) are provided in the following subsection.



CAUTION!

If you update the firmware on the cube CPU board, be sure to use the PDNA Explorer from the same release version as the new firmware.

To upload firmware with PowerDNA Explorer, do the following:

- STEP 1:** Connect power to the cube.
- STEP 2:** Connect an Ethernet cable between the NIC 1 port on the cube and the host PC or network (e.g., host PC Ethernet port, switch).
- STEP 3:** Start PowerDNA Explorer:
- From the Windows desktop menu, navigate to *Start >> Programs >> UEI >> PowerDNA >> PowerDNA Explorer*
 - On Linux systems, access PowerDNA Explorer under the UEI installation directory (<PowerDNA-x.y.z>/explorer) by typing
`java -jar PowerDNAExplorer.jar`
- STEP 4:** From the PowerDNA Explorer window, click *Network >> Scan Network*.
- STEP 5:** Select the icon of the cube system to be updated.
- STEP 6:** Click *Network >> Update Firmware...* from the menu.

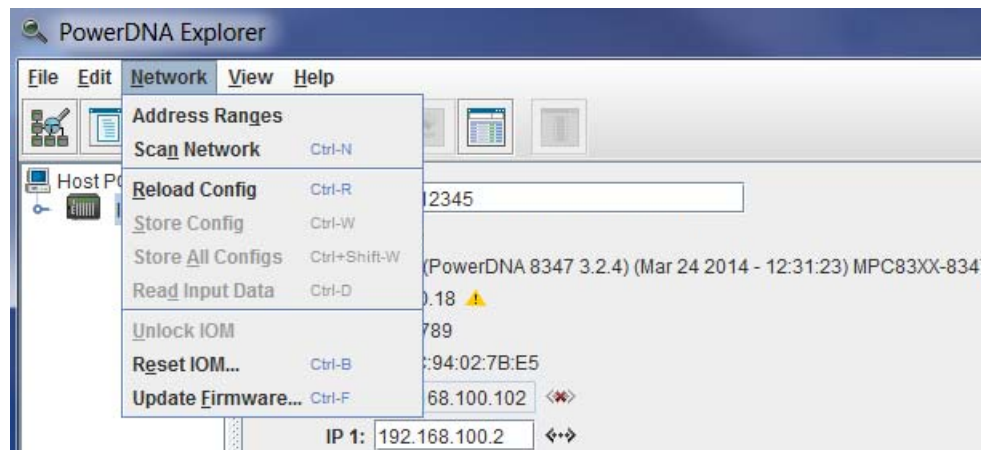


Figure 3-10. Update Firmware Menu Item

- STEP 7:** Click “Yes” when you see the prompt:
“Are you sure you want to update firmware...”
- STEP 8:** Verify you are in the Firmware_PPC_1G directory, and double-click the **rom8347_X.X.X.mot** (where X.X.X. is the version) file.



STEP 9: If asked, enter the password to continue. UEI cube and rack systems come with the default password set to `powerdna`.



Figure 3-11. Password Dialog Box

STEP 10: Wait for the progress dialog to complete. The system will then be updated and running the new firmware.

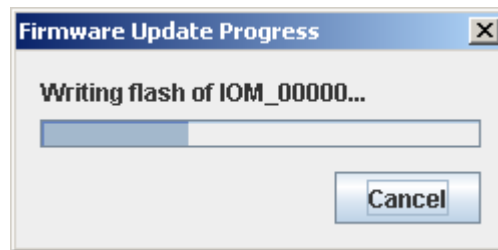


Figure 3-12. Firmware Update Progress Dialog Box

Each system is updated in three steps. First, the firmware is transferred to the system. Second, the firmware is written to the flash memory. During this step, the R/W light on the front of the chassis is lit, in addition to the PG light. Third, the system is reset. During this step, the ATT, COM, and PG lights are lit, and the R/W light will turn on and off periodically. When the system is finished resetting, only the PG light is lit.



3.6.3 Updating Firmware via Serial Interface

The following section provides the procedure for uploading firmware over the DNA-PPCx-1G serial port using a serial terminal client. In this procedure, we use MTTTY as the serial terminal client; however, any serial terminal application can be used to upload the ROM image.

- STEP 1:** Connect power to the DNA-PPCx-1G.
- STEP 2:** Attach the serial cable to the host PC and to the RS-232 port on the front panel of the cube serial port.
- Run a serial terminal-emulation program (e.g., MTTTY) on the PC.
 - Verify that COM parameters are set at 57600 baud, 8 bits, no parity, 1 stop bit.
 - Click **Connect** in MTTTY, or use the commands on one of the other terminal-emulation programs to establish communication with the cube system.
- STEP 3:** Cycle power to the cube to reset the CPU module, or type `reset` at the `DQ>` prompt in the serial window.
- STEP 4:** While the system is starting up again, press <Enter> on your keyboard to go into **U-Boot**. The `DQ>` prompt in the serial terminal window will change to the `=>` prompt when in U-Boot.
- STEP 5:** Type the commands shown below to erase firmware storage area in the Flash memory and load the new firmware (refer to Figure 3-13):

```
=> erase FF800000 FF9FFFFFFF
=> loads
```

NOTE: The `loads` command stores firmware into flash memory while downloading it after you select which firmware image file use.



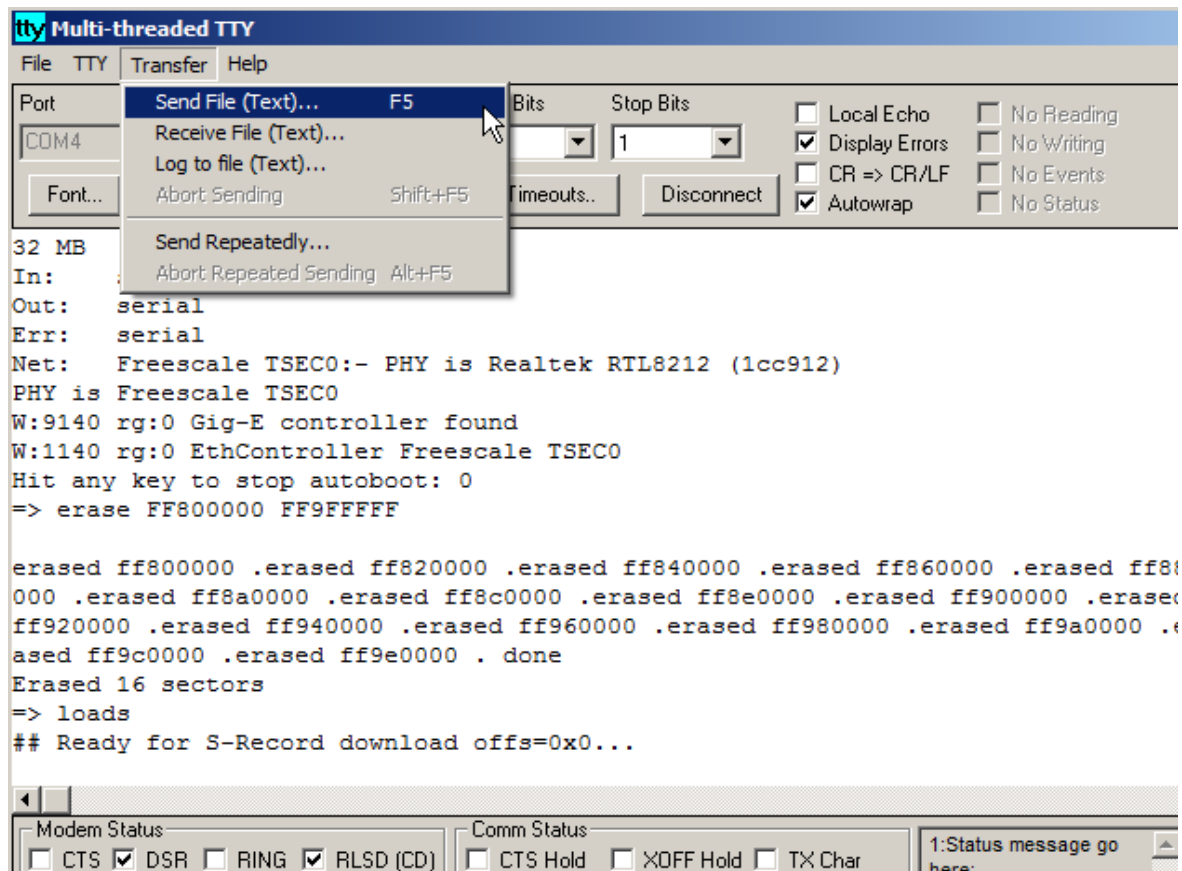


Figure 3-13. Firmware Update via Serial Port

STEP 6: Do the following to transfer the Motorola firmware image file (refer to Figure 3-13):

- In the MTTY menu bar, select *Transfer » Send File*.
- Navigate to your UEI installation, and select the image file:

`\Program Files (x86)\UEI\PowerDNA\Firmware\Firmware_PPC_1G\rom8347_4_x_y.mot`

NOTE: A progress bar will appear in the lower left corner of MTTY.

STEP 7: Wait for the upload to complete (it may take a few minutes).

STEP 8: After the process finishes, type `go FF800100` in the MTTY terminal window. The CPU module will then be updated and running the new firmware.



3.7 Mounting and Field Connections

You can mount the DNA-PPCx-1G cube on a flat horizontal surface such as a tabletop or floor, a flat vertical surface such as a wall, or in a standard 19-inch rack.

- For horizontal surface mounting, specify a flange accessory and secure the case directly to the surface.
- For mounting on a vertical wall surface, specify a 19RACKW accessory with DIN rail and attach the assembly to a standard 19-inch rack with screws.

If you need technical drawings, please contact UEI support at support@ueidaq.com.

3.7.1 Physical Dimensions

The housing used in a DNA-PPCx-1G cube consists of an extruded aluminum box with slotted guides plus a faceplate and rear cover.

The physical dimensions of PowerDNA GigE cube versions are listed below:

Table 3-1 DNA-PPCx-1G Cube Dimensions

Version	Dimensions ¹	I/O Slots
UEINet	4.1" x 4.0" x 2.7"	slots for 1 I/O board
DNA-PPC5-1G	4.1" x 4.0" x 4.0"	slots for up to 3 I/O boards
DNA-PPC8-1G	4.1" x 4.0" x 5.8"	slots for up to 6 I/O boards
DNA-PPC9-1G	4.1" x 4.0" x 6.6"	slots for up to 7 I/O boards

1. Dimensions are given as length × width × height.



3.7.2 Pinout Diagrams

Pinout diagrams for the power molex, synchronization port, and RS-232 serial port connectors are shown below in **Figure 3-14**.

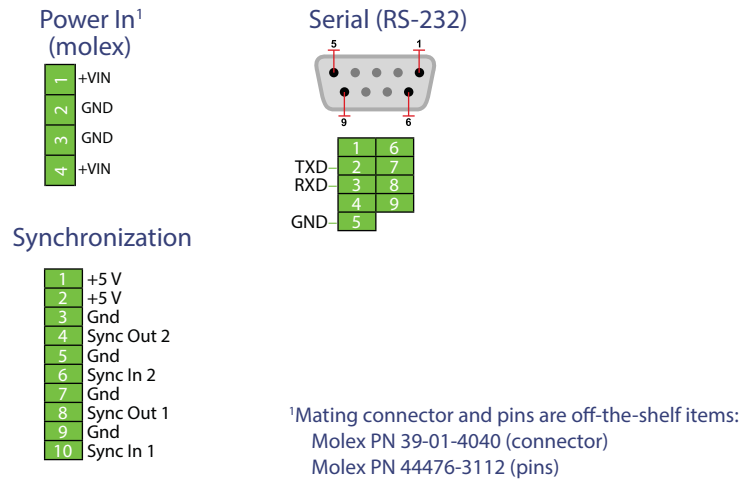


Figure 3-14 DNA-PPCx-1G Pinout Diagrams

3.7.3 Network Wiring

1000Base-T Wiring Configurations

A typical wiring configuration for a 1000Base-T network is shown below.

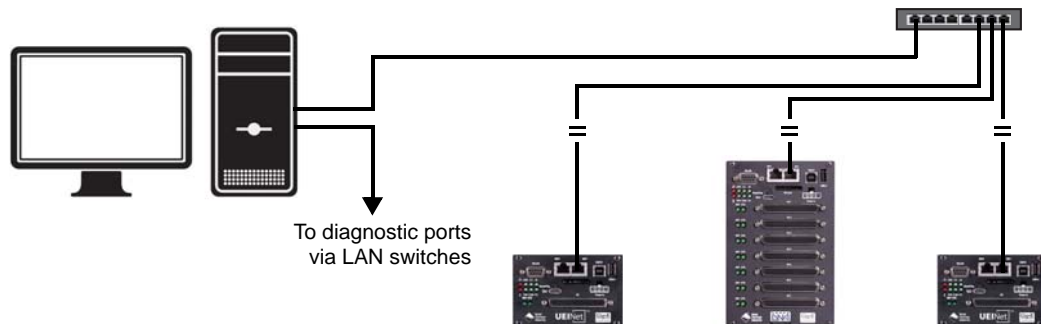


Figure 3-15. Example of System Configuration

Refer to “Network Configuration” on page 24 for more configuration options.



3.8 Wiring I/O Boards

Refer to the applicable I/O board manuals and data sheets for pinouts and proper wiring to boards.

3.9 Repairing / Upgrading a Cube System

DNA-PPCx-1G systems come from the factory fully configured and calibrated. Individual modules are designed for field replacement and are not suited for field repairs.

If you encounter a problem with a PowerDNA cube system, you can powerdown your system and remove and replace individual boards or other system modules in the field.

No Hot Swapping



Always turn POWER OFF before performing maintenance on a UEI system. Failure to observe this warning may result in damage to the equipment and possible injury to personnel.

If you rearrange the physical position of boards in the cube stack yourself, note that you may need to reprogram I/O board location(s) in your application and move hardware jumpers on your I/O board(s).

NOTE: Refer to the *PowerDNA Field Installation Guide* for more information about installing I/O boards and setting jumpers.

If you want to enhance, repair, or otherwise modify a specific I/O board, however, you must send the module back to the factory or to your local distributor.

This process requires that you request an RMA number from UEI before shipping. To do so, contact support@ueidaq.com and provide the following information:

1. Model Number of the unit, (e.g. DNA-AI-217)
2. Serial Number of the unit
3. Reason for return, (e.g. faulty channel, needs calibration, etc.)

UEI will process the request and issue an RMA number.

3.10 Configuring a NIC Port for Diagnostic Mode

The CPU core module has two Ethernet ports, NIC1 and NIC2. Either port can be assigned as the main operation port or as a diagnostics port.

The main and diagnostics ports are interchangeable. The user application can open both ports independently and use separate handles to access each of them. A port becomes a diagnostics port, which prevents changes in the state of the ongoing operation, after it is configured and locked-in as a diagnostics port. This allows great flexibility in IOM wiring — if either port or its cabling fails, you can use the other port as the main port.

If all I/O boards are in configuration mode and the lock is not set, the diagnostics port functions as an equivalent of the main port. Any command that can be executed on the main port can be executed on the diagnostics port as well.

Refer to the PowerDNA API Reference Manual for API used with this section.



The following standard DAQBIOS commands are accessible on the diagnostics port whenever one or more I/O boards are in operating mode:

```
DQCMD_ECHO          // echo
DQCMD_RDCFG         // read configuration (new)
DQCMD_RDSTS         // read status
DQCMD_WRCHNL (selected) // write channel
DQCMD_RDCHNL (selected) // read channel
DQCMD_IOCTL (selected) // ioctl() - low priority command
DQCMD_SETLOCK       // set/release port lock
```

Commands that are capable of changing the state of the running I/O boards will not execute.

3.10.1 Switching into Diagnostics Mode

To switch a port into diagnostics mode, use the `DqCmdSetLock` API, as described below:

```
int DAQLIB DqCmdSetLock(int Iom, uint8 Mode, char Password, uint32 *IP)
```

Parameters:

```
int Iom          // Pointer to the DQIOME structure
uint8 Mode       // Function mode (lock/unlock/check/diagnostics)
char *Password   // password string; ignored (and can be NULL)
                // if Mode is DQSETLOCK_CHECK
uint32 *IP       // returns the IP address of the locking host
                // if Mode is DQSETLOCK_CHECK
```

<Mode> can be one of the following:

```
#define DQSETLOCK_LOCK    0    // Lock IOM to host
#define DQSETLOCK_UNLOCK  1    // Unlock IOM
#define DQSETLOCK_CHECK   2    // Get locking host IP
#define DQSETLOCK_DIAG    4    // Switch to diagnostics
```

To advance a port into diagnostics mode, call this function with the <Mode> parameter set to `DQSETLOCK_DIAG`. To return a port to normal mode, use the same function call with `DQSETLOCK_UNLOCK`.

The following table describes the possible states of both ports:

Table 3-2 Port States

Port	LOCK State	First Port (NIC1)	Second Port (NIC2)
First	DQSETLOCK_UNLOCK	Full functionality	Full functionality
	DQSETLOCK_LOCK	Full functionality, locked to the host	All but state change functions
	DQSETLOCK_DIAG	Diagnostic functionality only	Full functionality
Second	DQSETLOCK_UNLOCK	Full functionality	Full functionality
	DQSETLOCK_LOCK	All but state change functions	Full functionality, locked to the host
	DQSETLOCK_DIAG	Full functionality	Diagnostics functionality only



3.10.2 Reading Configuration and Status in Diagnostic Mode

DQCMD_ECHO

This command returns information about the board(s) installed. Use of this command is described in the PowerDNA API Reference Manual.

DQCMD_RDCFG

This command returns the current configuration of the specified board(s):

```
int DAQLIB DqCmdReadCfg(int Iom, DQRDCFG pDQRdCfg[], uint32 maxsize, uint32* entries)
```

```
int Iom                // a pointer to the DQIOME structure
DQRDCFG pDQRdCfg[]     // structure that contains board configuration
uint32 maxsize         // number of DQRDCFG structures passed
uint32* entries        // number of DQRDCFG structures returned
```

```
typedef struct (
    uint8 DEV;          // device (host fills this field)
    uint8 ss;           // subsystem (host)
    uint32 status;      // device status (device returns following fields)
    uint32 cfg;         // configuration, including clocks
    uint32 rate;        // clock divider in 15.5ns intervals
    uint32 clsize;      // size of the channel list
    uint32 cl[];        // channel list - variable size
) DQRDCFG, *pDQRDCFG;
```

Note: Use device!=0x80 to indicate that this is the last device in the list.

DQCMD_RDSTS

This command returns the status of the IOM and each and every board in the stack (upon request):

```
int DAQLIB DqCmdReadStatus (int Iom, uint8 *DeviceNum, uint32 *Entries,
uint32 *Status, uint32 *StatusSize)
```

Parameters:

```
int Iom                // A pointer to the DQIOME structure
uint8 *DeviceNum       // Array of board numbers to retrieve status
uint32 *Entries        // Number of entries in DeviceNum array
uint32 *Status         // Buffer to store values received from device
uint32 *StatusSize     // Size of buffer, 32-bit chunks.
                      // Returns number of 32-bit values
                      // copied into Status
```

There are special device numbers to access status of various boards:

0xFE – returns IOM status and status of all boards (note that each board status is expressed as four 32-bit words. Thus, the maximum size of status packets is $(4 + 14 \times 4) \times \text{sizeof}(\text{uint32}) = 240$ bytes.

0x7F – returns IOM status only (four bytes)

0x0...0xE – returns status of one of the boards



The status for each board consists of four 32-bit words, as follows:

```
/* status offsets into devob].status array */
#define STS_STATE(0) // state of the board
#define STS_POST(1) // post status
#define STS_FW(2) // firmware status
#define STS_LOGIC(3) // logic status
```

The first word is the state of the board – what mode of operation it is in, and the lower 8-bits of the timestamp. If the 10 us timestamp does not change after each call, the logic is in the inoperative state, as:

```
/* state flags */
#define STS_STATE_TS_SH (8)
#define STS_STATE_TS_SH_INS(S,TS,MD)
((S & 0xfffff00f0) | ((TS<<8) & 0xff00) | (MD&0xf))
#define STS_STATE_STICKY (0)
```

The second word describes the status of the board. It is written when the board enters initialization mode and remains unchanged until the next reboot.

STS_POST_SDCARD_FAILED, STS_POST_DC24 and STS_POST_DCCORE can be changed during operation if the corresponding failure occurs.

```
/* POST status flags */
#define STS_POST_MEM_FAIL (1L<<0) // Memory test failed
#define STS_POST_EEPROM_FAIL (1L<<1) // EEPROM read failed
#define STS_POST_LAYER_FAILED (1L<<2) // board failure
#define STS_POST_FLASH_FAILED (1L<<3) // Flash checksum error
#define STS_POST_SDCARD_FAILED (1L<<4) // SD card is not present
#define STS_POST_DC24 (1L<<5) // DC->24 board failed
#define STS_POST_DCCORE (1L<<6) // Core voltage problem
#define STS_POST_BUSTEST_FAILED (1L<<7) // Bus test failed (hwtest.c)
#define STS_POST_BUSFAIL_DATA (1L<<8) // Bus test failed on data tst
#define STS_POST_BUSFAIL_ADDR (1L<<9) // Bus test failed on addr tst
#define STS_POST_OVERHEAT (1L<<10) // Overheat detected

#define STS_POST_STICKY (STS_POST_MEM_FAIL|STS_POST_BUSTEST_FAILED|
STS_POST_BUSFAIL_DATA|STS_POST_BUSFAIL_ADDR)
```



The third word contains the logic status flags. They are read and assembled from the various registers of the common board interface (CLI) upon request. Not all boards implement full functionality and boards operating normally should not show any flags set.

```
/*logic status flags */
#define STS_LOGIC_DC_OOR          (1UL<<0)    // DC/DC out of range (IOM
                                              //also)
#define STS_LOGIC_DC_FAILED      (1UL<<1)    // DC/DC failed (IOM also)
#define STS_LOGIC_TRIG_START     (1UL<<2)    // Trigger event started
                                              // (IOM also)
#define STS_LOGIC_TRIG_STOP      (1UL<<3)    // Trigger event stopped
                                              // (IOM also)
#define STS_LOGIC_CL0_NOT_RUNNING (1UL<<4)    // Output channel list not
                                              // running
#define STS_LOGIC_CLI_NOT_RUNNING (1UL<<5)    // Input channel list
                                              // not running
#define STS_LOGIC_CVCLK_CL0_ERR  (1UL<<6)    // CV clock error for CL0
#define STS_LOGIC_CVCLK_CLI_ERR  (1UL<<7)    // CV clock error for CLI
#define STS_LOGIC_CLCLK_CL0_ERR  (1UL<<8)    // CL clock error for CL0
#define STS_LOGIC_CVCLK_CLI_ERR  (1UL<<9)    // CL clock error for CLI

#define STS_LOGIC_NO_REPORTING    (1UL<<31)   // Installed logic does not
                                              // support error reporting

#define STS_LOGIC_STICKY          (STS_LOGIC_NO_REPORTING)
```

The fourth word contains the status of the firmware. A board operating normally does not have any flags set except STS_FW_CONFIG_DONE, which means the board was properly configured before entering operating mode (it is cleared upon re-entering configuration mode) and STS_FW_OPER_MODE, which means that the board switched into operating mode without any errors.

```
/* fw status flags */
#define STS_FW_CLK_OOR          (1UL<<0)    // Clock out of range (IOM
                                              // also)
#define STS_FW_SYNC_ERR        (1UL<<1)    // Synchronization interface
                                              // error (IOM also)
#define STS_FW_CHNL_ERR        (1UL<<2)    // Channel list is incorrect
#define STS_FW_BUF_SCANS_PER_INT (1UL<<3)    // Buf setting error:
                                              // scans/packet

#define STS_FW_BUF_SAMPS_PER_PKT (1UL<<4)    // Buf setting error:
                                              // samples/packet
#define STS_FW_BUF_RING_SZ     (1UL<<5)    // Buf setting error: FW
                                              // buffer ring size
#define STS_FW_BUF_PREBUF_SZ   (1UL<<6)    // Buf setting error: Pre-
                                              // buffering size
#define STS_FW_BAD_CONFIG      (1UL<<7)    // Board cannot operate in
                                              // current config
#define STS_FW_BUF_OVER        (1UL<<8)    // Firmware buffer overrun
#define STS_FW_BUF_UNDER       (1UL<<9)    // Firmware buffer underrun
#define STS_FW_LYR_FIFO_OVER   (1UL<<10)   // Board FIFO overrun
```



```

#define STS_FW_LYR_FIFO_UNDER(1UL<<11) // Board FIFO underrun
#define STS_FW_EEPROM_FAIL (1UL<<12) // Board EEPROM failed
#define STS_FW_GENERAL_FAIL (1UL<<13) // Board general failure
#define STS_FW_ISO_TIMEOUT (1UL<<14) // Isolated part reply timeout
#define STS_FW_FIR_GAIN_ERR (1UL<<15) // Sum of fir coeffs is not correct
#define STS_FW_OUT_FAIL (1UL<<16) // Output CB tripped or over-
// current
#define STS_FW_IO_FAIL (1UL<<17) // Messaging I/O failed (5xx
// boards)
#define STS_FW_NO_MEMORY (1UL<<18) //Error with memory allocation
#define STS_FW_BAD_OPER (1UL<<19) // Operation was not performed
// properly
#define STS_FW_LAYER_ERR (1UL<<20) // Board entered operation
// successfully

#define STS_FW_CONFIG_DONE (1UL<<30) //Configuration is completed
// (no error)
#define STS_FW_OPER_MODE (1UL<<31) // Board entered operation
// mode successfully

/* status helper macros/defines */
#define STS_FW_STICKY (STS_FW_EEPROM_FAIL|STS_FW_GENERAL_FAIL)

```

Status bits are divided into “conditional” and “sticky”. Conditional bits are set when a condition arises; they are cleared when the error condition expires. Sticky bits are persistent once set and are cleared by reading their status.

DQCMD_IOCTL

This command is used to retrieve data from the board. When a port is in diagnostic mode, it returns current data but cannot reprogram the channel list. The channel list is used to inform the handler the ID of the channel from which data should be retrieved.

The following table lists functions that rely on the DQCMD_IOCTL command for transport for several board types:

Table 3-3 Example Functions and Associated Boards

Function	Associated Board Type(s)
DqAdv201Read	AI-201 and AI-202
DqAdv205Read	AI-205
DqAdv207Read	AI-207
DqAdv225Read	AI-225
DqAdv3xxWrite	AI-302/308 and AI-332
DqAdv40xRead	DIO-401/405/404/406
DqAdv403Read	DIO-403
DqAdv416GetAll	DIO-416 -- Voltage, current, and circuit breaker state monitoring
DqAdv432GetAll	DIO-432 -- Voltage, current, and circuit breaker state monitoring
DqAdv448Read	DIO-448
DqAdv448ReadAdc	DIO-448 -- Voltage monitoring



Table 3-3 Example Functions and Associated Boards (Cont.)

Function	Associated Board Type(s)
DqAdv501GetStatistics	SL-501and SL-508 -- Received/error counters
DqAdv566GetStatistics	ARINC-429-566 -- Received/error counters
DqAdv601Read	CT-601 -- Counters, states of input lines
DqAdv604Read	QUAD-604 -- Positions, states of input lines

3.10.3 Sequence of Operation for Diagnostic Mode

To use the diagnostic port without affecting performance of the main port, UEI recommends that you use the following sequence of operations:

1. Open main port.
2. Open diagnostics port.
3. Perform hardware reset (optional) and re-open ports, if needed.
4. Lock diagnostic port into `DQSETLOCK_DIAG`.
5. When operation is configured on the main port, read the status of the diagnostics port to verify that the configuration was programmed correctly.
6. Once operation on the main port is started, the diagnostics port becomes available for data retrieval.
7. Read status of the diagnostics port to make sure that all boards of interest successfully entered operating mode without error.
8. In the cycle:
 - a. Retrieve the current status once a second.
 - b. Check the flags for error conditions.
 - c. Retrieve additional data if any flags are set.
9. Stop operation and unlock diagnostics port.
10. Resume normal operation with main port.



3.11 Disabling Writes to Flash/EEPROM (NVRAM)

Writing non-volatile memory (NVRAM) can be disabled via a hardware jumper on the CPU board.

By installing an NVRAM protection jumper, all writes to flash and EEPROM will be disabled on the hardware level.

NOTE: Writes to the EEPROM on the DNx-AO-358 and DNx-AO-364 are not disabled by this process.
Applications that must disable all NVRAM writes should not include the DNx-AO-358 and DNx-AO-364 products in their system.

Note that installing the NVRAM protection jumper requires removal and replacement of the CPU board in the cube chassis. In general UEI recommends that a cube be returned to the factory for adding or replacing boards. UEI can install and remove jumpers as needed, if you have any concerns.

3.11.1 Disabling NVRAM Writes

To disable writes to non-volatile memory, do the following:

- STEP 1:** Disconnect power to the cube system.
- STEP 2:** Attach a grounding strap to your wrist, and follow normal ESD procedures.
- STEP 3:** Tag all port and D-sub connector cabling, and disconnect cables from the front of the cube.
- STEP 4:** If the cube has a fan, remove the screws securing the rear cover to the housing. Lay the cover flat on the bench with the cable connected, and then disconnect the power connector for the fan from the power board.
- STEP 5:** Using a 3/16-inch nut driver, unscrew all jack screws on the sides of the RS-232 connector. Unscrew the jack screws securing each 37- and 62-pin D-sub connector to faceplate.
- STEP 6:** Remove the four corner screws located on the corners of the faceplate. Use an appropriate screwdriver to avoid stripping the screws.
- STEP 7:** Remove the faceplate. Carefully push or pull the faceplate/board stack assembly out of the cube housing. Exercise caution to not bend or damage the pins on the last I/O board. Place the assembly onto an anti-static surface.
- STEP 8:** Identify the board labeled DNx-POWER-1GB in the stack (it is the second from the top and includes the Molex connector).
- STEP 9:** Carefully separate the I/O board stack so that the DNx-POWER-1GB board can be removed. Carefully pull boards apart and do NOT bend or damage any pins.



STEP 10: Locate the J4 jumper block on DNx-POWER-1GB board removed in the previous step. Refer to **Figure 3-16** for jumper block location.

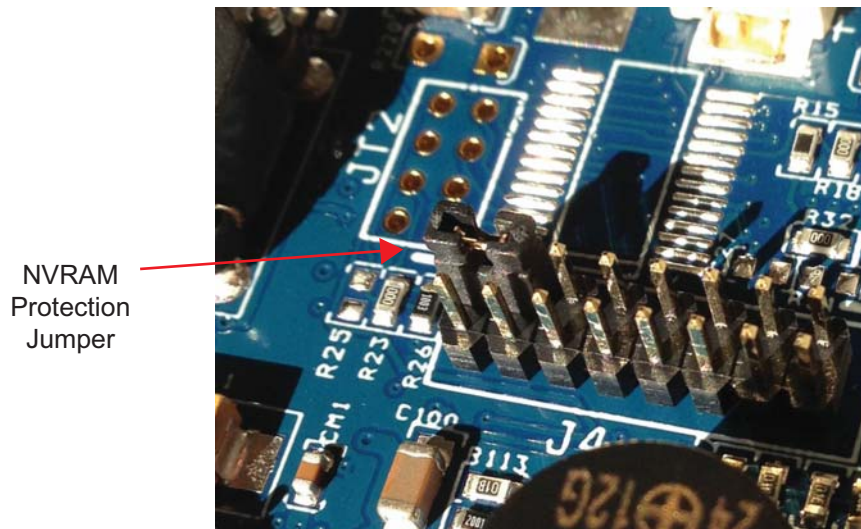


Figure 3-16. NVRAM Protection Jumper

STEP 11: Insert jumper between pins 13 and 15 on J4 jumper block. Refer to **Figure 3-16**.

STEP 12: Reassemble the cube: carefully align all pins and reassemble the stack.

STEP 13: Verify that all boards are in the correct positions and then attach the faceplate to the stack using the same jack screws previously removed. Use a 3/16-inch nut driver. Do not overtighten (5 lb-in. max torque).

STEP 14: Insert the stack into the cube housing, carefully aligning all boards with the correct slots in the housing.

STEP 15: Slide the faceplate/stack assembly into the housing so that the faceplate is seated properly in the housing.

STEP 16: Reinsert the mounting screws for the faceplate and tighten securely. Do not overtighten. Check the DNx-POWER-1GB board LEDs, RESET button, and sync port at the front of the carrier: RESET button should be free to move.

STEP 17: If fan was removed, plug fan power cable into connector on NIC board and secure rear cover to cube.

STEP 18: Return cube to working location and secure in place.

STEP 19: Check all cable tags and reattach all cables to the appropriate connectors.

STEP 20: Restore power to the system.

STEP 21: Restart the system with your normal operating procedure.

NOTE: It may be helpful to power up the cube stack outside of the housing so that you can verify your assembly.

NOTE: If your cube is repeatedly rebooting, check to ensure that your RESET pushbutton has not become stuck in the cube's case.

3.11.2 Re-enabling NVRAM Writes

To re-enable writes to non-volatile memory, repeat the procedure in Section 3.11.1 except remove the jumper in step 11 instead of installing it.



Chapter 4 PowerDNA Explorer

PowerDNA Explorer is a GUI-based application for communicating with your PowerDNA Cube systems. PowerDNA Explorer simplifies configuration and setup of your system, as well as allows you to check your communication link and start exploring your Cube and I/O boards.

This chapter provides the following information:

- Getting Started with PowerDNA Explorer (Section 4.1)
- Connecting PowerDNA Explorer to Your System (Section 4.2)
- Overview of the Main Window (Section 4.3)
- Example of Digital Input/Output Board Settings (Section 4.4)
- Example of Analog Output Board Settings (Section 4.5)
- Example of Analog Input Board Settings (Section 4.6)
- Example of Counter/Timer Board Settings (Section 4.7)

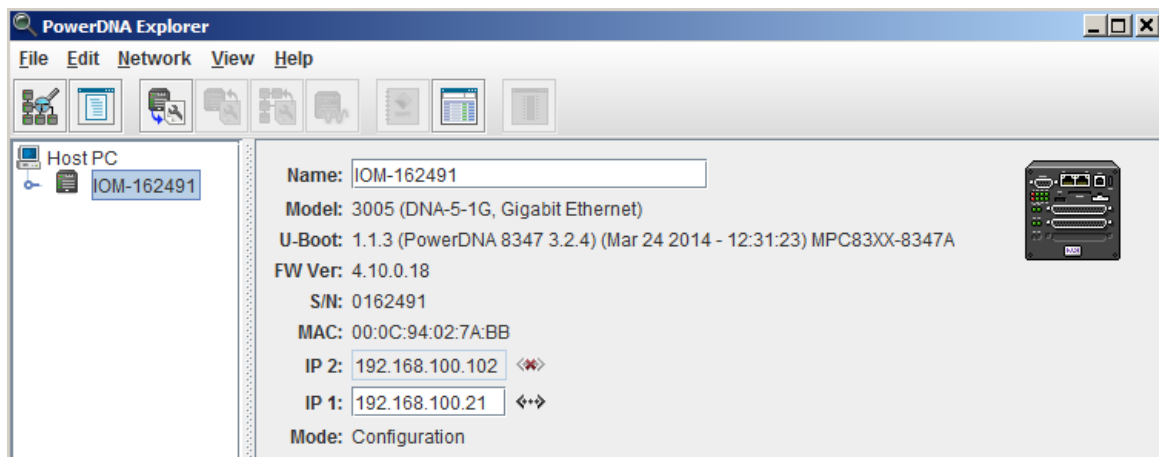


Figure 4-1. PowerDNA Explorer

4.1 Getting Started with PowerDNA Explorer

PowerDNA Explorer can be used on Windows or Linux systems.

On Windows systems, access PowerDNA Explorer from the Start menu:

- *Start > All Programs > UEI > PowerDNA > PowerDNA Explorer*

On Linux systems, access PowerDNA Explorer under the UEI installation directory (<PowerDNA-x.y.z>/explorer) by typing:

- `java -jar PowerDNAExplorer.jar`

NOTE: UEI provides a PowerDNA Explorer DEMO with the installation that lets you safely explore the menus and I/O board screens without using actual hardware. DEMOs are located in the same directories as the PowerDNA Explorer executables.



4.2 Connecting PowerDNA Explorer to Your System

PowerDNA Explorer has the capability of identifying PowerDNA Cubes and RACKs on a selected network. Using PowerDNA Explorer, you scan the network, and discovered systems list in the left-hand panel of the display.

- To display pertinent hardware and firmware information about a system, once it is discovered, click the specific system shown in the left-hand panel.
- To display I/O boards installed in your PowerDNA system, click the toggle to the left of the Cube image in the left-hand panel, and I/O boards will display below.
- To display pertinent information about an I/O board in the system, click the I/O board of a specific system and then manipulate its inputs or outputs in the settings screen.

PowerDNA Explorer lets you verify that the system is communicating with the host and that the I/O boards are functioning properly.

To scan the network for PowerDNA Cubes or RACKs, you must provide a range of addresses to scan. Do the following to setup the address range:

STEP 1: Select *Network >> Address Ranges* from the menu:

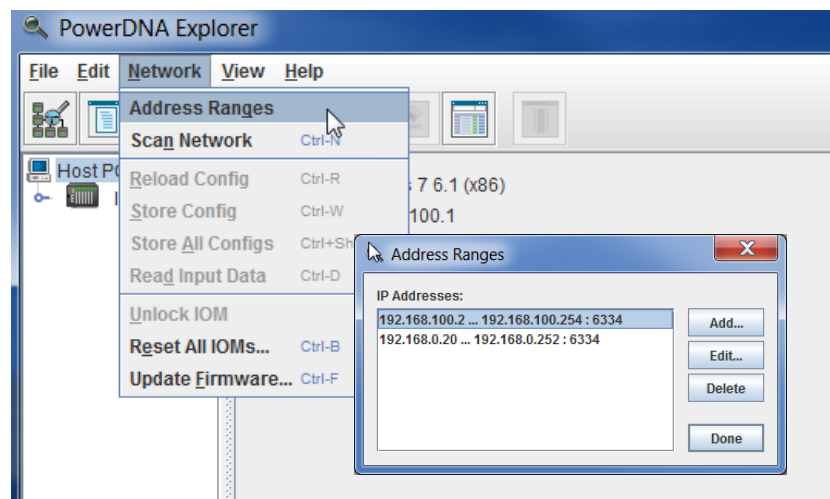


Figure 4-2. Address Ranges to be Scanned

STEP 2: If the IP address of your system (e.g. 192.168.100.2) is not in the listed range, edit the range to include it, and then click **Done**.



STEP 3: Click *Network >> Scan Network* to scan the LAN for PowerDNA Cubes or RACKs within the range specified in the previous step.

One or more system icons will display in the left-hand-side of the screen. If no icons are displayed, refer to the Troubleshooting section in the previous chapter (Section 3.5).

STEP 4: Double-click an icon to display its information and list the I/O boards:

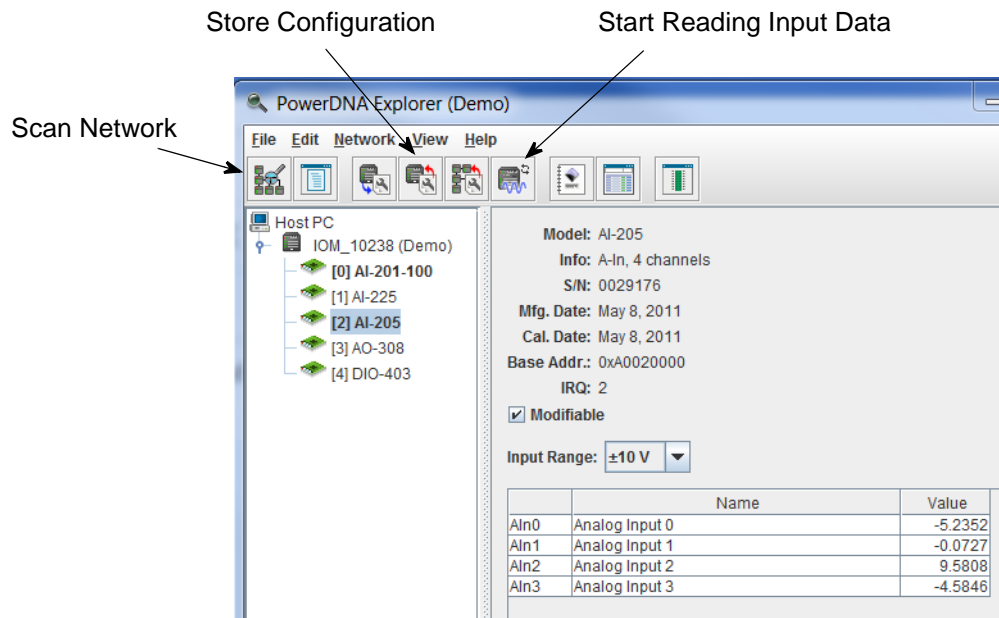


Figure 4-3. Typical Screen for Analog Input Board

The screenshot above is from the PowerDNA Explorer Demo.

The PowerDNA Explorer Demo provides a simulator for users without hardware or for new users who want to explore the PowerDNA Explorer interface without reading/writing to real hardware. Run this program and hover your mouse over the buttons to read the tool-tips and learn through interacting with the program.

Some quick notes:

- ✓ To read from a board, click **Start Reading Input Data**.
- ✓ To write to the board, change a Value and click **Store Configuration**. The **Restore** icon with the blue arrow restores the configuration.
- ✓ To change the IP address, change the number, deselect the field, and click **Store Configuration**. Take care not to set the IP Address to outside of the network's configuration subnet -or- to an IP address that is currently in use, as the system will then become unreachable.
- ✓ To obtain a hardware report, click *View >> Show Hardware Report*.

Refer to Section 4.3 for more descriptions of the PowerDNA Explorer Window.



4.3 Overview of the Main Window

The Main Window of the PowerDNA Explorer is shown below and consists of four primary sections:

- The Menu Bar (described in Section 4.3.1)
- The Toolbar (described in Section 4.3.2)
- The Device Tree (described in Section 4.3.3)
- The Settings Panel (described in Section 4.3.4).

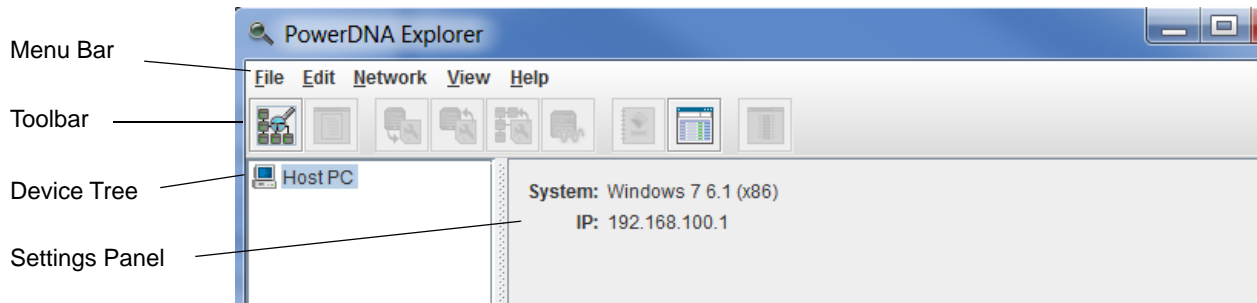


Figure 4-4. PowerDNA Explorer Main Window

When PowerDNA Explorer is first launched, the Main window has several buttons grayed out and shows only the Host PC in the Device Tree, as shown above. To access systems in your network, you must first scan the network (refer to Section 4.1).

4.3.1 Menu Bar

The following subsections describe menus and menu items contained in the Menu Bar.

4.3.1.1 File Menu

This section describes items under the File Menu.

4.3.1.1.1 Setting Timeouts

The *File >> Preferences* selection opens the preferences dialog. The preferences dialog allows you to specify timeout intervals.

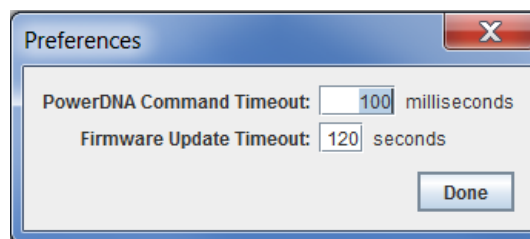


Figure 4-5. PowerDNA Explorer Timeout Preferences

PowerDNA Command Timeout sets the length of time PowerDNA Explorer will wait for response from a CPU/NIC Core Module before giving up with an error. It defaults to 100 milliseconds.

Firmware Update Timeout specifies the length of time PowerDNA Explorer will wait when updating firmware via *Network >> Update Firmware...* The firmware timeout defaults to 120 seconds. *File >> Exit* exits the application. If there are unsaved device settings changes, you are prompted for confirmation.



4.3.1.2 Network Menu This section describes items under the Network Menu.

4.3.1.2.1 Specifying IP Address Ranges *Network >> Address Ranges* opens the Address Ranges dialog, allowing you to specify where to scan for devices.

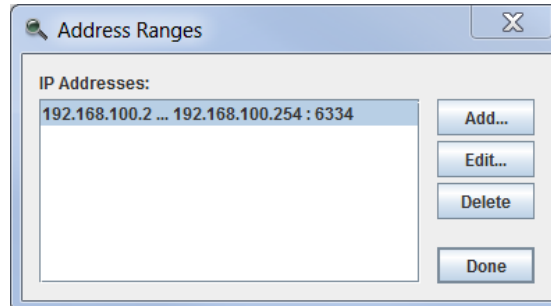


Figure 4-6. Address Ranges Dialog Box

The Address Ranges dialog allows you to specify the IP addresses and UDP port to use to find devices. The list in the above example defaults to a single range item that specifies the range 192.168.100.2 through 192.168.100.254.

By clicking **Add** or **Edit**, you can specify individual addresses, as well as address ranges. After clicking **OK**, specified items appear in the list, from which items can be added or deleted.

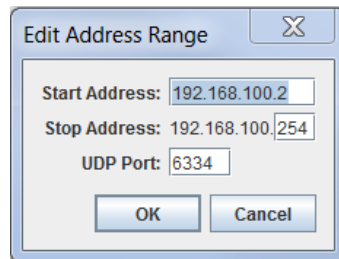


Figure 4-7. Edit Address Ranges Dialog Box



4.3.1.2.2 Scanning Network for UEI Chassis

Network >> Scan Network scans the network for devices and populates the device tree. How much of the network is scanned depends on the settings in the Network Ranges dialog.

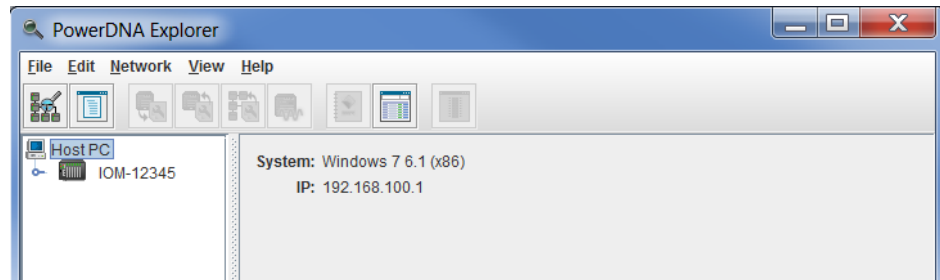


Figure 4-8. After a Network >>Scan Network

In the example shown above, after *Network >> Scan Network* was clicked, the PowerDNA chassis labeled “IOM-12345” was found and displays in the Device Tree panel.

If you choose **Scan Network** when the device tree is already populated, any new devices discovered will be added to the tree. Any existing devices that are missing will be removed from the tree, unless you have made unsaved changes to the device's configuration, in which case it will be marked in the tree as missing.

If you add a new device and **Scan Network** and do not see the device, refer to Section 3.5.

4.3.1.2.3 Reloading Configuration

Network >> Reload Config re-reads the configuration of the current device selected in the Device Tree. If you have made changes to the settings in the settings panel for the current device, **Reload Config** will replace those settings with the current settings for the device, after prompting for confirmation.

4.3.1.2.4 Storing a Configuration

Network >> Store Config writes the changed settings for the currently selected device to the device. The button is disabled for devices that haven't been modified.

4.3.1.2.5 Storing All Configuration

Network >> Store All Configs writes all of the changed device settings to the devices. The button is disabled if no devices have been modified.

4.3.1.2.6 Reading Input Data from I/O Boards

Network >> Start Reading Input Data is enabled when the currently selected device is an input device board. It reads the current input values to the device and displays data read in the settings panel.

4.3.1.2.7 Updating the Firmware

Network >> Update Firmware... loads a firmware update file to all connected PowerDNA systems if Host PC is selected. It updates only one chassis when a specific unit is specified. More information about updating firmware can be found in “Updating Firmware” on page 31.

Note that writing certain configuration changes to a PowerDNA system will bring up a password dialog box. PowerDNA Cube and RACK systems come with the default password set to “**powerdna**”.





Figure 4-9. Password Dialog Box for “Store Config” and “Store All Configs”



Figure 4-10. Password Dialog Box for “Update Firmware . . .”



4.3.1.3 View Menu

This section describes items under the View Menu.

4.3.1.3.1 Obtaining a Report of Cube Hardware

View >> Show Hardware Report displays hardware information for your PowerDNA system.

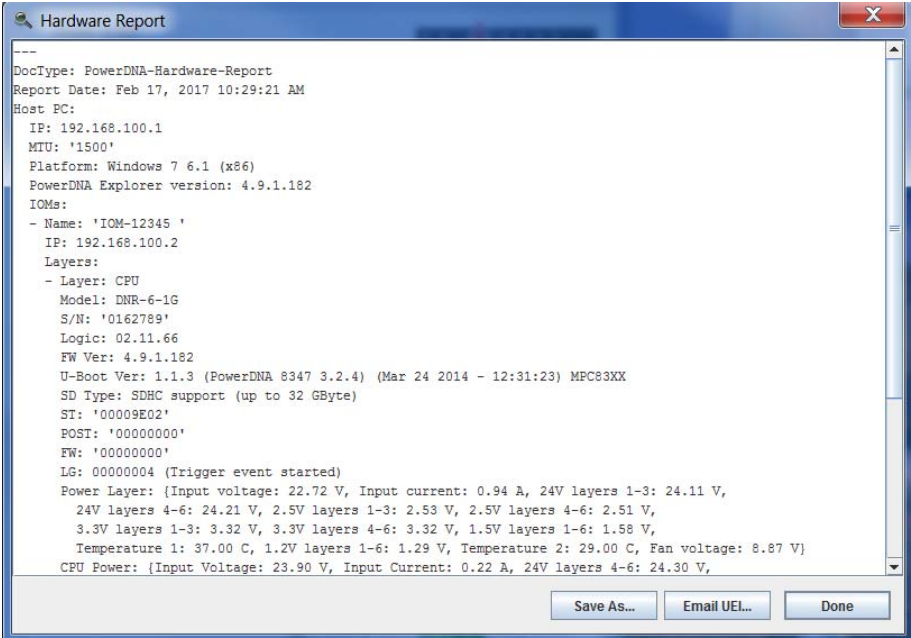


Figure 4-11. Example of a Hardware Report

Note that the above hardware report is for a RACK chassis (the DNR-6-1G); however, the concept is the same for the Cube.

4.3.1.3.2 Displaying the Wiring Diagram for an I/O Board

View >> Show Wiring Diagram displays connector pins for a specific board. All boards have this feature. The AI-207 is displayed below as an example. The wiring diagrams in PowerDNA Explorer match the wiring diagrams in the following sections.

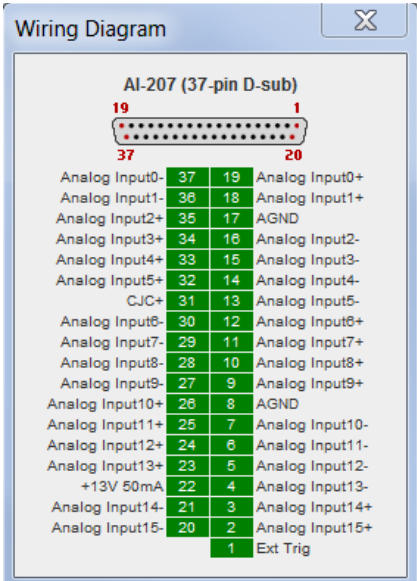


Figure 4-12. Example of a Wiring Diagram Display

4.3.1.4 Help Menu

Help >> About PowerDNA Explorer shows the **About ...** box, which shows the program icon, program name, version number, company name, and copyright notice.

4.3.2 Toolbar

Toolbar buttons duplicate the functionality of the corresponding menu items described in the previous Menu Bar sections.

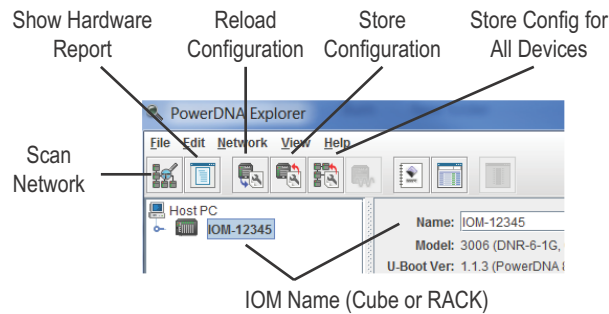


Figure 4-13. PowerDNA Explorer Toolbar Buttons (Config Level)

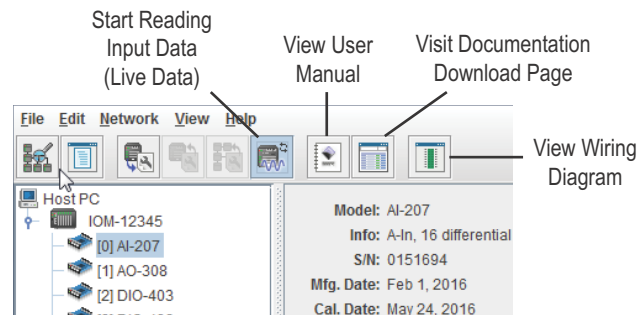


Figure 4-14. PowerDNA Explorer Toolbar Buttons (Board Level)



4.3.3 Device Tree

When the application is first launched, the device tree contains a single root item representing the host computer (see **Figure 4-4**).

When you select **Scan Network** from the Network menu or the toolbar, the device tree is populated with all central controllers, IOMs (racks and cubes), and device boards accessible from the network, as filtered through the *Network >> Address Ranges* dialogue.

Central controllers, if any, appear as children of the Host PC item. IOMs that are connected to the PC without use of a central controller also appear as direct children of the Host PC item.

Each item has an icon indicating whether it is a central controller, IOM (rack or cube), or board. The text label for each item is the device's model number, name, and serial number.

Boards are also labeled with their position number in brackets.

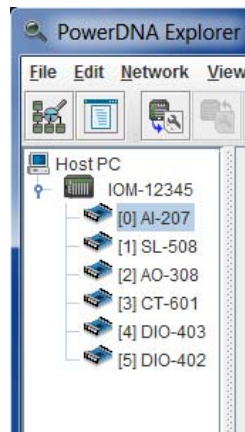


Figure 4-15. Example of the Device Tree

When an item is selected in the tree, the settings panel changes to reflect the settings for that device. The first time an item is selected, the device is queried as though you had invoked the **Start Reading Input Data** command.

On subsequent selections of the same item, the last settings are re-displayed. Thus, if you made changes but did not write them to the device, the changes are remembered. Invoking the **Start Reading Input Data** command will re-read the device and overwrite the current settings in the settings panel.

Devices whose settings have changed, but have not been written, are displayed in bold italics in the tree to provide a visual cue. Changed devices that become missing on a subsequent invocation of **Scan Network** turn red in the tree. (Unchanged items that become missing are simply removed from the tree.)



4.3.4 Settings Panel The settings panel presents a set of controls that allows you to change the settings of the device currently selected in the device tree or allows you to view acquired input data for the device selected.

4.3.4.1 IOM Settings The settings panel provides the following fields when an IOM is selected in the tree.

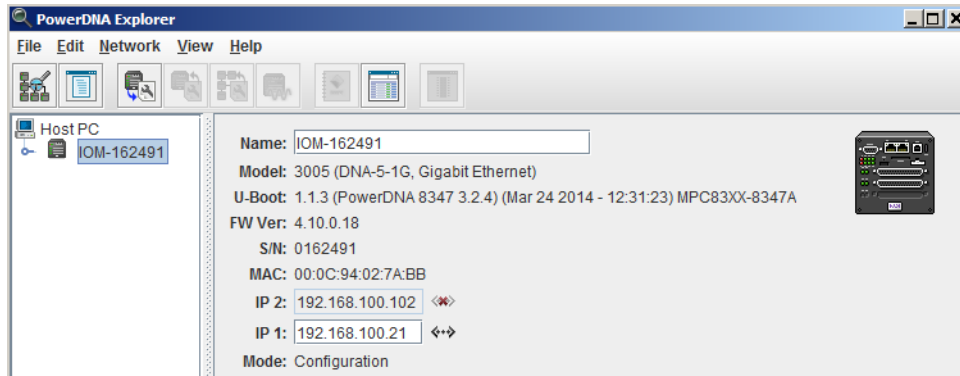


Figure 4-16. Example of IOM Settings Panel

Field	Description
Name	shows the IOM name. Users can enter a custom name
Model	shows the model number of the IOM
U-Boot Ver	shows the U-Boot version installed on the PowerDNA system
FW Ver	shows the version of the firmware installed on the PowerDNA system
S/N	shows the serial number of the IOM
MAC	shows the MAC address. It cannot be changed and is informational only
IP Address	shows the IP addresses of the IOM. IP 1 can be changed. See Section 3.3.3 for instructions on changing IP 2
Mode	shows the mode the IOM is in: <i>Initialization</i> , <i>Configuration</i> , <i>Operation</i> , or <i>Shutdown</i> .

Table 4-1 Fields and Descriptions for IOM Settings Panel



4.3.4.2 I/O Device / Board Settings

Figure 4-17 shows a screen for displaying I/O device settings.

Note that setting options vary for I/O boards on a per-board basis. The example below show settings for the AI-217 analog input board.

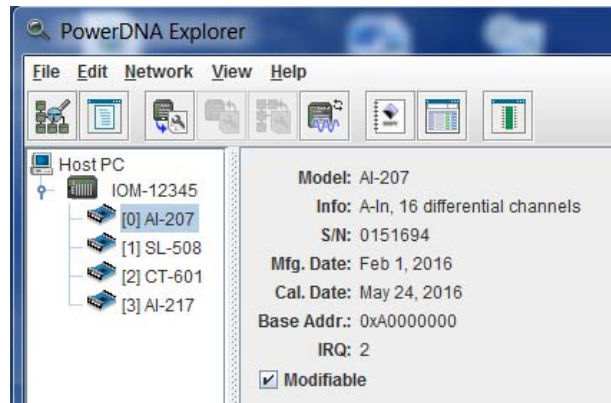


Figure 4-17. Example of I/O Device Settings

Each I/O device has the following settings.

- **Model** shows the model number of the device.
- **Info** shows some key features of the device: A for analog, D for digital, In for input, Out for output, and a number of channels available.
- **S/N** shows the device serial number.
- **Mfg. Date** shows the manufacturing date.
- **Cal. Date** shows the date of the last calibration done.
- **Base Address** shows the base address of the board in the IOM system.
- **IRQ** shows which interrupt is assigned to the board.
- **Modifiable** is a checkbox which, when unchecked, prevents parameters from being changed.



- 4.3.4.2.1 Reading Data from I/O Boards** To read data from the board, select *Network >> Read Input Data*. The **Value** column of any board will update, as shown below:

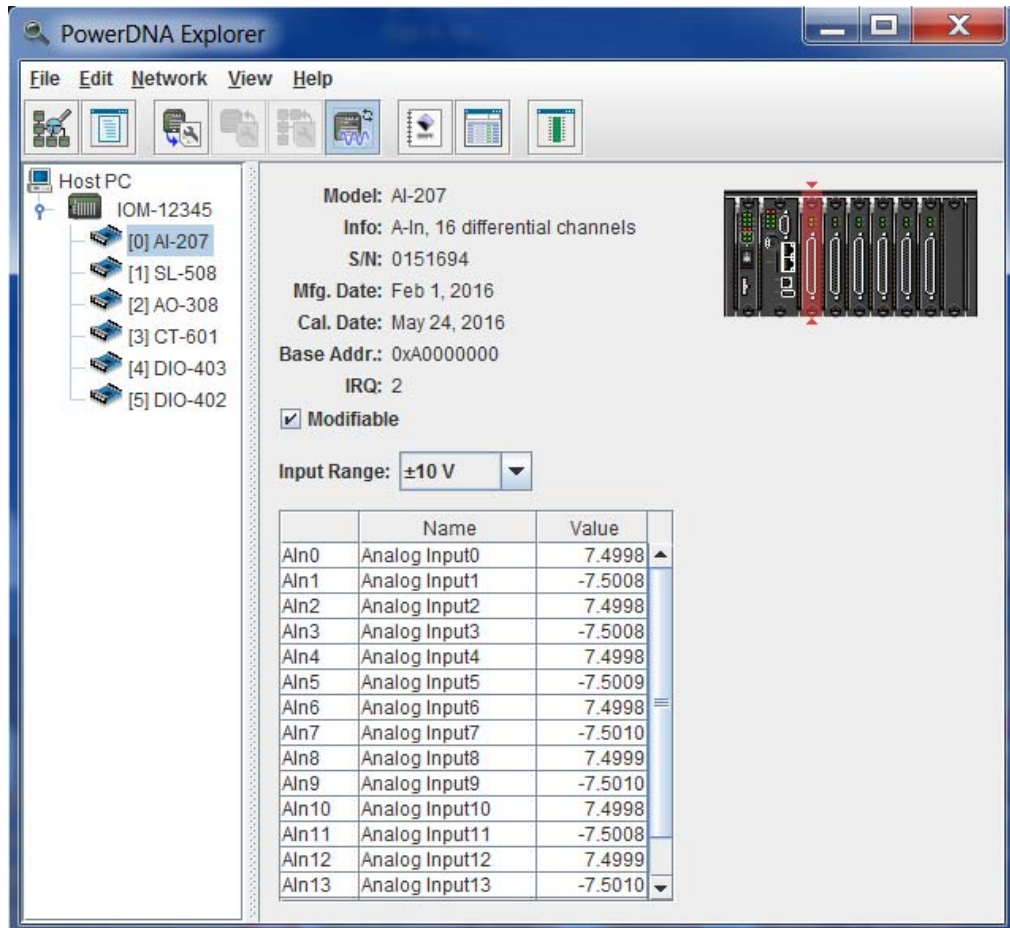


Figure 4-18. Screen from Network >> Read Input Data

- 4.3.4.2.2 Editing & Storing Board Configuration** You can also add or edit channel names and save the new configuration. After editing names, choose *Network >> Store Config* to save changes to the board. This is true for all boards. Additionally, if you have changed a configuration value, but have not chosen *Network >> Store Config* to save them, previous values can be re-read from the board, using *Network >> Reload Config*.



4.4 Example of Digital Input/Output Board Settings

This section provides an example of PowerDNA Explorer settings for digital input/output boards. Each type of I/O board will have displays specific to the features offered with that board. In this section, we use the DIO-403 as an example.

NOTE: Use *Network >> Read Input Data* to see immediate input values in Input tabs. Use *Network >> Store Config* to save values to the board.

The DIO-403 board is a 48-bit DIO board. The board is different from other digital I/O boards because it groups 8-bits at a time into ports, and three ports into two channels. This means that bit 0 in port 0 in channel 0 corresponds to DIO pin 0; bit 1 in port 1 in channel 0 corresponds to DIO pin 9; bit 2 in port 2 in channel 0 corresponds to DIO pin 18, etc.

For the sake of abstraction in PowerDNA Explorer, we'll call all the ports channels.

Other DIO boards display each bit individually.

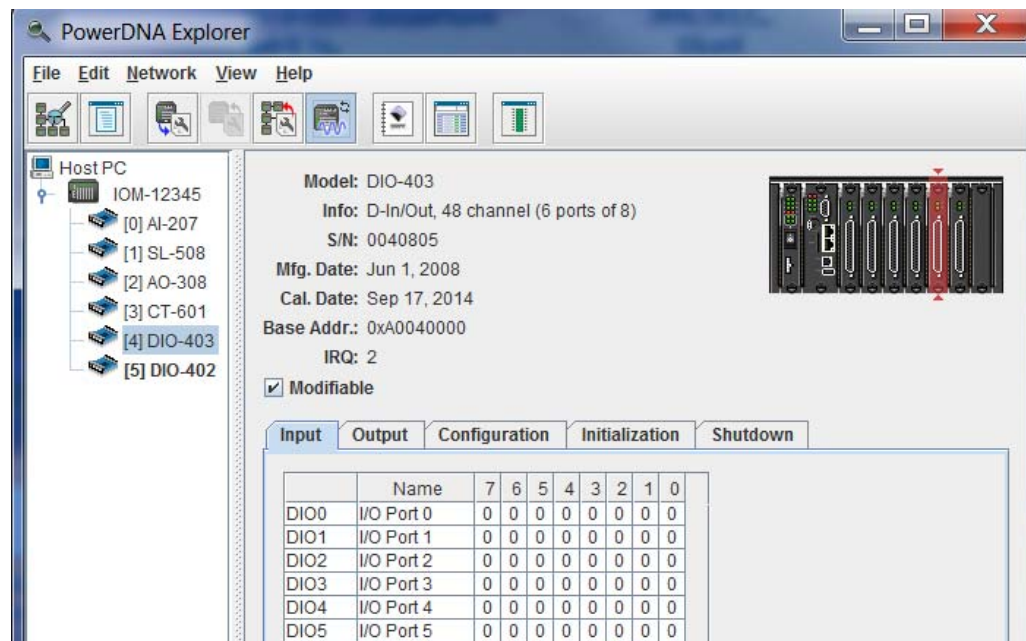


Figure 4-19. Example of DIO-403 Inputs

Input/Output/Configuration/Initialization/Shutdown tabs switch between displaying DIO pin reading of current input state data, setting DIO output state, configuring DIO as output or input, and settings for initial and shutdown states.

The Input tabs contain the following columns:

- **Name** is the channel (port) name, or a user-defined string.
- **7:0 Input Values** consist of 0 or 1 as read from the input pin.

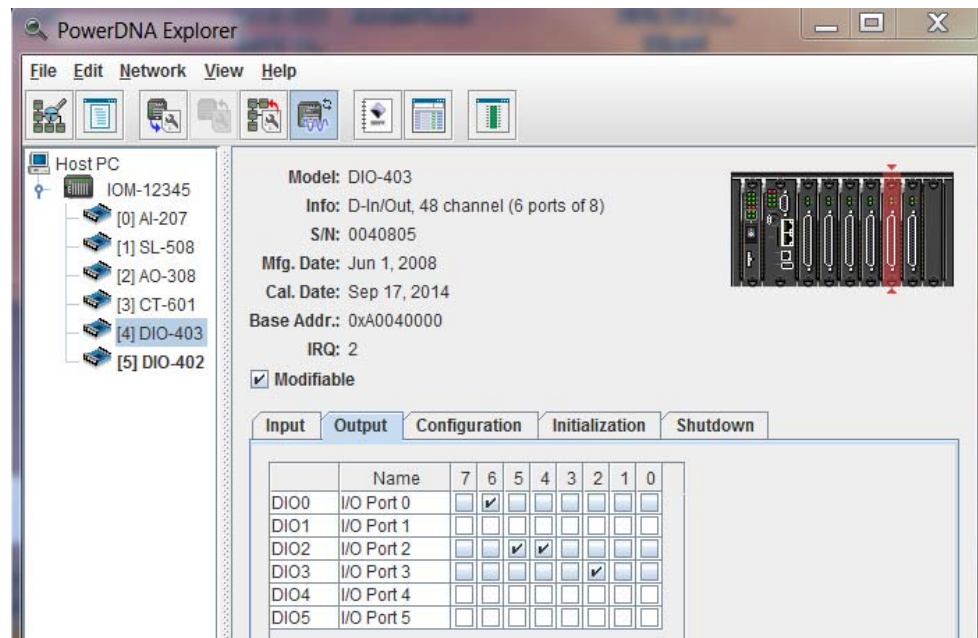


Figure 4-20. Example of DIO-403 Outputs

Output tabs set the current input/output values. They contain the following columns:

The Input tabs contain the following columns:

- **Name** is the channel (port) name, or a user-defined string.
- **7:0** Output values consist of the output state to be driven from the I/O pin: select 0 (unchecked) or 1 (checked).

The settings in Figure 4-20 will cause output high values on DIO pin 6, pin 20, pin 21, and pin 26. The settings will cause output low values on DIO pins 0, 1, 2, 3, 4, 5, 7, 16, 17, 18, 19, 22, 23, 24, 25, 27, 28, 29, 30, 31.

The rest of the pins are configured as inputs; input vs output configuration is set under the Configuration tab.



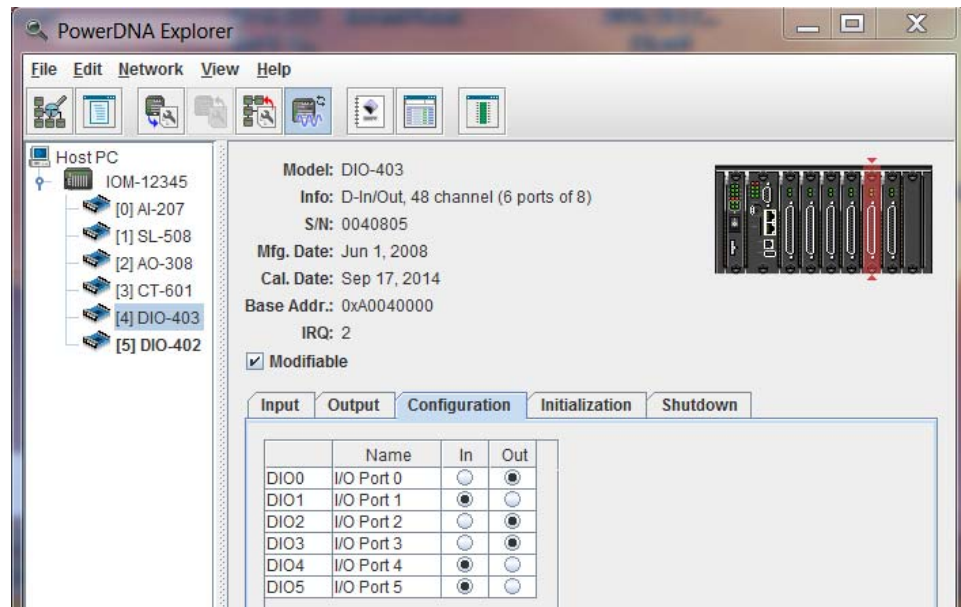


Figure 4-21. Example of DIO-403 Configuration

The **Configuration** tab gets/sets the current input/output directions per port. It contains the following columns:

- **Name** is the channel (port) name, or a user-defined string.
- **In/Out** contains toggle switches to select whether the channel is to be used for input or for output.

Initialization/Shutdown tabs allow you to set port as input or output, and set output values. They contain the following columns:

- **Name** is the channel (port) name, or a user-defined string.
- **Mode** specifies whether the channel is input or output.
- **7 through 0** contain the values 0 or 1. They are checkmarks for output channels that allow you to select 0 (unchecked) or 1 (checked).



4.5 Example of Analog Output Board Settings

This section provides an example of PowerDNA Explorer settings for analog output boards. Each type of analog output board will have displays specific to the features offered with that board. In this section, we use the AO-308 as an example.

NOTE: Use *Network >> Store Config* to save values to the board.

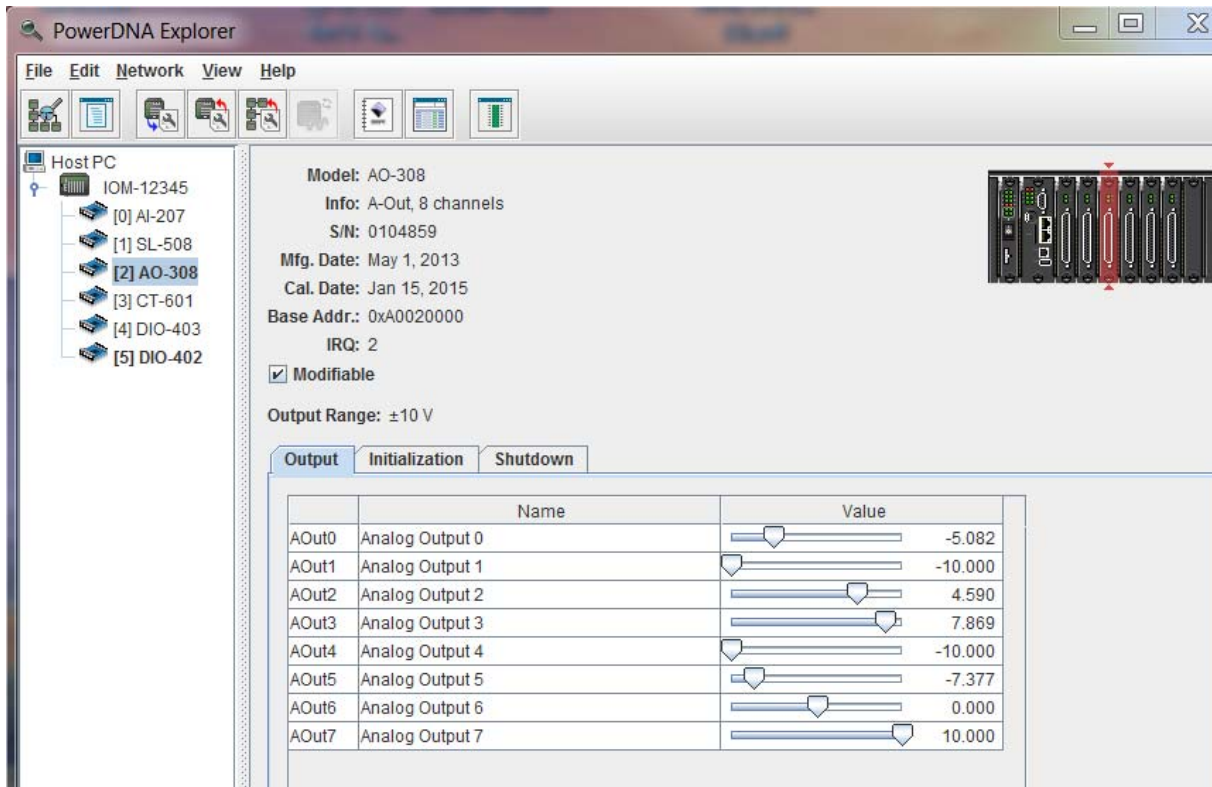


Figure 4-22. Example AO-308 Board

Controls for changing output, initialization, and shutdown values are available under each of the tabs in the settings panel. You can then choose *Network >> Store Config* to apply all changes to the board.

Output Range is displayed above the tabs. In this example, the output range cannot be changed and is informational only (the AO-308 output range is ± 10 V). On other boards, **Output Range** is a popup allowing you to choose between board-supported ranges.

The **Initialization** and **Shutdown** tabs contain controls for setting initial and shutdown states:

- **Name** is the channel name or a user-defined string.
- **Value** contains a slider to set the voltage to output for the channel and the numerical voltage value, which you can input directly.



4.6 Example of Analog Input Board Settings

This section provides an example of PowerDNA Explorer settings for analog input boards. Each type of analog input board will have displays specific to the features offered with that board. In this section, we use the AI-207 as an example.

NOTE: Use *Network >> Start Reading Input Data* to see immediate input values. Use *Network >> Store Config* to save values to the board.

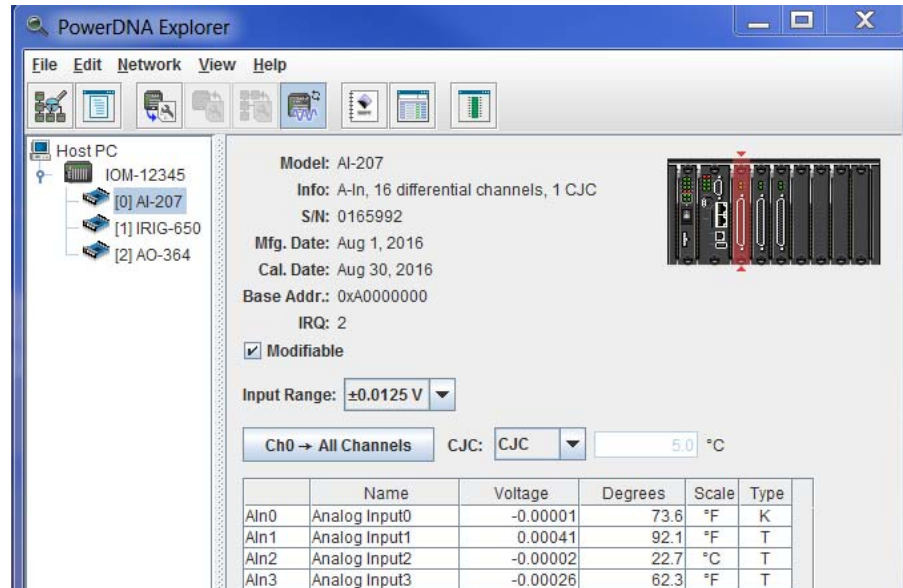


Figure 4-23. Example AI-207 Board

Input Range provides a pulldown menu of the range of expected input voltages to be measured by the board. On this board, the range can be specified as ± 10 V to ± 0.0125 V. Note if the actual voltage is outside of the range specified, the value displayed will clip at the maximum input range value.

The Data table contains the values currently read by the device. The table is initially blank until you refresh the data by clicking **Start Reading Input Data** (refer to Section 4.3.2).

The table for the AI-207 board in this example has the following columns:

- **Name** is the channel name or a user-defined string.
- **Value** shows the measured input value.
- **Degrees** shows the temperature converted from the measured input value.
- **Scale** provides a pulldown menu to select temperature scale (°C, °F, °K, °R) on a per channel basis.
- **Type** provides a pulldown menu to select thermocouple type (B, C, E, J, K, N, R, S, T) on a per channel basis.



4.7 Example of Counter/Timer Board Settings

This section provides an example of PowerDNA Explorer settings for counter/timer boards. Each type of I/O board will have displays specific to the features offered with that board. In this section, we use the CT-601 as an example.

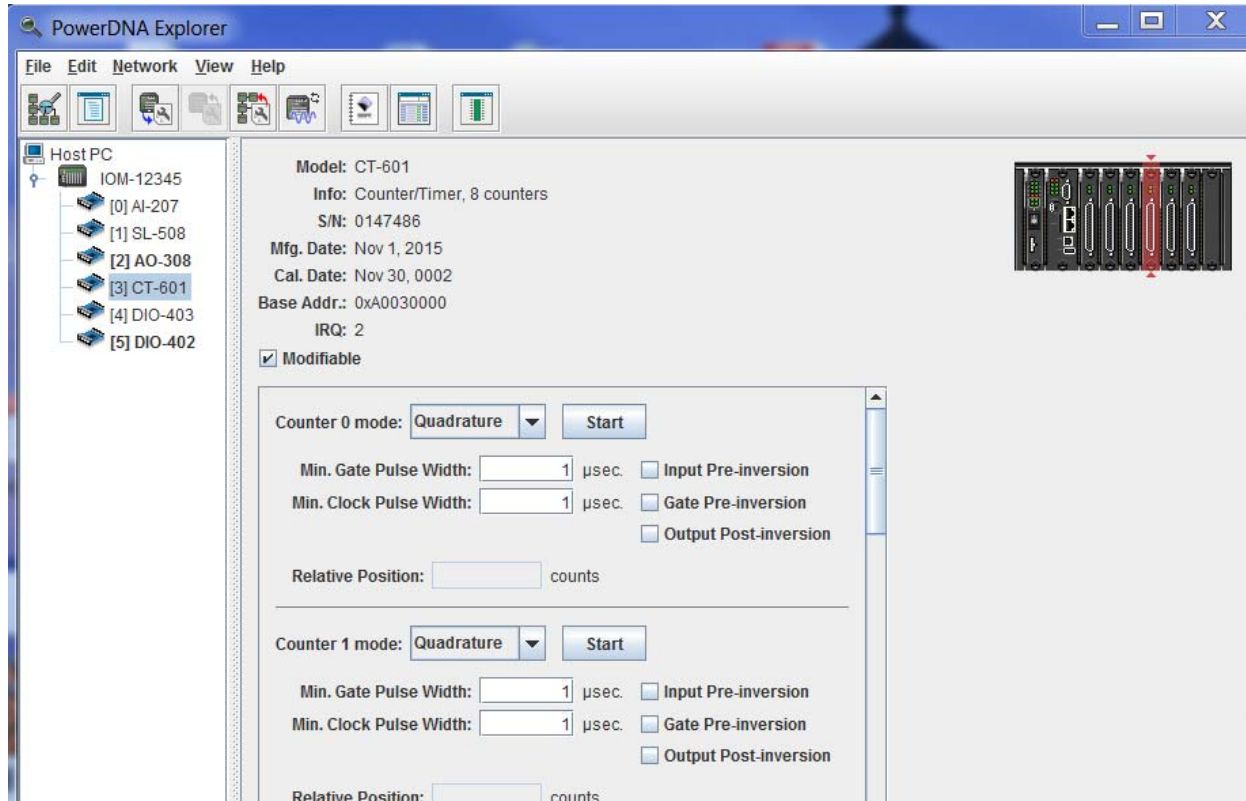


Figure 4-24. Example CT-601 Board

The CT-601 board has 8 counters. Each counter can be set to one of the different modes: Quadrature, Bin Counter, Pulse Width Modulation (PWM), Pulse Period, or Frequency.

When you change the mode of a counter using the mode pulldown menu, the controls for that counter will change to those appropriate for the mode.

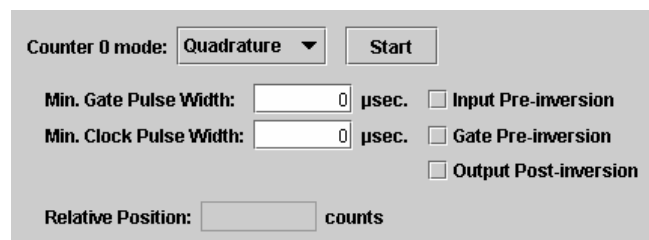


Figure 4-25. Example Quadrature Controls



Counter 0 mode: **Bin Counter** Start

Min. Gate Pulse Width: 0 μsec. ☐ Input Pre-inversion

Min. Clock Pulse Width: 0 μsec. ☐ Gate Pre-inversion

Prescaler Value: 33 ☐ Output Post-inversion

☐ Use External Clock

Counter Value:

Figure 4-26. Example Bin Counter Controls

Counter 0 mode: **PWM** Start

Duty Cycle: 50 % ☐ Output Post-inversion

Output Frequency: 1000 Hz (Actual Freq. = 1000 Hz)

Example Pulse Width Modulation (PWM) controls

Figure 4-27. Example Pulse Width Modulation (PWM) Controls

Counter 0 mode: **Pulse Period** Start

Min. Gate Pulse Width: 0 μsec. ☐ Input Pre-inversion

Min. Clock Pulse Width: 0 μsec. ☐ Gate Pre-inversion

Period Counter: 0 ☐ Output Post-inversion

Positive Count/Period: Frequency: Hz

Negative Count/Period:

Figure 4-28. Example Pulse Period Controls

Counter 0 mode: **Frequency** Start

Measurement Period: 0 μsec.

Measured Frequency: Hz

Figure 4-29. Example Frequency Controls

After setting the configuration for a counter, you can choose *Network >> Store Config* to store the settings on the device. Clicking the **Start** button will also write your configuration to the board.

Clicking the **Start** button for a counter will start that counter on the board. After clicked, the **Start** button will turn into a **Stop** button, and the other controls for that counter will become disabled until you click **Stop**.

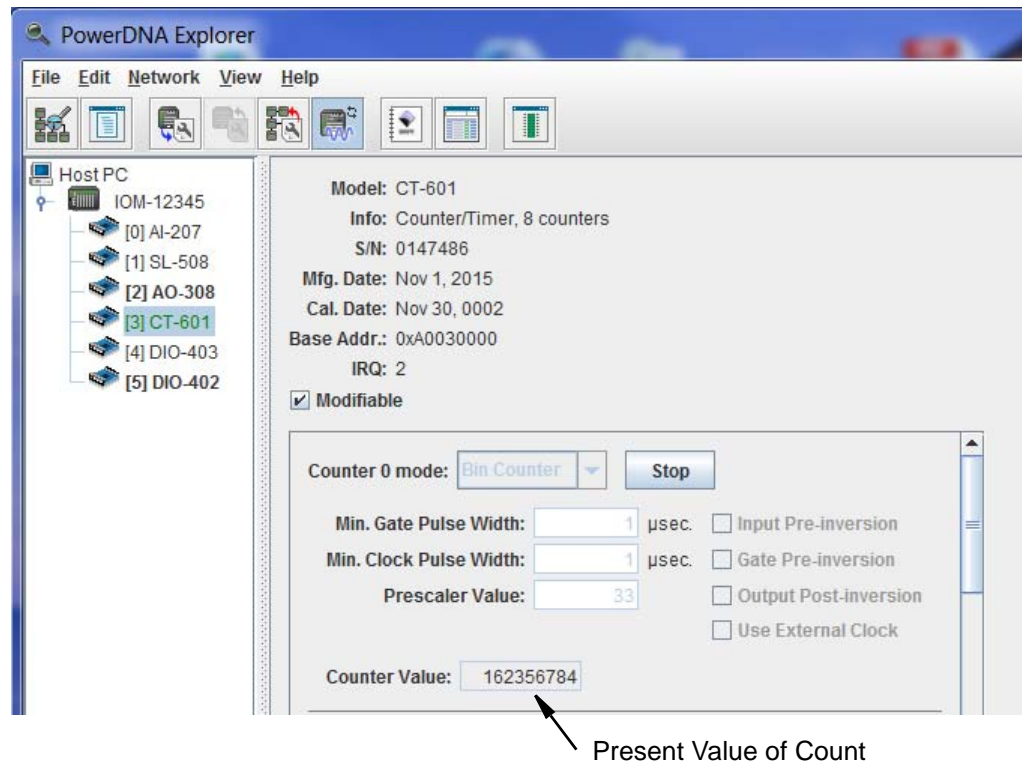


Figure 4-30. Example of Started Counter

While the board is running, you can choose *Network >> Store Config* to retrieve runtime values from the counter, which will display in the read-only text field(s) of the counter control panel.



Chapter 5 Programming CPU Board-specific Parameters

5.1 Overview

This chapter provides information about programming DNA-PPCx-1G CPU Core modules:

- Memory Maps (Section 5.2)
- Startup Sequence (Section 5.3)
- Setting and Reading CPU Core Parameters via Serial Port (Section 5.4)



Programming PowerDNA Products

This chapter primarily provides descriptions of configuration or diagnostic DNA-PPCx-1G CPU Core commands that can be issued over a serial terminal.

To program your application, please refer to example code and additional documentation, (e.g., getting started guides, API reference, synchronization documentation), that is provided with the installation.

5.2 Memory Maps

This section describes the memory maps for the PowerDNA CPU/NIC core modules (-00/-01, -02, and -03 versions).

NOTE: PowerDNA CPU/NIC board revisions align with product versions. For a list of for DNA-PPCx-1G product versions, refer to Section 1.3 on page 3.

Table 5-1 Memory Map for DNA-PPCx-1G CPU (-00/-01 CPU)

Device	Start Address	End Address	Size	Description
SDRAM	0x0	0x7FFFFFFF	128MB	SDRAM_ADDRESS
Exception table	0x0	0x3000	12 kB	Processor address map
CPU card address	0xA00E0000	0xA00EFFFF	64 kB	EXT_SRAM_ADDRESS
Processor RAMBAR	0xE0000000			
Module – CS2	0xA0000000	0xA00FFFFC	1 MB	EXT_DEV_ADDRESS2
Module – CS3	0xA0100000	0xA01FFFFC	1 MB	EXT_DEV_ADDRESS3
Flash (Linux kernel)	0xFE000000	0xFF7FFFFFFF	up to 24 MB	Linux kernel
Flash (firmware)	0xFF800000	0xFFEFFFFFFF	up to 7 MB	Firmware
Flash (U-Boot)	0xFFF00000	0xFFF5FFFF	approximately 320 kB	U-Boot
Flash (parameters)	0xFFF60000	0xFFFFFFFF	64 kB	Parameters (1 sector)



Table 5-2 Memory Map for DNA-PPCx-1G-02 CPU (-02 CPU)

Device	Start Address	End Address	Size	Description
SDRAM	0x0	0xFFFFFFFF	256MB	SDRAM_ADDRESS
Exception table	0x0	0x3000	12 kB	Processor address map
CPU card address	0xA00E0000	0xA00EFFFF	64 kB	EXT_SRAM_ADDRESS
Processor RAMBAR	0xE0000000			
Module – CS2	0xA0000000	0xA00FFFFC	1 MB	EXT_DEV_ADDRESS2
Module – CS3	0xA0100000	0xA01FFFFC	1 MB	EXT_DEV_ADDRESS3
Flash (Linux kernel)	0xFE000000	0xFF7FFFFFFF	up to 24 MB	Linux kernel
Flash (firmware)	0xFF800000	0xFFEFFFFFFF	up to 7 MB	Firmware
Flash (U-Boot)	0xFFF00000	0xFFF5FFFF	approximately 320 kB	U-Boot
Flash (parameters)	0xFFF60000	0xFFFFFFFF	64 kB	Parameters (1 sector)

Table 5-3 Memory Map for DNA-PPCx-1G-03 CPU (-03 CPU)

Device	Start Address	End Address	Size	Description
SDRAM	0x0	0xFFFFFFFF	256MB	SDRAM_ADDRESS
Exception table	0x0	0x3000	12 kB	Processor address map
CPU card address	0xA00E0000	0xA00EFFFF	64 kB	EXT_SRAM_ADDRESS
Processor RAMBAR	0xE0000000			
Module – CS2	0xA0000000	0xA00FFFFC	1 MB	EXT_DEV_ADDRESS2
Module – CS3	0xA0100000	0xA01FFFFC	1 MB	EXT_DEV_ADDRESS3
Flash (Linux kernel & ROM drive)	0xF8000000	0xFF7FFFFFFF	up to 120 MB	Linux kernel
Flash (firmware)	0xFF800000	0xFFEFFFFFFF	up to 7 MB	Firmware
Flash (U-Boot)	0xFFF00000	0xFFF5FFFF	approximately 320 kB	U-Boot
Flash (parameters)	0xFFF60000	0xFFFFFFFF	64 kB	Parameters (1 sector)

Two address ranges are notable for host software:

Module Address Space (0xA0000000 – 0xA00FFFFC and 0xA0100000 – 0xA01FFFFC). The first address range is dedicated for devices located on the CS2 line and it accommodates sixteen modules with 64k memory map each. The second address range is designated for fast devices located in the CS3 line and it accommodates fifteen devices with 16MB memory map each.



5.3 Startup Sequence

After reset, the processor reads the boot-up sequence located at the address shown in the memory maps in Section 5.2. The U-boot monitor initializes the processor and the address map, retrieves information from the parameter sector of the flash memory and tests system memory and other system resources.

When the DNA-PPCx-1G starts rebooting, you have the option of interrupting the reboot via a serial terminal connection between the DNA-PPCx-1G and a host PC. In the serial terminal window, if you type `<Return>` as U-Boot starts executing, the U-Boot sequence will be interrupted. The U-Boot monitor aborts loading firmware into memory and brings up the U-Boot command prompt `=>` (to load new firmware, for example).

Otherwise, U-Boot reads the firmware from the flash memory and stores it in RAM. Then, the monitor executes the firmware.

After initializing, U-Boot performs a command list stored in its environment sector under the `bootcmd` entry. A standard command to launch DNA-PPCx-1G firmware is `"go 0xff800100"`. U-Boot then gives up control to the firmware code located at `0xFF800100`. Firmware self-expands into the DDRAM, initializes the exception table, and starts execution.

5.4 Setting and Reading CPU Core Parameters via Serial Port

There are two ways to set CPU Core Module (CM) parameters. The first one is to use the serial interface and enter commands at the `DQ>` prompt, and the second one is the use of DAQBIOS calls by running an application on the host PC.

NOTE: The rest of this chapter provides descriptions of setting and reading CPU core parameters using the serial interface. For more information about accessing CPU core parameters via your application, please refer to the PowerDNA API Reference Manual.

To connect through the serial interface, do the following:

- Connect a 9-wire serial extender cable between the DNA-PPCx-1G CPU/NIC module (male plug connector) and your PC COM serial port (female connector). Some cables have female-to-female connectors, so you may have to use a gender-changer.
- Set up your terminal to the proper serial port, 57600 bit rate, no parity, eight data bits, and one stop bit.

NOTE: To use the MTTTY executable included with the UEI installation, open `mttty.exe` (available in the following directory on Windows machines), and then click **Connect**:

```
\Program Files(x86)\UEI\PowerDNA\Firmware\mttty.exe
```

- Once a connection to the Cube is established, press `<Enter>` on the keyboard once. The DNA-PPCx-1G should respond with a `"DQ>"` prompt (this is a firmware prompt). If you see a `"=>"` prompt, you are still in U-Boot.
- Once you see the `"DQ>"` prompt, you can type `"help <Enter>"` to receive the list of all available commands.



5.4.1 Help Command

The **help** command provides a list of available commands:

DQ> help

help	Display this help message	help
set	Set parameter	set option value
show	Show parameters	show
store	Store parameters (flash)	store
flrd	Re-read flash (flash)	flrd
mw	Write wr <addr><val> [width,b]	mw
mr	Read rd <addr>[width,b] [size]	mr
time	Show/Set time	time [mm/dd/yyyy] [hh:mm:ss]
pswd	Set password	pswd {user su}
ps	Show process state #	ps [value]
test	Test something	test [test number]
simod	System Init/Module Cal	simod [routine]
default	Default parameters	default
reset	Reset system	reset [all]
dqping	Send DQ_ECHO to <mac addr>	dqping
mode	Set current mode	mode {init config oper}[ID]
logf	Find entry in the log	logf marker [start [end]]
ver	Show firmware version	ver [all]
devtbl	Show all devices/layers	devtbl [logic verbose]
netstat	Show network statistics	netstat
pdj	Print device object	pdj <devno> cl
sd	SD Card Commands	sd <command> <arguments>
stat	Display status	stat [log]
nif	Display nif object	nif
clear	Clear terminal	clear



5.4.2 Show System Parameters Command

The **show** command is one of the most frequently used commands. **show** provides a list of DNA-PPCx-1G system parameters:

```
DQ> show
```

```
    name: "IOM-12345 "
  model: 3005
 serial: 0162789
option: 0001
  fwct: 1.2.0.0
   mac: 00:0C:94:02:7B:E5
   srv: 192.168.100.2
   ip: 192.168.100.100 (1Gbit)
gateway: 192.168.100.1
netmask: 255.255.255.0
  mac2: 00:0C:94:F2:7B:E5
  srv2: 192.168.100.102
  ip2: 192.168.100.102 (DOWN)
gateway2: 192.168.100.1
netmask2: 255.255.255.0
   udp: 6334
 license: "███"
bond prm: bonding mode: FFFFFFFF
Manufactured 7/27/2016
Calibrated 7/27/2016
```

To change parameters, use the “set” command (type **set** <Enter> for “set” command syntax).



5.4.3 Set and Store Commands

The **set** command allows you to change DNA-PPCx-1G system parameters and **store** allows you to save them to system memory (flash).

Typing `set <Enter>` provides a list of parameter names that can be changed.

```
DQ> set
Enter user password > *****

Valid 'set' options:
    name: <Device name>
    model: <Model id>
    serial: <Serial #>
    option: <Option>
    fwct: <autorun.runtype.portnum.umports>
    mac: <ethernet address port 1>
    srv: <Default IP address port 1>
    ip: <IOM IP address port 1>
    gateway: <gateway IP address port 1>
    netmask: <netmask port 1>
    mac2: <ethernet address port 2>
    srv2: <Default IP address port 2>
    ip2: <diagnostic port IP address>
    gateway2: <diagnostic port gateway IP>
    netmask2: <diagnostic port netmask>
    udp: <udp port (dec)>
    license: license string
    bond prm: license string
```

Table 5-4 Set Parameters

Set Parameter <Argument>	Description
name <Device name>	Sets the device name (up to 32 characters)
<model>	Device model (factory programmed, do not change)
<serial>	DNA-PPCx-1G serial number (factory programmed, do not change)
<mac or mac2>	DNA-PPCx-1G MAC Ethernet address (factory programmed, do not change)
fwct <autorun.runtype.portnum.umports>	Defines the behavior of the U-Boot upon boot-up. The following are valid values for each field. <ul style="list-style-type: none"> for “autorun”: <ul style="list-style-type: none"> 1 - copy firmware to SDRAM memory location and execute from there for “runtype”: 2 for the DNA-PPCx-1G for “portnum” and “umports” should be 0 (zero)
srv <Host IP address>	Sets the host IP address for connection with the IOM primary port (NIC1). You have to set the host IP address only if raw Ethernet protocol is in use (used in homogenous IOM networks only.) This parameter is ignored when the DNA-PPCx-1G system is used over the UDP protocol or from the host



Table 5-4 Set Parameters

Set Parameter <Argument>	Description
ip <IOM IP address>	Specifies the IOM primary IP address (NIC1). This is a critical parameter the user must change to allow the DNA-PPCx-1G system to be visible on the network. The DNA-PPCx-1G responds to every UDP packet containing a DaqBIOS prolog sent to this address. Since the current release does not support DHCP, the user should set up the IP address
gateway <gateway IP address>	Specifies where the DNA-PPCx-1G (NIC1) should send an IP packet if a requested IP packet exists outside of the DNA-PPCx-1G network (defined by the network mask)
netmask <network mask>	Specifies what type of subnet the DNA-PPCx-1G (NIC1) is connected to. The factory sets netmask to Type C IP network – 254 nodes maximum
srv2 <Host IP address>	Sets the host IP address for connection with the IOM diagnostic (secondary) port (NIC2)
ip2 <IOM IP address>	Specifies the IOM diagnostic (secondary) IP address (NIC2)
gateway2 <gateway IP address>	Specifies the IOM diagnostic (secondary) gateway (NIC2)
netmask2 <network mask>	Specifies the IOM diagnostic (secondary) subnet mask (NIC2)

NOTE: The **set** command may require a password. The default password for DNA-PPCx-1G systems is "powerdna".

5.4.4 Set and Store Example

The following are examples of setting DNA-PPCx-1G parameters:

- To set a new Primary IP address (NIC1), type
DQ> set ip 192.168.1.10
- To set a new Secondary Diagnostic Port IP address (NIC2), type
DQ> set ip2 192.168.100.3

Other parameters can be changed the same way. Refer to Section 5.4.3 for more information about each of the **set** parameters.

Once parameters are set, you must store them into non-volatile flash memory:

```
DQ> store
CRC: crc=0xDB097048 flcrc=DB097048
Flash: 1272 bytes of 1272 stored! CRC=0xDB097048
Old=0xC4F8C173
Xflash: 28 bytes CRC=35AA034B
Configuration stored
```

After parameters are stored, reset the firmware.



5.4.5 Reset Command

The **reset** command performs a physical reset of the CPU and initiates the full startup sequence on the DNA-PPCx-1G system:

```
DQ> reset
Stopping DaqBIOS

U-Boot 1.1.3 (PowerDNA 8347 3.2.4) (Mar 24 2014 - 12:31:23) MPC83XX

Clock configuration:
<...many U-Boot messages deleted...>
Net:   Freescale TSEC0:- PHY is Realtek RTL8212 (1cc912)
PHY is Freescale TSEC0
W:9140 rg:0 Gig-E controller found
W:1140 rg:0 EthController Freescale TSEC0
Hit any key to stop autoboot:  0
## Starting application at 0xFF800100 ...
Welcome to PowerDNA!
PowerDNA (C) UEI, 2001-2017. Running PowerDNA Firmware on MPC8347A
Built on 13:05:16 Aug 23 2017
RAM size:128MB Flash size:32MB
Initialize uC/OS-II (Real-Time Kernel v.280)
CM-4 PPC8347 detected
6 devices detected
```

Address	Irq	Model	Option	Phy/Virt	S/N	Pri	DevN
0xA0000000	2	207	1	phys	0165992	10	0
0xA0010000	2	650	1	phys	0154839	20	1
0xA0020000	0	364	1	phys	0170276	30	2
0xA0030000	2	217	1	phys	0153841	40	3
0xA00D0000	3	41	1	phys	0162573	30	4
0xA00E0000	3	4	1	cpu	0162491	0	14

```
-----
Current time: 10:19:54 08/30/2017
Starting filesystem... (H)
SD card is not present.
Power DNA version 4.10.0 release build 3
Built on 13:05:16 Aug 23 2017
396MHz MPC8347 DCache:32k uC/OS v.280 is running

Enter 'help' for help.

DQ>
```



5.4.6 Password Command

Some commands (such as `mr`, `mw`, `set`, and `store`) require entering a user password. Once the password is entered, these commands become enabled until firmware reset.

There are two levels of password protection available. The first is user level and the second is super-user level. Super-user level is currently used only for updating firmware over the Ethernet link.

- `DQ> pswd user` sets up a user level password.
First, you'll be asked to enter your current password and then (if it matches) to enter the new password twice.
- `DQ> pswd su` sets up super-user level password.
First, you'll be asked to enter your current super-user password and then (if it matches) to enter the new super-user password twice.

PowerDNA Cube systems come with both default passwords set to "powerdna". If you need to reset your password, use the following

- `DQ> pswd reset`

Some DaqBIOS commands require clearing up a user or super-user password. Use `DqCmdSetPassword()` before calling these functions. The PowerDNA API Reference Manual notes which functions are password-protected.

5.4.7 Display I/O Board Table Command

The `devtbl` command is a frequently used command.

This command displays all I/O boards found and initialized by firmware along with assigned device numbers.

Use these device numbers in host software to address the I/O devices.

```
DQ> devtbl
```

Address	Irq	Model	Option	Phy/Virt	S/N	Pri	DevN
0xA0000000	2	207	1	phys	0165992	10	0
0xA0010000	2	650	1	phys	0154839	20	1
0xA0020000	0	364	1	phys	0170276	30	2
0xA0030000	2	217	1	phys	0153841	40	3
0xA00D0000	3	41	1	phys	0162573	60	4
0xA00E0000	3	4	1	cpu	0162789	0	14

The `devtbl` command with the `logic` option added displays the CPU logic version on each installed I/O board:

```
DQ> devtbl logic
```

Logic information:

DevN	Mod-opt	Logic	CLI	CLO	LogOption
0	207-001	02.12.21	512	512	10127E0
1	650-001	02.11.36	1024	0	43000040
2	364-001	02.11.0A	0	4096	30000A0
3	217-001	02.11.9F	2048	512	90024E0
4	041-001	02.10.C4	0	0	1010081
14	3006-001	02.12.3E	0	0	30303720



The **devtbl** command with the **verbose** option added displays detailed information about each installed I/O board:

```
DQ> devtbl verbose
Logic capabilities:
Device:0 model:207-001
    - Sample counters are available
    - Logic compiled for CYCLONE family
    - 16.5MHz serial isolation interface speed based on 66MHz system
clock
    - 2-wire interface is used
    - Includes NIS-->IS serializer
    - Includes IS-->NIS deserializer
    - PWM output enabled for the TMR0/TMR1 timers in SYNC module
    - Standard input channel list implementation used
    - Standard output channel list implementation used

Device:1 model:650-001
    - Sample counters are available
    - Standard input channel list implementation used

Device:2 model:364-001
    - Sample counters are available
    - PWM output enabled for the TMR0/TMR1 timers in SYNC module
    - Standard output channel list implementation used

Device:3 model:217-001
    - Sample counters are available
    - 16.5MHz serial isolation interface speed based on 66MHz clock
    - 2-wire interface is used
    - PWM output enabled for the TMR0/TMR1 timers in SYNC module
    - Standard input channel list implementation used
    - Standard output channel list implementation used

Device:4 model:041-001
    - Sample counters are available
    - Logic compiled for CYCLONE family
    - PWM output enabled for the TMR0/TMR1 timers in SYNC module
    - 8-bit output test port is unavailable

DQ>
```



- 5.4.8 Display Power Diagnostics Command** Typing `simod 5` at the serial prompt displays diagnostic information about the DNA-PPCx-1G Power and CPU boards. This diagnostic information includes actual voltage readings on each of the 2.5 V, 24 V, 1.2 V, 3.3 V, and 1.5 V supplies, as well as actual temperature and current measurements.

```
DQ> simod 5

DNA_PWR_1G layer diagnostics

2.5DNx= 2.521*      GND1= 0.000*
3.3DNx= 3.316*      U-Cap= 0.022*
24DNx=24.101*      Vin=23.950*
1.5DNx= 1.507*      1.2DNx= 1.217*
VfanX= 8.968*      Iin= 0.473*
I 3.3= 0.590*      I 1.5= 0.744*
Temp1=47.071*      Temp2=47.105*
Unit logged 1375.8 hours
```

DQ>

Readings displayed under “DNA_PWR_1G layer diagnostics” show diagnostics for the DNA-CPU/NIC Module. Refer to Section 2.6 on page 11 for more information.

- 5.4.9 Memory Test/Memory Clear Command** Typing `simod 7` performs a memory test on the DNA-PPCx-1G CPU address space.
- The test writes standard memory test bit patterns to each memory location and then reads each location back and verifies. At the end, it reports any bit mismatches.
- Note that this memory test writes over any content in that memory space; therefore, it can be used to clear memory, as needed.

```
DQ> simod 7
Memory test/clear
Clear memory and reboot? y/[n]>n
CPU layer memory test
Start addr=0x00200000 End addr=0x07FFFFFFC (125MB)
Total errors: 0
DQ>
```

Typing “y” after “Clear memory and reboot? y/[n]>” causes the chassis to automatically reboot.

```
DQ> simod 7
Memory test/clear
Clear memory and reboot? y/[n]>y
CPU layer memory test
Start addr=0x00200000 End addr=0x07FFFFFFC (125MB)
ADDR: 0x04C00000 (76MB) errors=0
```

<...memory test completes and then system reboots...>



**5.4.10 Monitor CPU
and Pbuf
Usage
Command**

Entering `simod 15` at the serial command prompt causes the CPU and packet buffer load to continuously print to the serial console.

`simod 15` can be used to monitor the DNA-PPCx-1G serial port while your application is sending and receiving control words and data over Ethernet.

```
DQ> simod 15
Printing statistics
+cpu:1 pbuf:avail:576 used:20 max:20 err:0
+cpu:12 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
```

**5.4.11 Clock and
Watchdog
Access
Command**

The `time` command shows and sets up the date and time on the DNA-PPCx-1G system:

```
DQ> time
Current time: 14:56:17 09/01/2017
```

To set up time of the time of day, enter:

```
DQ> time 17:40:00
```

To set up date, enter:

```
DQ> time 11/03/2017
```

Date and time are stored in the battery-backed real-time clock chip.



Appendix A

Network Interface Card Configuration

A.1 Configuring an Ethernet Card on Windows 7

To configure an Ethernet card for your system, use the following procedure:

A. Set Up Your Ethernet Network Interface Card (NIC).

If you already have an Ethernet card installed, skip ahead to the next section, "B. Configure TCP/IPv4."

If you have just added an Ethernet card, to install it, do the following:

- STEP 1:** From the *Start* menu, and select *Control Panel*.
- STEP 2:** Under *Printers and Other Hardware*, click *Add a device* and follow the on-screen instructions.

NOTE: We recommend that you allow Windows to search for and install your Ethernet card automatically. If Windows does not find your Ethernet card, you will need to install it manually by following the manufacturer's instructions.

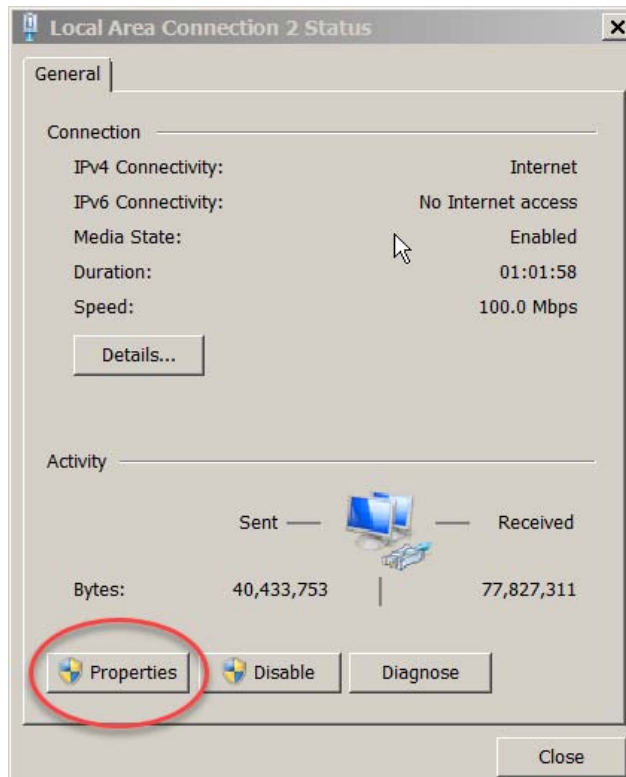
Once your Ethernet card has been installed, continue to the next section.

B. Configure TCP/IPv4.

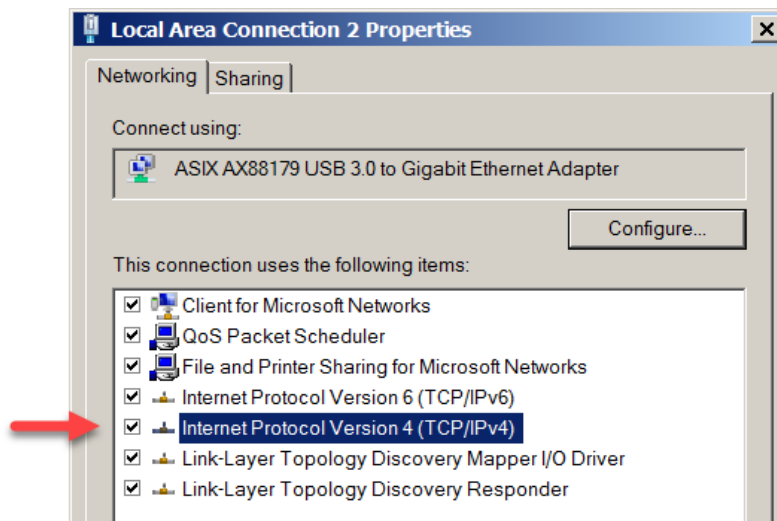
- STEP 1:** From the *Start* menu, select *Control Panel*.
- STEP 2:** In the Control Panel window, click *Network and Internet*.
- STEP 3:** In the Network and Internet window, click *Network and Sharing Center*.
- STEP 4:** In the left sidebar of the Network and Sharing Center window, click *Change adapter settings*.
- STEP 5:** Double-click the icon for the network interface you are connecting as your second NIC. This is typically under a *Local Area Connection* heading.



STEP 6: In the Local Area Connection Status window, click **Properties**:



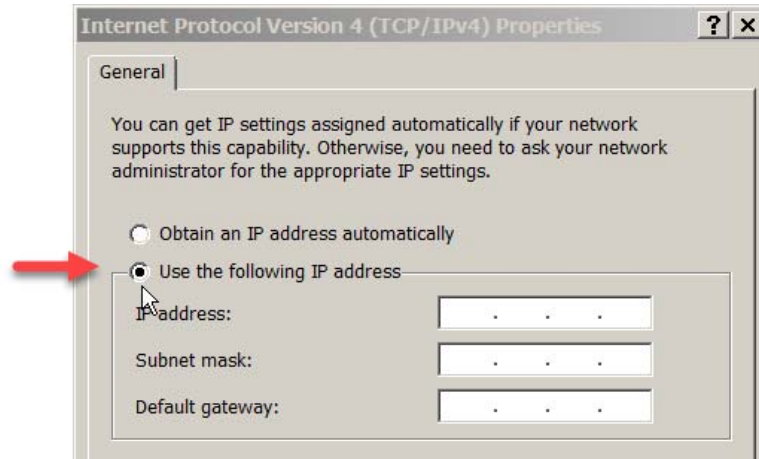
STEP 7: In the Local Area Connection Properties window, verify the Networking tab is selected, and double-click *Internet Protocol Version 4 (TCP/IPv4)*.



STEP 8: If Internet Protocol (TCP/IPv4) is not listed, click **Install** and follow directions on the screen.



STEP 9: Click the *Use the following IP address* button (see Figure below). Note any addresses listed in the *IP Address*, *Subnet Mask*, *Default Gateway*, *Preferred DNS Server* or *Alternate DNS Server* fields. You may want to re-enter them later to reconfigure your PC, if needed.



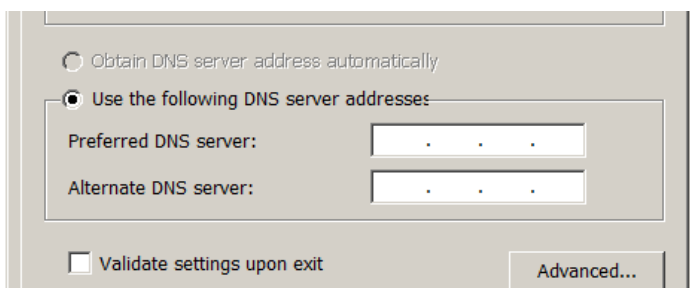
In the *IP address* field, type the IP address for the host PC NIC port (e.g., 192.168.100.1) .

In the *Subnet mask* field, type 255.255.255.0.

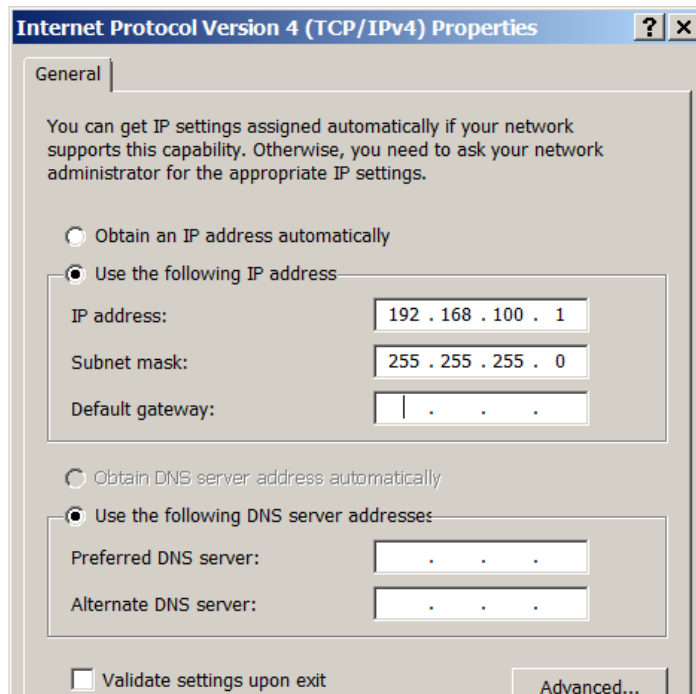
Leave the *Default Gateway* field blank.

NOTE: In the above example, setting the host PC NIC address to 192.168.100.1 with a subnet mask of 255.255.255.0 allows the host PC to communicate with components having IP addresses from 192.168.100.2 through 192.168.100.254 via that NIC port. All UEI cubes and racks on this network will need to have IP addresses unique and in that range. (The default IP address of the UEI RACKtangle / HalfRACK is 192.168.100.2.)

STEP 10: Select *Use the following DNS server addresses* and verify the *Preferred DNS server* fields and the *Alternate DNS server* fields are blank.



STEP 11: Click **OK** in the *TCP/IPv4 Properties* window (see figure below).



STEP 12: Click **OK** in the *Local Area Connection 2 Properties* window, and click **Close** in the *Local Area Status* window.

STEP 13: **Close** the *Control Panel* window.



For instructions to set the IP address, subnet mask, and default gateway on a UEI chassis, refer to “IP Address Overview & Update Procedures” on page 21.



Appendix B

Field Replacement of Fuses on DNA Boards

Some boards used in UEI DAQ I/O systems require field replacement of fuses when unexpected overloads occur. Locations of these fuses are shown in **Figure B-1** through **Figure B-2**. Part numbers for the replacement fuses are listed **Table B-1**.

Table B-1. DNA/DNR Replacement Fuses

UEI Fuse ID (Board)	Rating	UEI Part No.	Description	Mfr.	Mfr P/N
F1	5A	925-5125	FUSE 5A 125V SLO SMD SILVER T/R	Littlefuse	0454005.MR
F2	5A	925-5125	FUSE 5A 125V SLO SMD SILVER T/R	Littlefuse	0454005.MR
F3 (1GB)	10A	925-1125	FUSE 10A 125V FAST NAN02 SMD	Littlefuse	0451010.MRL

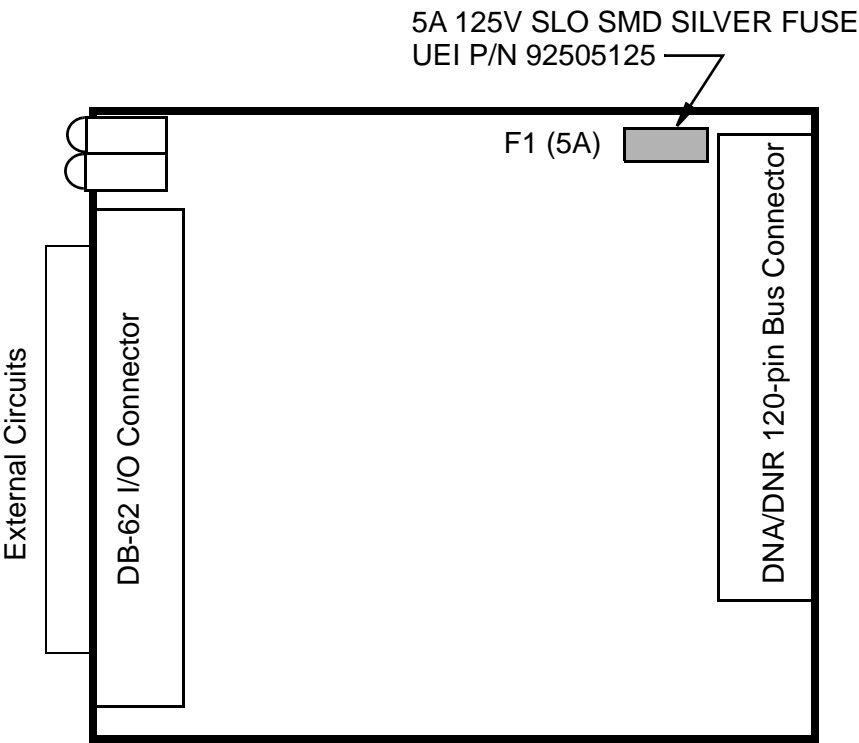


Figure B-1. Location of Fuse for Fuse-Equipped Base Boards

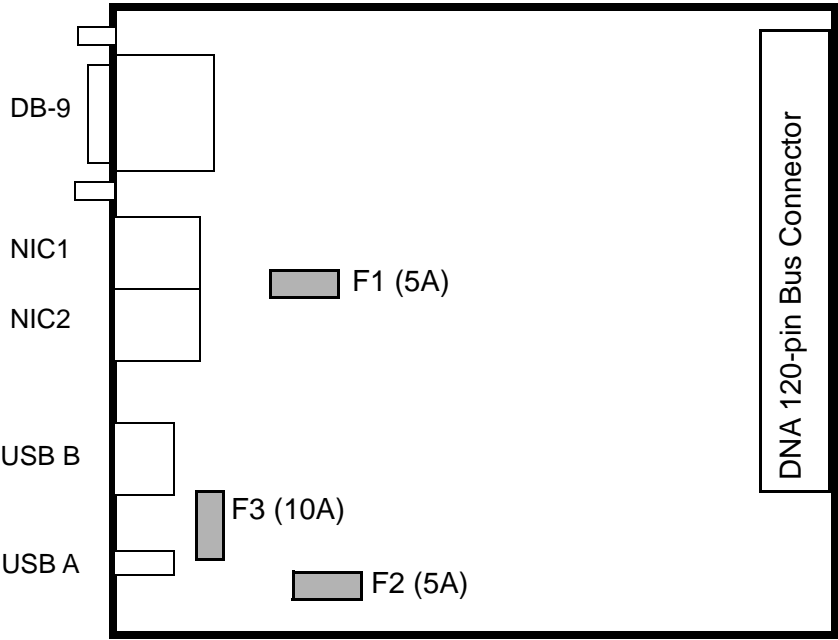


Figure B-2. Location of Fuses for DNA-POWER-1GB Board

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