

DNF-4-1G Series FLATRACK[™] Data Acquisition System — User Manual

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Chapter 1 Introduction

This document describes the features, performance specifications, and operating functions of the DNF-4-1G FLATRACK[™] data acquisition system. The system is available in an AC-powered version and a DC-powered version, DNF-4-1G-AC and DNF-4-1G-DC respectively.

This chapter provides the following information about the DNF-4-1G systems:

- Organization of This Manual (Section 1.1)
- Product Versions Described in This Manual (Section 1.2)

1.1 Organization of This Manual

This DNF-4-1G User Manual is organized as follows:

Chapter 1 – Introduction

This chapter describes the organization of the document and the conventions used throughout the manual.

• Chapter 2 – DNF-4-1G Series FLATRACK™ System

This chapter provides an overview of a DNF-4-1G system, features, accessories, and a list of all items you need for initial operation.

• Chapter 3 – Installation and Configuration

This chapter summarizes the recommended procedures for installing, configuring, starting up, and troubleshooting a DNF-4-1G system.

Chapter 4 – PowerDNA Explorer

This chapter provides a general description of the menus and screens of UEI's GUI-based communication application, PowerDNA Explorer, when used with a DNF-4-1G system.

- Chapter 5 Programming CPU Board-specific Functions
 This chapter describes programming the DNF-4-1G CPU.
- Appendix A Configuring Ethernet Cards

This appendix describes procedures for installing and configuring Network Interface Cards (NICs) for use with Windows operating systems.

Appendix B – Field Replacement of Fuses

This appendix describes procedures for replacing fuses in the field.

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This is an alphabetical listing of topics covered in the manual, identified by page number.

Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:



Tips are designed to highlight quick ways to get the job done or reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.



CAUTION! advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.

Text formatted in **bold** typeface generally represents text that should be entered verbatim. For instance, it can represent a filenames, as in the following example: "You can instruct users how to run setup using **setup.exe** executable."

Bold typeface will also represent button names, as in "Click Scan Network."

Text formatted in fixed typeface generally represents commands, source code, or other text that should be entered verbatim into the source code, initialization, or other file or at a command prompt.



Before plugging any I/O connector into the FLATRACK or I/O boards, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

Usage of Terms



Throughout this manual, the term "RACK" refers to either a RACKtangle/ HalfRACK product or to a FLATRACKTM rack mounted system, whichever is applicable.

Additionally throughout this manual, the following conventions apply:

- "DNF-4-1G" refers to both DNF-4-1G-AC and DNF-4-1G-DC types of systems. The DNF-4-1G-AC defines the AC-powered version and DNF-4-1G-DC is the DC-powered version. The two models are identical in all other respects.
- Unless otherwise noted, "DNF-4-1G" applies to all versions of the FLATRACK systems: DNF-4-1G, DNF-4-1G-02, and DNF-4-1G-03.
 Differences between product versions are noted on the following page.

1.2 Product Versions Described in This Manual

This user manual provides documentation for the DNF-4-1G series data acquisition systems: the DNF-4-1G, DNF-4-1G-02, and DNF-4-1G-03 product versions.

Each product version is available in a DNF-4-1G-AC FLATRACK version or a DNF-4-1G-DC FLATRACK version.

Table 1-1 below provides a summary of features for each product version. Refer to the following chapters in this manual for detailed descriptions.

NOTE: Unless otherwise noted, DNF-4-1G refers collectively to the DNF-4-1G, DNF-4-1G-02, and DNF-4-1G-03 series of products.

Table 1-1 Summary of DNF-4-1G/DNF-4-1G-XX Product Versions

Item	Summary of Features
DNF-4-1G	10/100/1000Base-T Ethernet interface
	Freescale MPC8347 CPU
	 1PPS synchronization support¹
	• 128MB RAM ²
	• 32MB flash memory ²
DNF-4-1G-02	10/100/1000Base-T Ethernet interface
	Freescale MPC8347 CPU
	1PPS/IEEE-1588 synchronization support ¹
	 Optional solid-state hard drives³
	• 256MB RAM ²
	32MB flash memory ²
DNF-4-1G-03	10/100/1000Base-T Ethernet interface
	 Freescale MPC8347E CPU, (encryption-ready / IPSec support pending)
	 1PPS/IEEE-1588 synchronization support¹
	 Optional solid-state hard drives³
	• 256MB RAM ²
	• 128MB flash memory ²

^{1.1}PPS and IEEE-1588 synchronization support is described in the PowerDNx 1PPS Sync Interface Manual.

^{2.}RAM and flash memory are not user-accessible for PowerDNA applications (hosted deployment). Portions of RAM and flash are available for UEIPAC-based systems (stand-alone deployment). See UEIPAC documentation for more information.

^{3.}On UEIPAC-based systems (stand-alone deployment), solid state drives are used for data and/or root file system storage. See UEIPAC documentation for more information.

Chapter 2 DNF-4-1G FLATRACK System

This chapter provides the following information about the DNF-4-1G Series FLATRACK™ system:

- DNF-4-1G System Overview (Section 2.1)
- DNF-4-1G Specifications (Section 2.2)
- DNF-4-1G Key Features (Section 2.3)
- DNF-4-1G FLATRACK Enclosure (Section 2.4)
- DNF-4-1G NIC/CPU and I/O Boards LEDs & Controls (Section 2.5)
- DNF-CPU/NIC Module (Section 2.6)
- DNF I/O Boards (Section 2.7)

NOTE: For a list of product versions available for the DNF-4-1G Series FLATRACK systems, refer to Section 1.2 on page 3.

2.1 DNF-4-1G System Overview

UEI's DNF-4-1G FLATRACK $^{\text{TM}}$ system is a compact, rugged and highly integrated Ethernet-based data acquisition platform.

The DNF-4-1G provides a low-profile footprint for space-constrained applications that require up to four I/O boards per chassis, in the form factor of a 1U rack-mounted version of UEI's PowerDNA Cube Ethernet-based data acquisition system.

All standard DNA- Cube I/O boards are also available as DNF- RACK versions for use in DNF-4-1G systems.



Figure 2-1. Typical DNF-4-1G FLATRACK System

A standard DNF-4-1G rack system consists of the following:

- One or more DNF-4-ENCL rack mounted enclosure(s)
- DNF-CPU-1000 or DNF-CPU-1000-XX Module (Freescale MPC8347 or MPC8347E CPU and 1-GB Ethernet 1000 Base-T Network Interface Module — one for each enclosure)
- Optional DNF-IO-FILLER panel (for unused I/O slots)
 Note: Slot covers are optional and not included in the price of the rack

To configure a complete data acquisition system, insert up to 4 DNF I/O boards into each DNF- rack enclosure. I/O boards may be specified in any combination of UEI's I/O boards.

All standard PowerDNA accessories are also available for use in a DNF-4-1G rack-mount system.

NOTE: For detailed descriptions of all I/O boards and accessories available for DNF-4-1G systems, refer to www.ueidag.com.



UEI stand-alone systems (UEIPAC, UEISIM, UEIModbus, and UEIOPCUA deployments) are also available for use with DNF-4-1G RACK systems:

- UEIPAC 400R Programmable Automation Controller
- UEISIM 400R Simulink / Simulink Coder Target
- UEIModbus 400R Modbus TCP-based Controller
- UEIOPCUA 400R OPC-UA Server, accessed by any OPC-UA client

2.2 DNF-4-1G Specifications

Figure 2-2 lists the technical specifications of the DNF-4-1G system.

Standard Interfaces	
To Host Computer	Two independent 1000Base-T Gigabit Ethernet
	ports (100/10Base-T compatible)
Distance from host	100 meters, max
Other Interfaces	One USB 2.0 controller, One USB 2.0 slave port.
Config/General	RS-232, 9-pin "D"
Sync	Custom cable to sync multiple racks
I/O Slots Available	castom caste to syne manapie racks
DNF-4-1G	4 slots
Allowable I/O configs	Any DNF-series I/O boards may be installed in
7 movable i, o comigs	any of the four slots.
Data transfer and com	munications rates
Ethernet data	20 megabytes per second
transfer rate	
Analog data	up to 6 megasample per sec (16-bit samples)
transfer rate	
DMAP I/O mode	update 1000 I/O channels (analog and/or digital)
	in less than 1 millisecond, guaranteed
Processor	
CPU	Freescale 8347, 400 MHz, 32-bit
Memory	128 MB (not including on-board Flash)
Status LEDs	Power supplies within spec, One second system
	heart-beat, Attention, Read/Write, Power, Com-
	munications Active
Environmental	
Temp (operating)	Tested to -40 °C to 70 °C
Temp (storage)	-40 °C to 85 °C
Humidity	0 to 95%, non-condensing
Vibration	
(IEC 60068-2-64)	10–500 Hz, 3 g (rms), Broad-band random
(IEC 60068-2-6)	10–500 Hz, 3 g, Sinusoidal
Shock	
(IEC 60068-2-27)	50 g, 3 ms half sine, 18 shocks at 6 orientations;
	50 g, 11 ms half sine, 18 shocks at 6 orientations
RoHS	All DNF series products are fully RoHS compliant
EMC testing	Fully CE/CSA/FCC tested and certified
MTBF	130,000 hours
Physical Dimensions	
	(" · 1 7 5" · 17 5" (AC an DC madel)
Size	6" x 1.75" x 17.5" (AC or DC model)
Weight (not including	DNF-4-1G-DC: 3.5 Lbs (1.6 kg)
Weight (not including I/O boards)	
Weight (not including	DNF-4-1G-DC: 3.5 Lbs (1.6 kg) DNF-4-1G-AC: 4.0 Lbs (1.8 kg)
Weight (not including I/O boards)	DNF-4-1G-DC: 3.5 Lbs (1.6 kg)
Weight (not including I/O boards) Power Requirements	DNF-4-1G-DC: 3.5 Lbs (1.6 kg) DNF-4-1G-AC: 4.0 Lbs (1.8 kg)
Weight (not including I/O boards) Power Requirements Voltage	DNF-4-1G-DC: 3.5 Lbs (1.6 kg) DNF-4-1G-AC: 4.0 Lbs (1.8 kg) 9 - 36 VDC, 100 - 240 VAC (50-60 Hz)
Weight (not including I/O boards) Power Requirements Voltage Power Dissipation	DNF-4-1G-DC: 3.5 Lbs (1.6 kg) DNF-4-1G-AC: 4.0 Lbs (1.8 kg) 9 - 36 VDC, 100 - 240 VAC (50-60 Hz)
Weight (not including I/O boards) Power Requirements Voltage Power Dissipation Power Monitoring	DNF-4-1G-DC: 3.5 Lbs (1.6 kg) DNF-4-1G-AC: 4.0 Lbs (1.8 kg) 9 - 36 VDC, 100 - 240 VAC (50-60 Hz) 8 W (not including I/O boards) All internal power supplies monitored to ±1% accuracy. All internal PS voltages may be read by
Weight (not including I/O boards) Power Requirements Voltage Power Dissipation Power Monitoring Internal power supplies	DNF-4-1G-DC: 3.5 Lbs (1.6 kg) DNF-4-1G-AC: 4.0 Lbs (1.8 kg) 9 - 36 VDC, 100 - 240 VAC (50-60 Hz) 8 W (not including I/O boards) All internal power supplies monitored to ±1% accuracy. All internal PS voltages may be read by host. LED annunciators indicate out of range
Weight (not including I/O boards) Power Requirements Voltage Power Dissipation Power Monitoring Internal power sup-	DNF-4-1G-DC: 3.5 Lbs (1.6 kg) DNF-4-1G-AC: 4.0 Lbs (1.8 kg) 9 - 36 VDC, 100 - 240 VAC (50-60 Hz) 8 W (not including I/O boards) All internal power supplies monitored to ±1% accuracy. All internal PS voltages may be read by

Figure 2-2. DNF-4-1G Technical Specifications

2.3 DNF-4-1G Key The following table is a list of key features of a DNF-4-1G system. **Features**

Easy to Configure and Deploy

- Gigabit Ethernet based (100/10Base-T compatible)
- Bracket kits for mounting to surfaces or in 19" racks
- Passive backplane ensures extremely low MTTR
- Standard "Off-the-shelf" products and delivery
- 10 year availability guarantee

True Real-time Performance

- 1 msec updates guaranteed with 1,000 I/O
- Up to 6 million samples per second
- Use QNX, RTX, Linux, VxWorks, InTlme and more

Flexible Connectivity

- 1000Base-T with Cat-5/5e cable
- Dual IP addresses (one control, one diagnostic)
- Built-in USB 2.0 slave and controller ports

Compact Size:

- 7.2" x 1.75" x 17.5" (including optional AC power module)
- 100 analog inputs per rack
- 128 analog outputs per rack
- 192 digital I/O bits per rack
- 32 counter/quadrature channels per rack
- 48 ARINC-429 channels per rack
- 32 RS-232/422/485 ports per rack

Low Power:

- Less than 8 watts per chassis (not including I/O)
- Universal AC, 9-36 VDC or battery powered

Stand alone Modes

- Upgradeable to UEISIM 400R
- Upgradeable to UEIPAC 400R
- Upgradeable to UEIModbus 400R

Rugged and Industrial:

- Solid Aluminium construction
- 130,000 hour MTBF
- Operation tested from -40°C to +70°C
- Vibration tested to 3 g, (operating)
- Shock tested to 50 g, (operating)
- All I/O isolated from rack and host PC

Outstanding Software Support

- Windows, Linux, RTX, InTime, VxWorks and QNX operating systems
- VB, VB .NET, C, C#, C++
- MATLAB, LabVIEW, OPC, ActiveX support

Figure 2-3. DNF-4-1G Product Features

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2.4 DNF-4-1G FLATRACK Enclosure

This section describes the DNF-4-1G chassis and provides an overview of common components included in every DNF-4-1G system.

2.4.1 DNF-4-1G Enclosure

The DNF-4-1G enclosure is a rigid mechanical structure with complete EMI shielding (see **Figure 2-4** below). An unused slot can be filled with filler panels.

The DNF-4-1G is available in AC or DC powered versions. The DC version requires a DC power source between 9 and 36 Volts. The AC unit operates from 100 to 240 VAC, from 50 to 60 Hz. The power module provides output voltages of 24, 3.3, 2.5, 1.5, and 1.2 VDC for the logic/CPU and 8 VDC to power cooling fans.

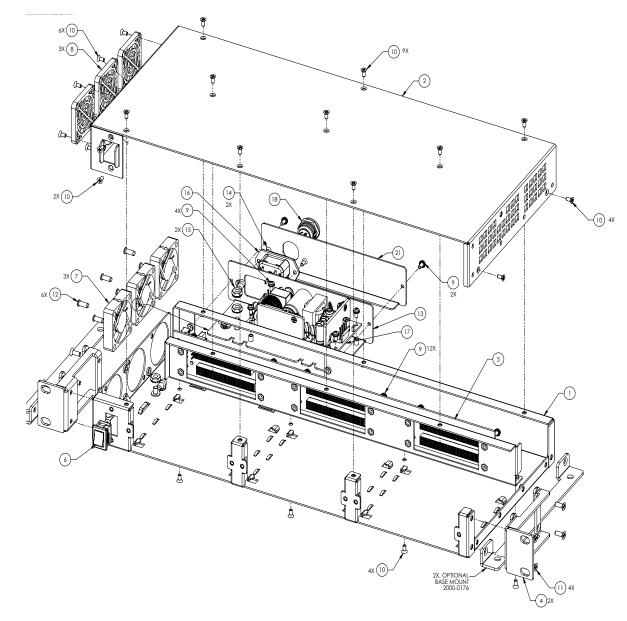


Figure 2-4. Typical DNF-4-1G Enclosure (Exploded View)

Table 2-1 DNF-4-1G Parts List (Refer to Figure 2-4 on the previous page)

Item No.	DNF-4-1G-AC Quantity	DNF-4-1G-DC Quantity	Description (Vendor/Vendor Part No.)
1	1	1	Chassis, DNF-4-1G Base
2	1	1	Chassis, DNF-4-1G Cover
3	1	1	Support, DNF-4-1G Backplane
4	2	2	Bracket, Mounting, 19" RACK, DNF-4-1G
5	1	1	Backplane Assembly, PCB, DNFBP4-RA DNFBP4-RA
6	1	1	Power Switch, Rocker, SNAP-IN, 2A 250VAC ITT DA102J12S215PQF
7	3	3	Fan, Axial, 40x10mm
8	3	3	Filter Assembly, 40MM FAN QUALTEK 09150-F/30PPI
9	18	14	Screw, #4-40x.250, PAN HD, PH, SEMS, SQ CONE 1001- 028
10	25	25	Screw, #4-40x¼,82° FH,PHIL,SST,BLK OXIDE 1001-082
11	8	8	Screw, #6-32x.375,100D FH,PHIL,SST,BLK OXIDE 1001- 375
12	6	6	Screw, M3.9x1.2 x 10.5mm, FH, PHIL, FAN MOUNT PENCOM M3.9 X 10.5mmPHFL-FAN-NI
13	1	NA	Plate, Mounting, CUI POWER SUPPLY 2000-0178
14	2	NA	Screw, Oval Head, #4-40 X .250, SLT/Z MCMASTERCARR 91802A106
15	3	NA	Nut, Hex, KEPS, #8-32
16	1	NA	Connector, AC Inlet, IEC 320 SCHURTER 6100-3300
17	1	NA	Power Supply, 60W, 24VDC, 2"X4" CUI INC VMS-60-24
18	NA	1	Connector, RCPT, MINI CIRC DIN, 4P CUI SD-40LS
21	NA	1	Plate, Mounting, CUI POWER SUPPLY 2000-0184

2.4.2 DNF-4-1G Enclosure Common Components

Each DNF-4-1G chassis contains a CPU board with a dedicated GigE CPU and two Network Interface Control (NIC) ports, one for controlling up to 4 I/O boards mounted in the enclosure and another for diagnostic functions. Front-loading slots allow I/O boards to be quickly and easily installed and removed, as needed.

Up to 4 DNF- I/O boards can be installed in the chassis; DNF- I/O boards are functionally identical to the corresponding DNA boards for the PowerDNA Cube. The only differences between RACK and Cube I/O boards are the mounting hardware. The DNA version I/O boards are designed to stack in a Cube chassis. The DNR/DNF version I/O boards are designed to plug into the backplane of a RACK chassis. UEI recommends unused slots be covered with filler panels to allow for proper cooling.

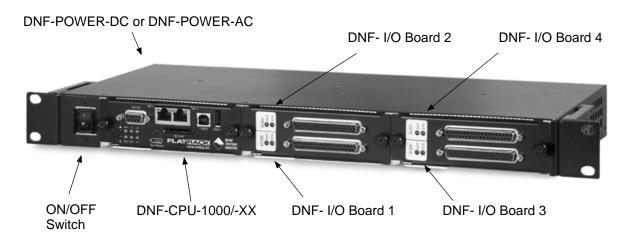


Figure 2-5. Typical DNF-4-1G Board Placement

Table 2-2 Components in DNF-4-1G Enclosure

Item / Part No.	Description
DNF-POWER-DC or DNF-POWER-AC	Mounting plate and connecting hardware for use with DNF-4-1G-DC or Mounting plate, connecting hardware, and 9-36 VDC power supply for use with DNF-4-1G-AC (see Table 2-1 and Figure 2-4)
DNF-CPU-1000, DNF-CPU-1000-02, DNF-CPU-1000-03	One dual-slot CPU/NIC module with status indicators, two Ethernet connectors (Main and Diagnostic Ports), sync connector, reset pushbutton, SD card slot, USB controller/slave ports (reserved), and a DB-9 connector for a serial port. (Refer to Section 2.6 for detailed information)
PowerDNF I/O Boards	Up to 4 front pull-out I/O boards (DNF boards are functionally identical to PowerDNA Cube I/O boards but designed for installation in a DNF rack enclosure). (Refer to Section 2.7 for more information)
DNF-4-ENCL	One backplane/assembly with temperature sensors (see Figure 2-4 for diagram)
DNF-IO-FILLER	Blank filler panels for all unused slots (Note that this item is optional / not included in price of rack)
Fans	Three cooling fans mounted to the left of the enclosure (see Figure 2-4)

All UEI modules and accessories are available in both PowerDNA and PowerDNR/F package designs.

2.4.3 DNF-4-1G Cooling Air Flow

Cooling air is drawn into the left side of the enclosure via three fans, routed over the power supply and electronic components, and then out the right of the enclosure. The system is designed to maintain positive pressure cooling within the enclosure at all times. Filters on the fan inlets are designed to significantly reduce dust.

Sensors mounted on the backplane continuously monitor internal temperatures, turning fans on if the internal temperature exceeds 45°C, off if it falls below 45°C, and shutting down power if a high limit is exceeded.

2.5 DNF-4-1G NIC/CPU and I/O Boards LEDs & Controls

DNF-4-1G LED indicators are illustrated in **Figure 2-6** and **Figure 2-7** respectively.

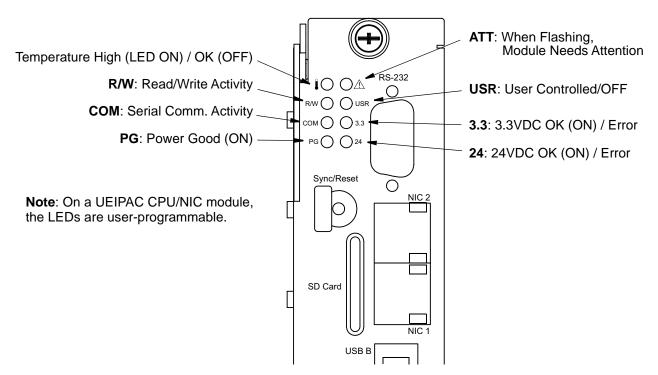


Figure 2-6. DNF-CPU-1000/-XX Module LEDs

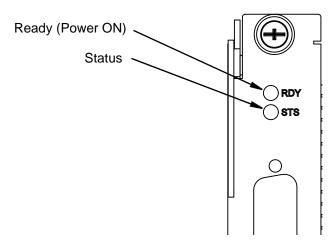


Figure 2-7. Typical I/O Module LEDs

2.6 DNF-CPU/NIC Module

The DNF-CPU/NIC Core Module (DNF-CPU-1000, DNF-CPU-1000-02, or DNF-CPU-1000-03) occupies the two left-most slots of a DNF-4-1G FLATRACK™ enclosure.

The DNF-CPU/NIC Core module consists of a Freescale MPC8347 or MPC8347E 32-bit 400 MHz CPU and peripheral devices (USB 2.0, RS-232, NIC, SD, etc) for use with a Gigabit Ethernet communication network and an internal 66 MHz 32-bit common logic interface bus. The NICs are copper (1000BaseT) interfaces.

The module has an RS-232 port used for configuration and also two USB 2.0 ports (controller and slave) for general purpose use (not implemented yet). LEDs on the front panel of each module indicate the current operating status of the device.

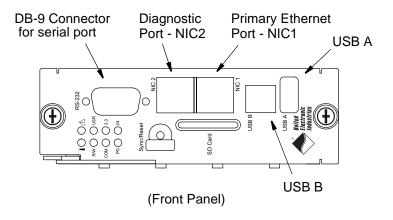


Figure 2-8. DNF-4-1G Series Core Module (CPU/NIC)

2.6.1 Device Architecture of DNF Core Module

Figure 2-9 shows the architecture of the DNF-CPU-1000 Series Core Modules:

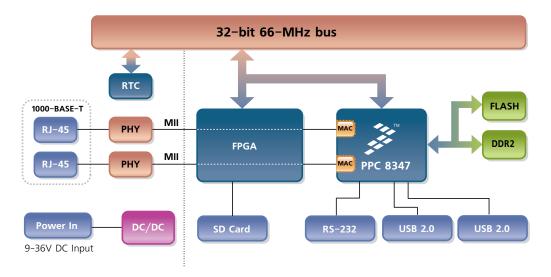


Figure 2-9. FreeScale PowerPC CPU/NIC Controller Architecture

The core of the system is a Freescale PowerPC MPC8347 or MPC8347E 32-bit 400 MHz processor, which controls the following components:

Table 2-3 Components in DNF-4-1G Core Module (DNF-CPU-1000 Series)

Item	Description
NIC1: Primary Network Interface MII Port	The NIC1 port provides communication between the DNF-4-1G system and the primary LAN network.
NIC2: Diagnostic Network Interface MII Port	The NIC2 port provides access to the DNF-4-1G system for monitoring system health during operation, using a separate diagnostic port. This port may also be assigned as the primary Ethernet port if NIC1 is not available for use.
RS-232 Port	The RS-232 port provides a serial communication link between the DNF-4-1G system and a standard RS-232 terminal.
USB 2.0 Dual Port (Controller and Slave)	The USB A and B ports are not supported on DNF-4-1G PowerDNA (hosted) systems (only supported on UEIPAC, UEISIM, UEIModbus, and UEIOPC-UA deployments).
32 MB or 128 MB Flash Memory ¹	DNF-4-1G systems provide 32 MB of flash memory (DNF-CPU-1000). DNF-4-1G-02 systems provide 32 MB of flash memory (DNF-CPU-1000-02). DNF-4-1G-03 systems provide 128 MB of flash memory (DNF-CPU-1000-03).
128 MB or 256 MB of SDRAM ¹	DNF-4-1G systems provide 128 MB of RAM (DNF-CPU-1000). DNF-4-1G-02 systems provide 256 MB of RAM (DNF-CPU-1000-02). DNF-4-1G-03 systems provide 256 MB of RAM (DNF-CPU-1000-03).

Table 2-3 Components in DNF-4-1G Core Module (DNF-CPU-1000 Series)

Item	Description
SYNC Port	A high-speed system-to-system synchronization connector permits triggers and/or clocks to be shared among multiple systems. Two systems may be connected together directly and larger groups may use the SYNC interface to share timing signals among many racks and systems.
	The trigger and clock inputs will accept signals from standard digital logic that is powered in the range of 3.3V to 5V. The inputs also have internal pull-up resistors to an internal 5V supply, making the inputs also compatible with a low-side drive open-collector output. The Sync and trigger outputs have 5V logic levels. The sync connector's ground and 5V power connections are provided by its own isolated DC-DC converter.
IEEE-1588 Synchronization Support	DNF-4-1G-02 and DNF-4-1G-03 systems implement IEEE-1588 synchronization in hardware. (DNF-CPU-1000-02 and DNF-CPU-1000-03)
SD Card ¹	A slot for inserting a Secure Digital card. SD cards are not supported on DNF-4-1G hosted systems. (SD cards are only supported on UEIPAC, UEISIM, UEIModbus, and UEIOPC-UA deployments, uses EXT3 as filesystem for the system partition and optionally FAT32 for one or more data partitions on the UEIPAC-based standalone systems only).
Solid state hard drive ¹	Optional solid state hard drive (only supported on UEIPAC, UEISIM, UEIModbus, and UEIOPC-UA deployments).
LEDs	The operating conditions indicated by the front panel LEDs are described in Figure 2-6 on page 11 and Figure 2-7 on page 12.
Watchdog Timer With Real-time Clock (Battery Backed)	The DNF-4-1G system includes a watchdog timer with battery backed-up real-time clock.

1. RAM, flash, solid state drives, and SD cards are not user-accessible on PowerDNA (hosted) systems (only for use with UEIPAC, UEISIM, UEIModbus, and/or UEIOPC-UA deployments).

Not all components are available for control from the CPU. The CPU can program flash memory, set the LEDs, set up the watchdog timer, set the real-time clock and use 256 bytes of backed-up memory in the watchdog timer chip. All functions are available at the firmware level only (described in iom.c/iom.h).

2.7 DNF I/O Boards

All standard cube-based PowerDNA I/O boards are also available as rack-based PowerDNF boards. A typical PowerDNF board is functionally identical to its corresponding PowerDNA version. The only difference between them is the physical mounting arrangement. PowerDNF modules are designed for insertion into the DNF-4-1G enclosure; DNA- modules can be inserted only into a PowerDNA Cube.

NOTE: When specifying I/O boards in your application, the device number is a zero-based reference. For example, the first I/O board will be referenced as DEVN 0. Refer to Figure 2-5 on page 10 for I/O board locations.

Refer to the datasheets and user manuals for detailed electrical specifications, board descriptions, and user instructions for I/O boards. These documents are available on the UEI website at www.ueidaq.com.

Chapter 3 Installation and Configuration

The following installation and configuration topics are included in this chapter:

- Initial Installation Guide (Section 3.1)
- Initial Boot-up (Section 3.2)
- IP Address Overview & Update Procedures (Section 3.3)
- Improving Network Performance (Section 3.4)
- Troubleshooting (Section 3.5)
- Updating Firmware (Section 3.6)
- Mounting and Field Connections (Section 3.7)
- Wiring (Section 3.8)
- Peripheral Terminal Panel Wiring (Section 3.9)
- Repairing (and Upgrading) a DNF System (Section 3.10)
- Configuring a NIC Port for Diagnostic Mode (Section 3.11)
- Disabling Writes to Flash/EEPROM (NVRAM) (Section 3.12)

3.1 Initial Installation Guide

This section describes the procedure recommended for performing an initial hardware and software setup when you first receive a DNF-4-1G system:

- DNF-4-1G hardware setup
- DNF- software package installation
- Configuration

3.1.1 Inspect Package

Inspect the contents of the shipping package. With a standard DNF-4-1G system, you should find:

- A DNF-4-1G enclosure, preinstalled with a NIC/CPU module (DNF-CPU-1000/-XX), DNF-POWER-DC or -AC (mounting hardware, connectors and, for -AC versions, a DC power supply), blank filler panels (if specified), plus your selection of I/O boards.
- Mounting brackets (DNF-BRACKET).
- A power cord (PWR-CBL).
- A DB-9 serial cable for initial hardware configuration and firmware downloading (DNA-DB9MF-CBL).
- A Cat5e Ethernet cable, 7 foot (DNA-CAT5E-CBL).
- CD-ROM with support software.

3.1.2 Install Software

This section describes how to load the PowerDNA software suite onto a Windows- or Linux-based computer (i.e. host PC) and run some initial tests.

The latest support software is online at www.ueidaq.com/download; a copy is also on the PowerDNA Software Suite CD.

A. Software Install: Windows

The PowerDNA CD provides one installer that combines the UEI low-level driver and UEIDAQ Framework.

The installer automatically searches for third-party IDE and testing suites, and adds them as tools to the suites found. Be sure to install third-party applications (such as LabVIEW, MATLAB, or Visual Studio) *before* installing the PowerDNA Software Suite.

To install the PowerDNA Software Suite, do the following:

STEP 1: Run Setup as an Administrator

a. Insert the PowerDNA Software Suite CD into your CD-ROM drive. Windows should automatically start the PowerDNA Setup program. An installer with the UEI logo and then PowerDNA Welcome screen should appear. If none appears, run setup.exe from the CD drive:

Start >> Run >> d:\setup.exe >> OK.

If you downloaded the most recent executable from www.ueidaq.com, double-click on the filename to run the executable.

b. Choose the PowerDNA Software Suite option.

- c. Unless you are an expert user and have specific requirements, select *Typical Installation* and accept the default configuration. The Software Suite installer automatically installs any required tools and plugins. If 32-bit Java VM is not detected on the system, Java JRE 1.6.5 for Windows XP will automatically be installed for PowerDNA Explorer. As an alternative, use the *Custom* option to display and ensure that all of the necessary packages are installed.
 - Companion Documentation:

Quick Start Guide, Configuration and Core Module, I/O Board Manuals, API Programming Guide

- SDK: includes/lib for C/Java, examples, and JRE; (The SDK is not the UeiDag Framework).
- PowerDNA Apps: PowerDNA Explorer, MTTTY
- PowerDNA Components (incl. DLL files)
- PowerDNA Firmware
- d. Click **Next** to continue through the dialogs.
- e. Click **Finish** to complete the installation.

This Software Suite will install tools needed in later steps, such as MTTTY, PowerDNA Explorer, and the low-level driver.

UEIDAQ Framework provides the structure for developing applications under C/C++, C#, VB.NET, ActiveX, MATLAB, LabVIEW, LabWindows/CVI, OPC, and other programming languages.

STEP 2: Restart the computer.

NOTE: Because the installation process modifies your Windows registry, you should always install or uninstall the software using the appropriate utilities. Never remove PowerDNA software from your PC directly by deleting individual files; always use the Windows Control Panel Add/Remove Programs utility.

B. Software Install: Linux

The PowerDNA_*.tgz file in the CD\Linux folder contains the software package for Linux. To extract the file to a local directory:

```
tar -xjvf <Path to file>/PowerDNA*.tgz
```

Follow the instructions in the readme.txt file provided in the tar file.

- **3.2 Initial Boot-up** Perform an initial boot in preparation for configuring the network using the following procedure:
 - **STEP 1:** Familiarize yourself with your DNF-4-1G system front-panel layout. Refer to Figure 2-5 on page 10 for board placement.
 - **STEP 2:** Optionally, set up communication over the serial port by attaching the serial cable between the host PC and to the RS-232 port on the front panel of the DNF-4-1G:
 - Run a serial terminal-emulation program (e.g., MTTTY) on the PC. Any terminal-emulation program, except HyperTerminal, may be used (MTTTY, Minicom, TeraTerm, PuTTY, etc.).
 - b. Verify that COM parameters are set at: 57600 baud, 8 bits, no parity, 1 stop bit.
 - Click Connect in MTTTY, or use the commands on one of the other terminal-emulation programs to establish communication with the DNF-4-1G system.
 - **STEP 3:** Connect power to the system (9-36 VDC for DNF-4-1G-DC or 100-240 VAC / 50-60 Hz for DNF-4-1G-AC) by plugging the power connector from your power supply into the mating connector at the rear of the DNF-4-1G chassis.
 - **STEP 4:** Turn on the ON/OFF power switch at the front of the DNF-4-1G chassis.

NOTE: As soon as the system powers up, it runs through a self-diagnostic mode and, if you have serial communications set up, generates output on the terminal program. A typical readout is shown below.

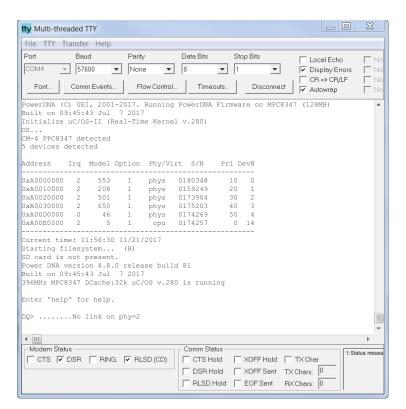


Figure 3-1. Typical MTTTY Screen after DNF-4-1G Boot-up

The boot process displays the model, serial number, and slot positions of boards in the rack enclosure.

You can also type show <Return> at the DQ> serial prompt to display additional information about the system configuration:

```
DQ> show
        name: "IOM-174257"
       model: 3004
      serial: 0174257
        fwct: 1.2.0.0
         mac: 00:0C:94:02:A8:B1
         srv: 192.168.100.2
          ip: 192.168.100.2 (1Gbit)
     gateway: 192.168.100.1
     netmask: 255.255.255.0
        mac2: 00:0C:94:F2:A8:B1
        srv2: 192.168.100.102
         ip2: 192.168.100.102 (DOWN)
    gateway2: 192.168.100.1
    netmask2: 255.255.255.0
         udp: 6334
     license: ""
    Manufactured 4/6/2017
    Calibrated 4/6/2017
```

All parameters can be changed, including the IP address, gateway, and subnet mask (netmask) system configuration.

The next section provides instructions for changing the IP address. You can also refer to Chapter 6 for more information about changing the IP address and other parameters via the serial port.

DQ>

3.3 IP Address Overview & Update Procedures

The DNF-4-1G ships with preconfigured factory default IP addresses for NIC1 and NIC2 in nonvolatile memory (usually 192.168.100.2 for NIC1 and 192.168.100.102 for NIC2). These are static IP addresses; a hosted DNF-4-1G system never retrieves its IP address from a DHCP server.

This section describes when and how to change the default IP addresses.

3.3.1 When Should You Change the IP Address?

You should change your IP address if you have multiple UEI chassis in your application or if your application has network addressing guidelines you must conform to.

Before connecting your DNF-4-1G to a general-purpose (company domain) network, consider the following:

- High sampling rate measurements consume a lot of the available bandwidth.
- Some samples may be significantly delayed or entirely dropped (lost) due to network congestion, collisions or a slow switch.
- Whether a system will be accessed by multiple parties on a LAN.
- Whether multiple Cubes/RACKs/systems will operate (and interact) on the same network.

Alternatively, if you plan to use the system for high-speed measurements where high reliability is necessary – a direct connection between the host PC and the DNF-4-1G NIC¹ is recommended.

Refer to "Improving Network Performance" on page 23 for more information.

^{1.} NIC - Network Interface Controller; a commercially available Ethernet (i.e. IEEE 802.3-2005) adapter.



3.3.2 How to Change the Primary IP Address (NIC1)

Instructions for changing the IP address are provided in this section. You can use PowerDNA Explorer (a UEI-developed GUI application) or a serial terminal program to change the IP address.

The first step in changing the IP address is to consult your system or network administrator to obtain unused IP addresses.

You can change the IP address from the default using the procedure in Section 3.3.2.1 (via PowerDNA Explorer) or Section 3.3.2.2 (via the serial port).

3.3.2.1 Update IP Address via PowerDNA Explorer

PowerDNA Explorer provides an interface for updating your IP address over the Ethernet connection.

To use PowerDNA Explorer, you must first establish communication between your host PC and chassis. Refer to "Getting Started with PowerDNA Explorer" on page 49 for additional information about how to open, set up and use PowerDNA Explorer, if needed.

To update your IP address, do the following in the PowerDNA Explorer window:

- **STEP 1:** Click **Scan Network** to explore your system (refer to **Figure 3-2** for button location).
- **STEP 2:** Click the DNF-4-1G system that you want to update, (e.g., IOM-12345. DNF-4-1G systems are listed in the left panel).
- STEP 3: Enter the new IP address in the IP 1 field.
- STEP 4: Press <Return> on your keyboard.
- **STEP 5:** Click **Store Configuration** to save your change and reset the DNF-4-1G.

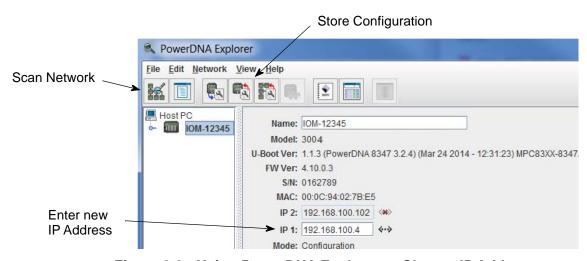


Figure 3-2. Using PowerDNA Explorer to Change IP Address

Storing the configuration downloads the new IP address into the system's non-volatile memory.

If needed, the gateway and network mask can be changed via the serial port. Refer to Section 5.4 on page 72 for instructions.

3.3.2.2 Update IP Address via Serial Port

To update the IP address on your DNF-4-1G over the serial port, you must first establish serial communication between your host PC and chassis.

To set up communication over the serial port, do the following:

- a. Attach a serial cable between the host PC and the RS-232 port on the front panel of the DNF-4-1G.
- b. Run a serial terminal-emulation program (e.g., MTTTY) on the PC. Any terminal-emulation program, except HyperTerminal, may be used (MTTTY, Minicom, TeraTerm, PuTTY, etc.).
- c. Verify that COM parameters are set at 57600 baud, 8 bits, no parity, 1 stop bit.
- d. Click **Connect** in MTTTY, or use the commands on one of the other terminal-emulation programs to establish communication with the DNF-4-1G system.

To update the IP address on your DNF-4-1G, enter the following commands in the serial terminal window:

```
DQ> set ip 192.168.200.65
Enter user password > powerdna

DQ> store
DQ> reset

DQ> reset

// Sets the system IP to 192.168.200.65
// The default password is "powerdna"

// Saves the newly changed configuration
// Reboots the system for the new IP to
// take effect
```

To verify, you can type show to display the new IP address.

NOTE: Refer to Section 5.4 for more descriptions of commands you can issue via a serial connection, including descriptions of the set and store commands.

Once your IP address is configured, you can connect the DNF-4-1G NIC to your switch with a CAT5e cable and communicate with it via a network connection.

3.3.3 How to Change the Secondary (Diagnostic) IP Address (NIC2)

To change the IP address of the secondary port (NIC2), you use a serial terminal program as with the primary port, but instead use the command:

```
set ip2 aaa.bbb.ccc.ddd
```

where aaa.bbb.ccc.ddd is the new IP address for the secondary port.

Then proceed the same as with the primary port. NIC2 IP addresses cannot be changed using PowerDNA Explorer.

3.4 Improving Network Performance

To improve DNF-4-1G network performance, we recommend that instead of connecting to a company-wide network, you use separate commercially available network interface controller (NIC) cards and, where possible, set up a single dedicated mini-network for DNF-4-1G racks for both operation and diagnostics, as shown in **Figure 3-4** on the next page.

As an alternative, you can configure two separate networks, one for operation and one for diagnostic purposes, as shown in **Figure 3-5**.

If you do not need to connect to a company LAN and have only a single DNF-4-1G in your system, you can connect it directly to your host as shown in **Figure 3-3** below.

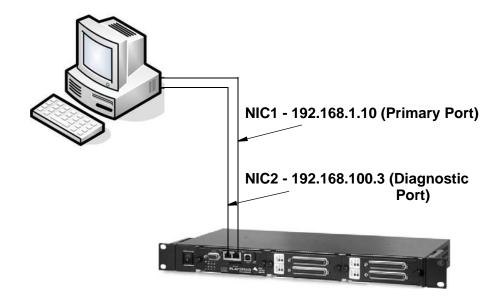


Figure 3-3. Single DNF-4-1G Direct-Connected to Host without LAN Switch

Figure 3-4 shows a two-rack single network system with a LAN switch that performs both data acquisition and diagnostic functions.

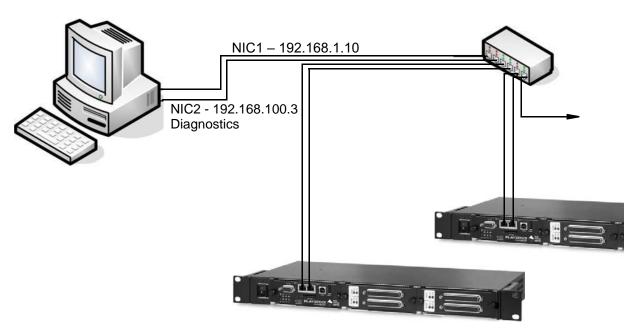


Figure 3-4. Single Network for Operation and Diagnostics Using DNF Racks and LAN Switch

Figure 3-5 shows a two-rack dual network system with two LAN switches that performs both data acquisition and diagnostic functions.

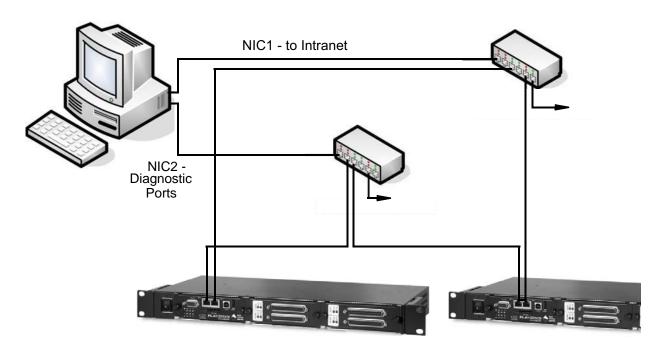


Figure 3-5. Separate Networks for Operation and Diagnostics: Two Racks & Two Switches

3.4.1 Example of Configuring Network Settings

As an example, assume that your office uses a Class C network (the class intended for small networks with fewer than 256 devices), and your host PC is configured with a static IP or via DHCP (Dynamic Host Configuration Protocol).

STEP 1: Obtain your networking configuration of your host PC:

• On Windows systems, open the command prompt and type ipconfig to display the configuration:

Start >> Programs >> (Accessories >>) Command Prompt

```
C:\> ipconfig
```

Ethernet adapter Local Area Connection:

Connection-specific DNS Suffix .:
IPv4 Address. : 192.168.1.10

• On Linux systems, use "ifconfig" instead.

In the above example, the subnet mask of 255.255.255.0 on NIC1 uses the subnet range 192.168.1.0 through 192.168.1.255. Refer to the IP Addressing Side Note on the next page for more information about subnets.



IP Addressing Side Note:

The range of usable addresses is defined by the IP address and subnet mask.

- An IP address is a number that lies within the range of 0.0.0.0 and 255.255.255.255. In the ipconfig example shown in step 1, the IP address is 192.168.1.10.
- The subnet mask indicates where an address range starts and stops. For example, a subnet mask 255.255.255.240 has 15 usable addresses (255.255.255.255 255.255.255.240). In the ipconfig example shown in step 1, the subnet is 255.255.255.0, or 255 addresses.

The subnet limits from anything.anything.0 up to the max.

- The usable range for 192.168.1.10/255.255.255.0 is 192.168.1.1 to 192.168.1.254 (192.168.1.0 and 192.168.1.255 are reserved for Router and Broadcast messages).
- The usable range for 192.168.100.2/255.255.255.0 is 192.168.100.1 to 192.168.100.254

Not every IP address from 0.0.0.0 to 255.255.255.255 is usable; however, these three ranges of IP addresses are guaranteed open for private use:

- 10.0.0.0 10.255.255.255
- 172.16.0.0 172.31.255.255
- 192.168.0.0 192.168.255.255

STEP 2: Install a secondary NIC card, if needed.

STEP 3: Set up a secondary network that does not overlap the existing one:

In our example, the address space 192.168.1.0-192.168.1.255 is used by NIC1. The IP address block 192.168.100.1 to 192.168.100.255 is available and is in the private range.

Let us choose 192.168.100.1-192.168.100.255 for the PC's secondary NIC and setup the port as follows:

IPv4 Address: 192.168.100.3 Subnet mask: 255.255.255.0 Default Gateway:192.168.100.3

a. On your host PC, open the Network and Internet settings in the control panel:

Start >> Programs >> Control Panel >>Network and Internet >> View network status and tasks

- b. Click *Change adapter settings* in the left-sidebar, and then right-click the adapter to bring up the Properties window.
- c. Open the TCP/IPv4 properties of the adapter and edit to the network settings noted above.

NOTE: Refer to the Appendix A for step-by-step instructions and screenshots on how to set up TCP/IPv4 properties.

d. Open the Command Prompt:

Start >> Programs >> (Accessories >>) Command Prompt

e. Type ipconfig at the Command Prompt to confirm the network configuration on the host PC:

C:\> ipconfig

<unused adapter settings are not shown in this example>

STEP 4: Use a serial terminal application (e.g. MTTTY) on the host to configure the DNF-4-1G system to use the same subnet as the host PC:

```
Rack NIC2 IP: 192.168.100.2
Rack NIC2 Gateway:192.168.100.3
Rack NIC2 Netmask: 255.255.255.0
```

- a. Attach a serial cable between the host PC and the RS-232 port on the front panel of the DNF-4-1G.
- b. Run a serial terminal-emulation program (e.g., MTTTY) on the PC. Any terminal-emulation program, except HyperTerminal, may be used (MTTTY, Minicom, TeraTerm, PuTTY, etc.).
- c. Verify that COM parameters are set at 57600 baud, 8 bits, no parity, 1 stop bit.
- d. Click Connect in MTTTY, or use the commands on one of the other terminal-emulation programs to establish communication with the DNF-4-1G system.
- e. Enter the following commands when you see the DQ command prompt:

```
DQ> set ip2 192.168.100.2

DQ> set gateway2 192.168.100.3

DQ> set netmask2 255.255.255.0

DQ> store

DO> reset
```

NOTE: The DNF-4-1G rack in this example is changed to 192.168.100.2 in step 4 above (in the same subnet as your host PC's NIC2 at 192.168.100.3 which was set up in step 3).

Note that this example assumes NIC1 is already set on your DNF-4-1G system.

- **STEP 5:** Connect the DNF-4-1G to your PC's second NIC using a CAT5 cable. The green LEDs on the DNF-4-1G NIC2 should light up.
- **STEP 6:** Ping the DNF-4-1G system from the command prompt on the host PC to make sure that it is alive (the following shows a successful response):

```
C:\> ping -n 1 192.168.100.2
Pinging 192.168.100.2 with 32 bytes of data:

Reply from 192.168.100.2: bytes=32 time<1ms TTL=128
Ping statistics for 192.168.100.2:
Packets: Sent = 1, Received = 1, Lost = 0 (0% loss),</pre>
```

NOTE: A "Request Timed Out" message indicates an error.

STEP 7: The system should now be configured as shown in Figure 3-6.

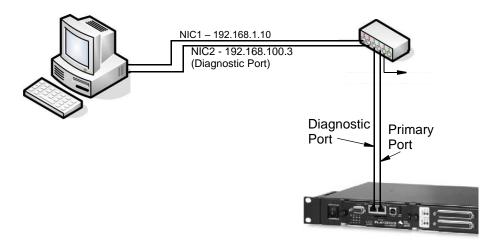


Figure 3-6. Typical Configuration for a Single DNF-4-1G with a LAN Switch

STEP 8: You may now use PowerDNA Explorer to access the system via the network. (Refer to **Chapter 4** for more information about PowerDNA Explorer, if needed.)

3.5 Trouble-shooting

The following sections provide suggestions when troubling shooting your system.

3.5.1 Troubleshooting System Communication

Use following checklist as a starting point when troubleshooting a system.

- ✓ Verify the PG (Power Good) LED is ON:
 This indicates power is applied to the chassis. (Refer to Figure 2-6 on page 11 for LED locations)
- ✓ Verify the green LEDs on NIC ports are blinking: This indicates the CAT5e cables are connected.
- Check communication over the Ethernet connection:
 Use the command prompt to ping <system IP>.

 (For example: ping 192.168.100.2)
 If ping doesn't respond, check the following
 - Disable the firewall (temporarily) on the NIC.
 - Check the NIC's network settings.
 - Check the system's network settings.
- Check communication over the serial connection:

 Connect a serial cable between your host PC and your DNF-4-1G chassis, open a serial communication program (e.g., MTTTY), and click Connect:
 - Press [Enter] in the serial terminal window to display the DQ> prompt. (No prompt indicates that you are not connected).
 - If you cannot connect over the serial port, check the following:
 - Verify the settings: 57600 baud, no parity, 8 data bits, 1 stop bit.
 - Check the device manager on your PC to see which com port you are using. Enter that com port in your serial communications program, (e.g., COM1, COM2, COM3), click Connect and press [Enter].
 - If you are able to connect over the serial port, check the following:
 - Type "show" the serial terminal window to verify the IP, Subnet Mask, and Gateway.
 - Note "show" results, and verify computers are on a valid subnet and have valid IPs.
- Reboot the DNF-4-1G system. The start-up screen should display upon restart.
- ☑ If all else fails, contact UEI support at support@ueidaq.com.

3.5.2 Troubleshooting Communication after Reset

After your FLATRACK IOM is set up and you reset the chassis, you may notice a situation where you can't see your FLATRACK (or IOM) from a host computer immediately after reset. After up to two minutes, the connection shows up again.

This is caused by the operating system Address Resolution Protocol (ARP) implementation. When you try to contact an offline host that was previously online, the OS invalidates the Ethernet <-> IP address resolution protocol table until a timeout expires and it can be re-queried.

3.5.2.1 How to Find ARP Timeout Setting

To find how long the refresh timeout is on Windows machines, do the following:

- **STEP 1:** Open a command window on your host computer.
- **STEP 2:** Type netsh interface ipv4 show interfaces at the command prompt to find the index number of the interface connected to your IOM, (e.g., 11 for the Local Area Connection):



Figure 3-7. Show Interfaces

STEP 3: Type netsh interface ipv4 show interface <Idx #> to learn the timeout and other interface parameters of a connection:

```
C:\Users\netsh interface ipu4 show interface 11

Interface Local Area Connection Parameters

IfLuid : ethernet_6
IfIndex : 11
State : connected
Metric : 19
Link MTU : 1500 bytes
Reachable Time : 24000 ms
Base Reachable Time : 30000 ms
Retransmission Interval : 1000 ms
DAD Transmits : 3
Site Prefix Length : 64
Site Id : 1
```

Figure 3-8. Show Interface Parameters

NOTE: In the above example, the timeout, or Base Reachable Time, is set to 30000 ms.

3.5.2.2 How to Speed Up ARP Timeout

To avoid waiting for the timeout, you can either force an immediate rebuild of the ARP cache or change the delay for subsequent timeout situations. Both of the following must be entered as an Administrator.

- To immediately reset, type the following at the command prompt: arp -d *
- To modify the Base Reachable Time, type the following to set the timeout to 5000 ms on interface 11:

netsh interface ipv4 set interface 11 basereachable=5000

3.6 Updating Firmware

This section provides the following information about updating the firmware for DNF-4-1G FLATRACK (i.e., RACK) systems:

- Determining Currently Installed Firmware Version (Section 3.6.1)
- Updating Firmware via PowerDNA Explorer (Section 3.6.2)
- Updating Firmware via Serial Interface (Section 3.6.3)

The CPU/NIC module in a DNF-4-1G stores the system firmware.

Updated firmware is periodically released to introduce new features and to improve the performance of existing features. Updated firmware releases are bundled with the full PowerDNA Software Suite, available for download at any time from the UEI web site (www.ueidaq.com).

To locate the latest UEI firmware after installing the PowerDNA Software Suite, browse to the installation's Firmware directory, (e.g. *C:\Program Files (x86)\UEI\PowerDNA\Firmware*).

The directory contains the following:

- an MTTTY executable (serial terminal application)
- two sub-directories containing the firmware

Locate the firmware in the GigE system directory: this is the **Firmware_PPC_1G** subdirectory and the rom image file with extension MOT.

3.6.1 Determining Currently Installed Firmware Version

Before updating the firmware of a system, check the version to determine which update method to use.

PowerDNA Explorer, a GUI-based troubleshooting application provided with the installation, can be used to check the firmware version. Refer to **Chapter 4** if you need additional information about setting up and using PowerDNA Explorer.

To check the firmware version, do the following:

- STEP 1: Connect power to the DNF-4-1G system (RACK):
- **STEP 2:** Connect an Ethernet cable between the NIC 1 port on the RACK and the host PC or network (e.g., host PC Ethernet port, switch).
- STEP 3: Start PowerDNA Explorer:
 - From the Windows desktop menu, navigate to
 Start >> Programs >> UEI >> PowerDNA >> PowerDNA Explorer
 - On Linux systems, access PowerDNA Explorer under the UEI installation directory (<PowerDNA-x.y.z>/explorer) by typing java -jar PowerDNAExplorer.jar
- **STEP 4:** In the PowerDNA Explorer window, click *Network >> Scan Network*.
- **STEP 5:** Select the RACK icon you wish to query (by clicking the icon). Note the version that is given in the **FW Ver** field (Figure 3-9).

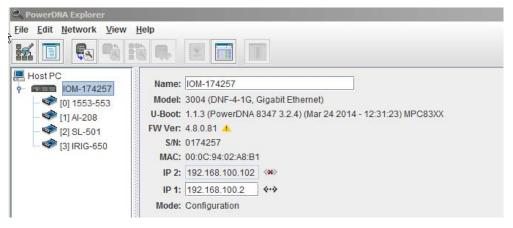


Figure 3-9. Displaying the Version of Your Firmware

If the **FW Ver** has a yellow triangle with an exclamation point next to it (see figure above), you have a mismatch between the firmware installed on your RACK system and the software version on your host PC. If you see this warning, UEI highly recommends that you update your firmware to match your software (or software to match your firmware). Firmware version mismatches can result in unexpected operation.

If the **FW Ver** shows a version of 2.x.x.x, 3.x.x.x, or 4.x.x.x, follow the firmware update instructions on the following pages.

For other versions of firmware, (i.e. 1.x.x.x), refer to the user manual on the CD that accompanied your device when you purchased it.

3.6.2 Updating Firmware via PowerDNA Explorer

Before using a new release of UEI libraries and applications to communicate with your system, you should install the latest version of the firmware onto the CPU core module in your RACK. Mismatched versions can cause operational errors.

Instructions for updating the CPU core via PowerDNA Explorer (over Ethernet LAN line) are described below, and instructions for updating the CPU core via a serial interface (using MTTTY) are provided in the following subsection.



CAUTION!

If you update the firmware on the RACK CPU board, be sure to use the PDNA Explorer from the same release version as the new firmware.

To upload firmware with PowerDNA Explorer over LAN, do the following:

- **STEP 1:** Connect power to the DNF-4-1G RACK:
 - Plug the power cable into the DNF-4-1G power connector at the rear of the chassis.
- **STEP 2:** Connect an Ethernet cable between the NIC 1 port on the DNF-4-1G RACK and the host PC or network (e.g., host PC Ethernet port, switch).
- STEP 3: Start PowerDNA Explorer:
 - From the Windows desktop menu, navigate to Start >> Programs >> UEI >> PowerDNA >> PowerDNA Explorer
 - On Linux systems, access PowerDNA Explorer under the UEI installation directory (<PowerDNA-x.y.z>/explorer) by typing java -jar PowerDNAExplorer.jar
- **STEP 4:** From the PowerDNA Explorer window, click *Network* >> *Scan Network*.
- STEP 5: Select the icon of the DNF-4-1G RACK system to be updated.
- **STEP 6:** Click *Network* >>*Update Firmware...*from the menu.



Figure 3-10. Update Firmware Menu Item

- **STEP 7:** Click "Yes" when you see the prompt:
 - "Are you sure you want to update firmware..."
- **STEP 8:** Verify you are in the Firmware_PPC_1G directory, and double-click the rom8347_X.X.X.mot (where X.X.X. is the version) file.

STEP 9: If asked, enter the password to continue. UEI cube and RACK systems come with the default password set to powerdna.



Figure 3-11. Password Dialog Box

STEP 10: Wait for the progress dialog to complete. The system will then be updated and running the new firmware.

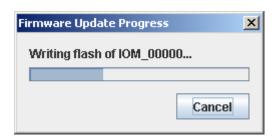


Figure 3-12. Firmware Update Progress Dialog Box

Each system is updated in three steps. First, the firmware is transferred to the system. Second, the firmware is written to the flash memory. During this step, the R/W light on the front of the chassis is lit, in addition to the PG light. Third, the system is reset. During this step, the ATT, COM, and PG lights are lit, and the R/W light will turn on and off periodically. When the system is finished resetting, only the PG light is lit.

3.6.3 Updating Firmware via Serial Interface

The following section provides the procedure for uploading firmware over the DNF-4-1G serial port using a serial terminal client. In this procedure, we use MTTTY as the serial terminal client; however, any serial terminal application can be used to upload the ROM image.

- **STEP 1:** Connect power to the DNF-4-1G FLATRACK.
- **STEP 2:** Attach the serial cable to the host PC and to the RS-232 port on the front panel of the RACK serial port.
 - a. Run a serial terminal-emulation program (e.g., MTTTY) on the PC.
 - b. Verify that COM parameters are set at: 57600 baud, 8 bits, no parity, 1 stop bit.
 - Click Connect in MTTTY, or use the commands on one of the other terminal-emulation programs to establish communication with the DNF-4-1G RACK system.
- **STEP 3:** Use the hardware Reset switch on the front of the RACK chassis to reset the CPU Module, or type reset at the DQ> prompt in the serial window.
- **STEP 4:** While the system is starting up again, press <Enter> on your keyboard to go into **u_boot**. The DQ> prompt in the serial terminal window will change to the => prompt when in **u_boot**.
- **STEP 5:** Type the commands shown below to erase firmware storage area in the Flash memory and load the new firmware (refer to Figure 3-13):
 - => erase FF800000 FF9FFFFF
 - => loads

NOTE: The loads command stores firmware into flash memory while downloading it.

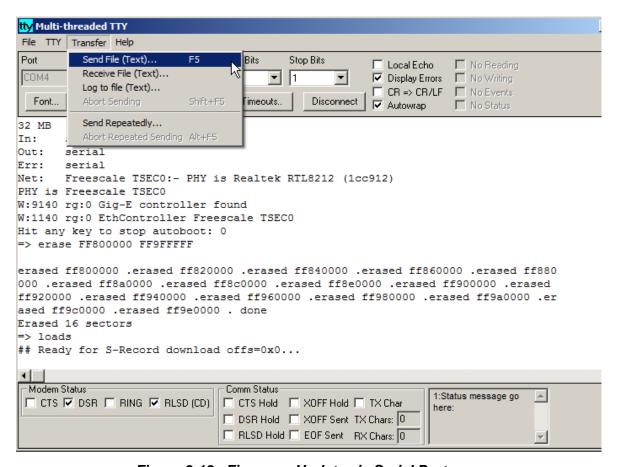


Figure 3-13. Firmware Update via Serial Port

- **STEP 6:** Do the following to transfer the Motorola firmware image file (refer to Figure 3-13):
 - a. In the MTTTY menu bar, select *Transfer » Send File*.
 - b. Navigate to your UEI installation, and select the image file:

\Program Files (x86)\UEI\PowerDNA\Firmware\Firmware_PPC_1G\rom8347_4_x_y.mot

NOTE: A progress bar will appear in the lower left corner of MTTTY, indicating progress.

- STEP 7: Wait for the upload to complete (it may take a few minutes).
- **STEP 8:** After the process finishes, type go FF800100 in the MTTTY terminal window. The CPU module will then be updated and running the new firmware.

3.7 Mounting and Field Connections

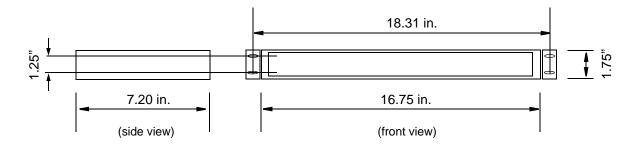
The DNF-4-1G can be mounted in a standard 19-inch rack using the included rack mount brackets or on a horizontal surface using the base mount brackets.

 For mounting in a standard 19-inch rack, attach flanges to both ends of the enclosure with the flanges aligned flush with the front of the enclosure. Then attach the flanges to the rack with bolts.

If you need technical drawings, please contact UEI support.

3.7.1 Physical Dimensions

The DNF-4-1G enclosure used in a DNF-4-1G system is compatible with Specification EIA-310-C for 19" Rack Mounting Equipment and is designed to occupy 1U unit of vertical space (where 1U is 1.75"). The physical dimensions of the DNF-4-1G enclosure are shown below in **Figure 3-14**.



Note: For horizontal mounting, align flanges flush with base of enclosure. For rack mounting, align flanges with front of enclosure.

Figure 3-14. Physical Dimensions of DNF-4-1G Enclosure

3.7.2 Pinouts

Pinout diagrams for the synchronization and RS-232 serial port connectors are shown below in **Figure 3-15**.

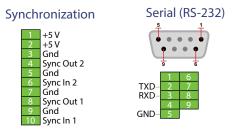


Figure 3-15 DNF-4-1G Pinout Diagrams

3.8 Wiring

1000Base-T Wiring Configurations

A typical wiring configuration for a 1000Base-T network is shown in the following figure.

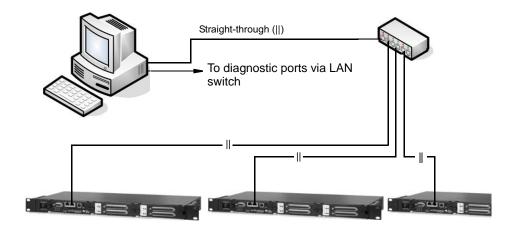


Figure 3-16. System Configuration with LAN Switch

Refer to "Improving Network Performance" on page 23 for more configuration options.

3.9 Peripheral Terminal Panel Wiring

Refer to the applicable I/O board manuals for proper wiring to boards.

3.10 Repairing (and Upgrading) a DNF System

DNF-4-1G systems come from the factory fully configured and calibrated. Individual modules are designed for field replacement and are not suited for field repairs.

If you encounter a problem with a DNF system, you can quickly remove and replace individual boards or other system modules in the field. You can also rearrange the locations of boards within the enclosure at any time; however, note that you may need to reprogram I/O board locations in your application.

If you want to enhance, repair, or otherwise modify a specific I/O board, however, you must send the module back to the factory or to your local distributor.

This process requires that you request an RMA number from UEI before shipping. To do so, contact support@ueidaq.com and provide the following information:

- 1. Model Number of the unit, (e.g. DNF-AI-217)
- 2. Serial Number of the unit
- 3. Reason for return, (e.g. faulty channel, needs calibration, etc.)

UEI will process the request and issue an RMA number.

3.11 Configuring a NIC Port for Diagnostic Mode

The CPU Core Module has two Ethernet ports, NIC1 and NIC2. Either port can be assigned as the Main Operation Port or as a Diagnostics Port.

The main and diagnostics ports are interchangeable. The user application can open both ports independently and use separate handles to access each of them. A port becomes a diagnostics port, which prevents changes in the state of the ongoing operation, after it is configured and locked-in as a diagnostics port. This allows great flexibility in IOM wiring — if either port or its cabling fails, you can use the other port as the main port.

If all I/O boards are in configuration mode and the lock is not set, the diagnostics port functions as an equivalent of the main port. Any command that can be executed on the main port can be executed on the diagnostics port as well.

Refer to the PowerDNA API Reference Manual for API used with this section.

The following standard DAQBIOS commands are accessible on the diagnostics port whenever one or more I/O boards are in operating mode:

Commands that are capable of changing the state of the running I/O boards will not execute.

// Switch to diagnostics

To switch a port into diagnostics mode, use the DqCmdSetLock API, as described below:

int DAQLIB DqCmdSetLock(int Iom, uint8 Mode, char Password, uint32 *IP) Parameters: int Iom // Pointer to the DQIOME structure uint8 Mode // Function mode (lock/unlock/check/diagnostics) char *Password // password string; ignored (and can be NULL) if Mode is DQSETLOCK_CHECK uint32 *IP // returns the IP address of the locking host // if Mode is DQSETLOCK_CHECK <Mode> can be one of the following: #define DQSETLOCK LOCK // Lock IOM to host Ω #define DQSETLOCK UNLOCK 1 // Unlock IOM // Get locking host IP

#define DQSETLOCK_CHECK 2

#define DQSETLOCK DIAG

To advance a port into diagnostics mode, call this function with the <Mode> parameter set to DQSETLOCK_DIAG. To return a port to normal mode, use the same function call with DQSETLOCK_UNLOCK.

The following table describes the possible states of both ports:

Table 3-1 Port States

Port	LOCK State	First Port (NIC1)	Second Port (NIC2)
First	DQSETLOCK_UNLOCK	Full functionality	Full functionality
	DQSETLOCK_LOCK	Full functionality, locked to the host	All but state change functions
	DQSETLOCK_DIAG	Diagnostic functionality only	Full functionality
Second	DQSETLOCK_UNLOCK	Full functionality	Full functionality
	DQSETLOCK_LOCK	All but state change functions	Full functionality, locked to the host
	DQSETLOCK_DIAG	Full functionality	Diagnostics functionality only

DQCMD ECHO

This command returns information about the board(s) installed. Use of this command is described in the PowerDNA API Reference Manual.

DQCMD RDCFG

This command returns the current configuration of the specified board(s):

int DAQLIB DqCmdReadCfg(int Iom, DQRDCFG pDQRdCfg[], uint32 maxsize, uint32* entries)

```
int Iom
                    // a pointer to the DQIOME structure
DQRDCFG pDQRdCfg[]
                    // structure that contains board configuration
uint32 maxsize
                    // number of DORDCFG structures passed
uint32* entries
                    // number of DQRDCFG structures returned
```



```
typedef struct (
   uint8 DEV;
                    // device (host fills this field)
   uint8 ss;
                    // subsystem (host)
   uint32 status;
                    // device status (device returns following fields)
                    // configuration, including clocks
   uine32 cfg;
   uint32 rate;
                    // clock divider in 15.5ns intervals
                    // size of the channel list
   uint32 clsize;
   uint32 cl[];
                    // channel list - variable size
) DQRDCFG, *pDQRDCFG;
```

Note: Use device! = 0x80 to indicate that this is the last device in the list.

DQCMD RDSTS

This command returns the status of the IOM and each and every board in the stack (upon request):

```
int DAQLIB DqCmdReadStatus (int Iom, uint8 *DeviceNum, uint32 *Entries,
uint32 *Status, uint32 *StatusSize)
```

Parameters:

There are special device numbers to access status of various boards:

OxFE – returns IOM status and status of all boards (note that each board status is expressed as four 32-bit words. Thus, the maximum size of status packets is (4 + 14*4)*sizeof(uint32) = 240 bytes.

```
0x7F - returns IOM status only (four bytes)
```

```
0x0 . . 0xE – returns status of one of the boards
```

The status for each board consists of four 32-bit words, as follows:

```
/* status offsets into devob].status array */
#define STS_STATE(0) // state of the board
#define STS_POST(1) // post status
#define STS_FW(2) // firmware status
#define STS_LOGIC(3) // logic status
```

The first word is the state of the board – what mode of operation it is in, and the lower 8-bits of the timestamp. If the 10 us timestamp does not change after each call, the logic is in the inoperative state, as:



The second word describes the status of the board. It is written when the board enters initialization mode and remains unchanged until the next reboot. STS_POST_SDCARD_FAILED, STS_POST_DC24 and STS_POST_DCCORE can be changed during operation if the corresponding failure occurs.

```
/* POST status flags */
                                            // Memory test failed
#define STS_POST_MEM_FAIL
                                 (1L << 0)
#define STS POST EEPROM FAIL
                                 (1L << 1)
                                            // EEPROM read failed
                                            // board failure
#define STS_POST_LAYER_FAILED
                                 (1L << 2)
#define STS_POST_FLASH_FAILED
                                 (1L << 3)
                                            // Flash checksum error
#define STS_POST_SDCARD_FAILED
                                            // SD card is not present
                                 (1L << 4)
#define STS_POST_DC24
                                 (1L < < 5)
                                            // DC->24 board failed
#define STS_POST_DCCORE
                                 (1L<<6)
                                            // Core voltage problem
#define STS_POST_BUSTEST_FAILED (1L<<7)</pre>
                                            // Bus test failed (hwtest.c)
#define STS_POST_BUSFAIL_DATA
                                 (1L < < 8)
                                            // Bus test failed on data tst
#define STS_POST_BUSFAIL_ADDR
                                 (1L<<9)
                                            // Bus test failed on addr tst
#define STS_POST_OVERHEAT
                                (1L << 10)
                                            // Overheat detected
#define STS POST STICKY
                                (STS POST MEM FAIL STS POST BUSTEST FAILED
                                 STS_POST_BUSFAIL_DATA | STS_POST_BUSFAIL_ADDR)
```

The third word contains the logic status flags. They are read and assembled from the various registers of the common board interface (CLI) upon request. Not all boards implement full functionality and boards operating normally should not show any flags set.

```
/*logic status flags */
#define STS LOGIC DC OOR
                                   (1UL<<0)
                                              // DC/DC out of range (IOM
                                              //also)
#define STS LOGIC DC FAILED
                                   (1UL<<1)
                                              // DC/DC failed (IOM also)
#define STS_LOGIC_TRIG_START
                                              // Trigger event started
                                   (1UL<<2)
                                              // (IOM also)
#define STS LOGIC TRIG STOP
                                              // Trigger event stopped
                                   (1UL<<3)
                                              // (IOM also)
#define STS LOGIC CL0 NOT RUNNING (1UL<<4)</pre>
                                              // Output channel list not
                                              // running
#define STS_LOGIC_CLI_NOT_RUNNING (1UL<<5)</pre>
                                              // Input channel list not
                                              // running
#define STS LOGIC CVCLK CLO ERR
                                   (1UL<<6)
                                              // CV clock error for CL0
#define STS_LOGIC_CVCLK_CLI_ERR
                                   (1UL<<7)
                                              // CV clock error for CLI
#define STS LOGIC CLCLK CLO ERR
                                   (1UL<<8)
                                              // CL clock error for CLO
#define STS_LOGIC_CVCLK_CLI_ERR
                                   (1UL<<9)
                                              // CL clock error for CLI
#define STS LOGIC NO REPORTING
                                   (1UL<<31)
                                             // Installed logic does not
                                              // support error reporting
#define STS_LOGIC_STICKY
                                   (STS_LOGIC_NO_REPORTING)
```

The fourth word contains the status of the firmware. A board operating normally does not have any flags set except STS_FW_CONFIG_DONE, which means the board was properly configured before entering operating mode (it is cleared upon re-entering configuration mode) and STS_FW_OPER_MODE, which means that the board switched into operating mode without any errors.

```
/* fw status flags */
#define STS_FW_CLK_OOR
                              (1UL<<0)
                                         // Clock out of range (IOM
                                         // also)
#define STS_FW_SYNC_ERR
                              (1UL<<1)
                                         // Synchronization interface
                                         // error (IOM also)
#define STS_FW_CHNL_ERR
                              (1UL<<2)
                                         // Channel list is incorrect
#define STS_FW_BUF_SCANS_PER_INT
                              (1UL<<3)
                                         // Buf setting error:
                                         //
                                                scans/packet
#define STS_FW_BUF_SAMPS_PER_PKT
                              (1UL<<4)
                                         // Buf setting error:
                                                samples/packet
                                         //
#define STS FW BUF RING SZ
                              (1UL<<5)
                                         // Buf setting error: FW
                                         // buffer ring size
#define STS_FW_BUF_PREBUF_SZ (1UL<<6)</pre>
                                         // Buf setting error: Pre-
                                         // buffering size
#define STS_FW_BAD_CONFIG
                              (1UL<<7)
                                         // Board cannot operate in
                                         // current config
#define STS_FW_BUF_OVER
                                         // Firmware buffer overrun
                              (1UL<<8)
#define STS_FW_BUF_UNDER
                              (1UL<<9)
                                         // Firmware buffer underrun
#define STS_FW_LYR_FIFO_OVER (1UL<<10)</pre>
                                         // Board FIFO overrun
#define STS_FW_LYR_FIFO_UNDER(1UL<<11)</pre>
                                         // Board FIFO underrun
                                         // Board EEPROM failed
#define STS_FW_EEPROM_FAIL
                              (1UL<<12)
#define STS FW GENERAL FAIL
                              (1UL<<13)
                                         // Board general failure
#define STS_FW_ISO_TIMEOUT
                              (1UL<<14)
                                         // Isolated part reply timeout
#define STS_FW_FIR_GAIN_ERR
                              (1UL<<15)
                                         // Sum of fir coeffs is not correct
#define STS_FW_OUT_FAIL
                              (1UL<<16)
                                         // Output CB tripped or over-
                                         // current
                                         // Messaging I/O failed (5xx
#define STS_FW_IO_FAIL
                              (1UL<<17)
                                         // boards)
#define STS_FW_NO_MEMORY
                              (1UL<<18
                                         //Error with memory allocation
#define STS_FW_BAD_OPER
                                         // Operation was not performed
                              (1UL<<19)
                                         // properly
#define STS_FW_LAYER_ERR
                              (1UL<<20)
                                         // Board entered operation
                                         // successfully
#define STS_FW_CONFIG_DONE
                              (1UL<<30)
                                         //Configuration is completed
                                         // (no error)
#define STS_FW_OPER_MODE
                              (1UL<<31)
                                                  // Board entered operation
                                         // mode successfully
/* status helper macros/defines */
#define STS_FW_STICKY (STS_FW_EEPROM_FAIL|STS_FW_GENERAL_FAIL)
```

Status bits are divided into "conditional" and "sticky". Conditional bits are set when a condition arises; they are cleared when the error condition expires. Sticky bits are persistent once set and are cleared by reading their status.

DQCMD_IOCTL

This command is used to retrieve data from the board. When a port is in diagnostic mode, it returns current data but cannot reprogram the channel list. The channel list is used to inform the handler the ID of the channel from which data should be retrieved.

The following table lists functions that rely on the DQCMD_IOCTL command for transport for several board types:

Table 3-2 Example Functions and Associated Boards

Function	Associated Board Type(s)
DqAdv201Read	AI-201 and AI-202
DqAdv205Read	AI-205
DqAdv207Read	AI-207
DqAdv225Read	AI-225
DqAdv3xxWrite	AI-302/308 and AI-332
DqAdv40xRead	DIO-401/405/404/406
DqAdv403Read	DIO-403
DqAdv416GetAll	DIO-416 Voltage, current, and circuit
	breaker state monitoring
DqAdv432GetAll	DIO-432 Voltage, current, and circuit
	breaker state monitoring
DqAdv448Read	DIO-448
DqAdv448ReadAdc	DIO-448 Voltage monitoring
DqAdv501GetStatistics	SL-501and SL-508 Received/error counters
DqAdv566GetStatistics	ARINC-429-566 Received/error counters
DqAdv601Read	CT-601 Counters, states of input lines
DqAdv604Read	QUAD-604 Positions, states of input lines

Sequence of Operation

To use the diagnostic port without affecting performance of the main port, UEI recommends that you use the following sequence of operations:

- 1. Open main port.
- 2. Open diagnostics port.
- 3. Perform hardware reset (optional) and re-open ports, if needed.
- 4. Lock diagnostic port into DQSETLOCK_DIAG.
- When operation is configured on the main port, read the status of the diagnostics port to verify that the configuration was programmed correctly.
- 6. Once operation on the main port is started, the diagnostics port becomes available for data retrieval.
- 7. Read status of the diagnostics port to make sure that all boards of interest successfully entered operating mode without error.
- 8. In the cycle:
 - a. Retrieve the current status once a second.
 - b. Check the flags for error conditions.
 - c. Retrieve additional data if any flags are set.
- 9. Stop operation and unlock diagnostics port.
- 10. Resume normal operation with main port.

3.12 Disabling Writes to Flash/ EEPROM (NVRAM)

DNF-4-1G systems include a hardware feature that provides the option of disabling writes to non-volatile memory (NVRAM).

By installing the NVRAM protection jumper, all writes to flash and EEPROM will be disabled on the hardware level.

NOTE: Writes to the EEPROM on the DNx-AO-358 and DNx-AO-364 are not disabled by this process.

Applications that must disable all NVRAM writes should not include the DNx-AO-358 and DNx-AO-364 products in their system.

Note that installing the NVRAM protection jumper requires the DNF-CPU-1000/DNF-CPU-1000-XX module in the DNF-4-1G chassis to have a PCB board removed and replaced. In general UEI does not recommend that users remove PCB boards from their carriers: over-torquing screws or bending PCB boards can permanently damage the DNF-CPU-1000 modules. UEI can install and remove jumpers as needed, if you have any concerns.

3.12.1 Disabling NVRAM Writes

To disable writes to non-volatile memory, do the following:

- **STEP 1:** Turn OFF power to the DNF-4-1G system using the toggle switch at the front of the system.
- STEP 2: Identify the DNF-CPU-1000 module in your DNF-4-1G chassis, and using a torque screwdriver, loosen the thumbscrews securing the module to the chassis.
 Lift the insertion/extraction lever and remove the CPU/NIC board (DNF-CPU-1000/-XX) from the enclosure. (Refer to figure below).

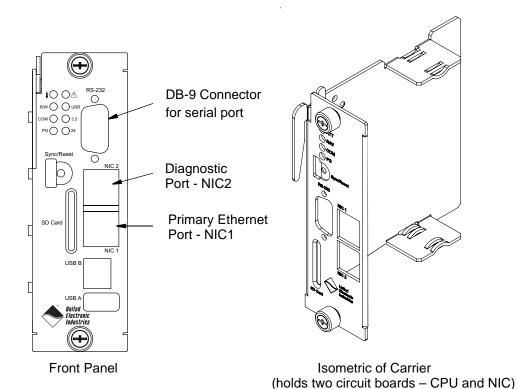


Figure 3-17. DNF-4-1G NIC/CPU Core Module and Carrier



CAUTION! Care must be taken when removing PCB boards from carrier. Over-tightening or forcing hardware can crack boards, damage components and/or leave the DNF- NIC/CPU module inoperable.

- **STEP 3:** To remove the lower PCB board from the carrier, do the following:
 - a. Loosen 1 Phillips screw (4-40 x 1 inch) from the bottom of the carrier using 1/4" locknut driver and Phillips screwdriver. Remove screw, 3 plastic spacers, and locknut. Retain hardware.
 - b. Gently slide lower PCB board from carrier.
- **STEP 4:** Locate J4 jumper block on board removed in the previous step. Refer to **Figure 3-18** for location.

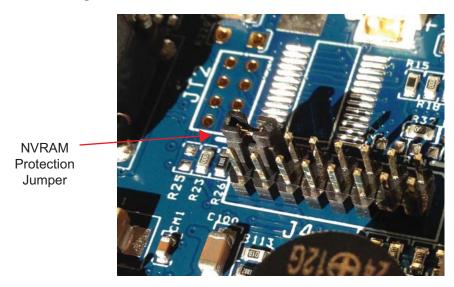


Figure 3-18. NVRAM Protection Jumper

STEP 5: Insert jumper between pins 13 and 15 on J4 jumper block. Refer to Figure 3-18.



CAUTION! Care must be taken when replacing PCB boards into carrier. Over-tightening or forcing hardware can crack boards, damage components and/or leave the DNF- NIC/CPU module inoperable.

- **STEP 6:** To install the lower PCB board into the carrier, do the following:
 - a. Gently slide lower PCB board into carrier. Care must be taken when sliding the board in; electrolytic capacitors on board can get damaged if they scrape against top board.
 - Align PCB board LEDs, RESET button, and sync port with openings on carrier: Be sure the RESET button is free to move. (See Figure 3-17 for location)
 - Slide and align retained small plastic spacer between carrier and lower board.

- d. Slide and align retained large plastic spacer between lower and upper boards.
- e. From the bottom of the carrier, insert the retained Phillips screw (4-40 x 1 inch) through the carrier, small plastic spacer, lower PCB board, large plastic spacer, and upper PCB board.
- f. Check PCB board LEDs, RESET button, and sync port at the front of the carrier: RESET button should be free to move.
- Slide retained small plastic spacer on Phillips screw and install locknut.
- h. Gently tighten with 1/4" locknut driver and Phillips screwdriver, taking care not to over-tighten. Over-tightening can crack PCB boards.
- STEP 7: Insert the DNF-CPU-1000/-XX module into the enclosure, being careful to align the board with the top and bottom guides. Fully insert the module into the guides and use the insertion lever to seat the board into the backplane connector.
- STEP 8: Using the torque screwdriver set to 5 lb-in, screw in the thumbscrews until the torque screwdriver clicks.
- **STEP 9:** Power up the system by turning ON the power switch at the front of the chassis.

3.12.2 Re-enabling

To re-enable writes to non-volatile memory, repeat the procedure in NVRAM Writes Section 3.12.1 except remove the jumper in step 5 instead of installing it.

Chapter 4 PowerDNA Explorer

PowerDNA Explorer is a GUI-based application for communicating with your DNF-4-1G system. PowerDNA Explorer simplifies configuration and setup of your system, as well as allowing you to check your communication link and start exploring your FLATRACK and I/O boards.

This chapter provides the following information:

- Getting Started with PowerDNA Explorer (Section 4.1)
- Overview of the Main Window (Section 4.2)
- Exploring I/O Boards with PowerDNA Explorer (Section 4.3)

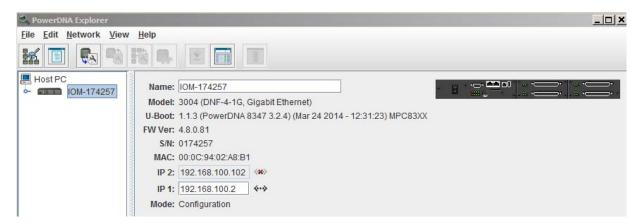


Figure 4-1. PowerDNA Explorer

NOTE: The screenshot in Figure 4-1 shows the PowerDNA Explorer screen for a DNF-4-1G system. Throughout this chapter, example screenshots may show RACKtangle or Cube representations.

Each corresponding FLATRACK screen is the same as the RACKtangle or Cube representation except for the image icon in the left sidebar, the model number and description in the IOM settings panel, and the chassis image in the corner of the IOM & I/O boards settings panels.

4.1 Getting Started with PowerDNA Explorer

PowerDNA Explorer can be used on Windows or Linux systems.

On Windows systems, access PowerDNA Explorer from the Start menu:

Start > All Programs > UEI > PowerDNA > PowerDNA Explorer

On Linux systems, access PowerDNA Explorer under the UEI installation directory (<PowerDNA-x.y.z>/explorer) by typing:

• java -jar PowerDNAExplorer.jar



UEI provides a PowerDNA Explorer DEMO with the installation that lets you safely explore the menus and I/O board screens without using actual hardware. DEMOs are located in the same directories as the PowerDNA Explorer executables.

4.1.1 Connecting PowerDNA Explorer to Your System

PowerDNA Explorer has the capability of identifying DNF-4-1G systems (or any UEI Cube or RACK system) on a selected network. Using PowerDNA Explorer, you scan the network, and discovered systems are listed in the left-hand panel of the display.

To scan the network for UEI systems, you must provide a set of addresses to scan. Do the following to setup the address range:

STEP 1: Select *Network* >> *Address Ranges* from the menu:

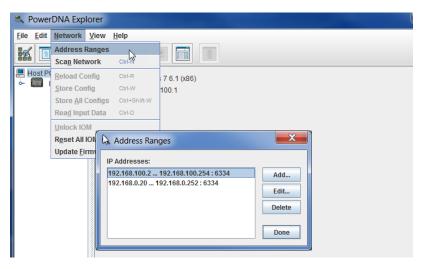
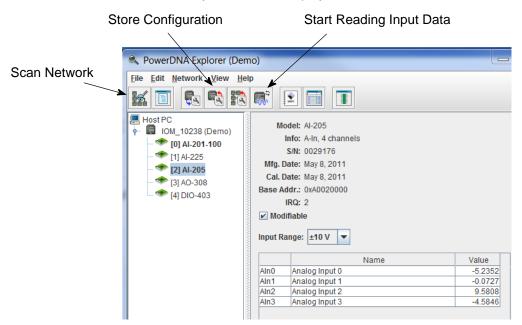


Figure 4-2. Address Ranges to be Scanned

- **STEP 2:** If the IP address of your DNF-4-1G system (e.g. 192.168.100.2) is not in the listed range, edit the range to include it, and then click **Done**.
- **STEP 3:** Click *Network* >> *Scan Network* to scan the LAN for DNF-4-1G or other UEI systems within the range specified in the previous step.

One or more gray icons will display in the left-hand-side of the screen. If no icons are displayed, refer to the Troubleshooting section in the previous chapter (Section 3.5).



STEP 4: Double-click a system icon to display its information and list the I/O boards:

Figure 4-3. Typical Screen for Analog Input Board

To display pertinent hardware and firmware information about a system once it is discovered, you simply click the specific system shown in the left-hand panel.

To display pertinent information about an I/O board in the system, you can click the I/O board of a specific system, which will be listed under the chassis icon and manipulate its inputs or outputs in the settings screen. PowerDNA Explorer lets you verify that the system is communicating with the host and that the I/O boards are functioning properly.

4.1.2 PowerDNA Explorer DEMO

The screenshot above is from the PowerDNA Explorer Demo. The "demo" is a simulator for users without hardware or for new users who want to explore the PowerDNA Explorer program without reading/writing to real hardware. Run this program and hover your mouse over the buttons to read the tool-tips and learn through interacting with the program.

Some quick notes:

- To read from a board, click the fourth-to-last button: "Start Reading Input Data"
- To write to the board, change a value and click the fourth button with the red arrow on top of the chassis: "Store Configuration". The icon with the blue arrow on it restores the configuration.
- To change the IP address, change the number, deselect the field, and "Store Configuration". Take care not to set the IP Address to outside of the network's configuration subnet -or- to an IP address that is currently in use, as the system will then become unreachable.
- ☑ To obtain a hardware report, click *View* >> *Show Hardware Report*.

Refer to Section 4.2 for more descriptions of the PowerDNA Explorer Window.

4.2 Overview of the Main Window

The Main Window of the PowerDNA Explorer is shown in **Figure 4-4** and consists of four primary sections:

- The Menu Bar (described in Section 4.2.1)
- The Toolbar (described in Section 4.2.2)
- The Device Tree (described in Section 4.2.3)
- The Settings Panel (described in Section 4.2.4).

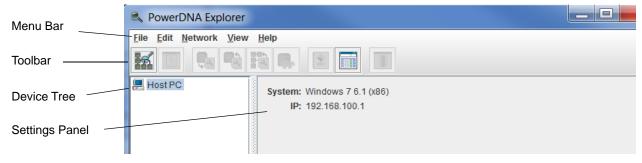


Figure 4-4. PowerDNA Explorer Main Window

When PowerDNA Explorer is first launched, the Main window has several buttons grayed out and shows only the Host PC in the Device Tree, as shown in **Figure 4-4**. To access systems in your network, you must first scan the network (refer to Section 4.1).

4.2.1 Menu Bar

The following subsections describe menus and menu items contained in the Menu Bar.

4.2.1.1 File Menu

This section describes items under the File Menu.

4.2.1.1.1 Setting Timeouts

The File >> Preferences selection opens the preferences dialog.

The preferences dialog allows you to specify timeout intervals.

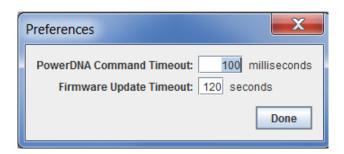


Figure 4-5. PowerDNA Explorer Timeout Preferences

PowerDNA Command Timeout sets the length of time PowerDNA Explorer will wait for response from a CPU/NIC Core Module before giving up with an error. It defaults to 100 milliseconds.

Firmware Update Timeout specifies the length of time PowerDNA Explorer will wait when updating firmware via *Network* >> *Update Firmware...* The firmware timeout defaults to 120 seconds. *File* >> *Exit* exits the application. If there are unsaved device settings changes, you are prompted for confirmation.

- **4.2.1.2 Network Menu** This section describes items under the Network Menu.
- 4.2.1.2.1 Specifying IP Address Ranges

Network >> *Address Ranges* opens the Address Ranges dialog, allowing you to specify where to scan for devices.

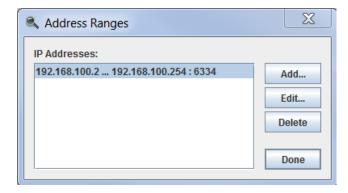


Figure 4-6. Address Ranges Dialog Box

The Address Ranges dialog allows you to specify the IP addresses and UDP port to use to find devices. The list in the above example defaults to a single range item that specifies the range 192.168.100.2 thru 192.168.100.254.

By clicking **Add** or **Edit**, you can specify individual addresses, as well as additional address ranges. After clicking **OK**, specified items appear in a list in which you can add or delete.

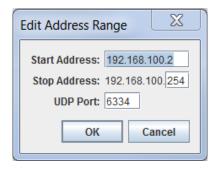


Figure 4-7. Edit Address Ranges Dialog Box

4.2.1.2.2 Scanning Network for UEI Chassis Network >> Scan Network scans the network for devices and populates the device tree. How much of the network is scanned depends on the settings in the Network Ranges dialog.



Figure 4-8. After a Network >> Scan Network

In the example shown above in Figure 4-8, after *Network* >> *Scan Network* was clicked, the UEI chassis labeled "IOM-12345" was found and displays in the Device Tree panel.

If you choose **Scan Network** when the device tree is already populated, any new devices discovered will be added to the tree. Any existing devices that are missing will be removed from the tree, unless you have made unsaved changes to the device's configuration, in which case it will be marked in the tree as missing.

4.2.1.2.3 Reloading Configuration

Network >> Reload Config re-reads the configuration of the current device selected in the Device Tree. If you have made changes to the settings in the settings panel for the current device, **Reload Config** will replace those settings with the current settings for the device, after prompting for confirmation.

4.2.1.2.4 Storing a Configuration

Network >> *Store Config* writes the changed settings for the currently selected device to the device. The button is disabled for devices that haven't been modified.

4.2.1.2.5 Storing All Configuration

Network >> *Store All Configs* writes all of the changed device settings to the devices. The button is disabled if no devices have been modified.

4.2.1.2.6 Reading Input Data from I/O Boards

Network >> *Start Reading Input Data* is enabled when the currently selected device is an input device board. It reads the current input values to the device and displays data read in the settings panel.

4.2.1.2.7 Updating the Firmware

Network >> Update Firmware... loads a firmware update file to all connected PowerDNA systems if Host PC is selected. It updates only one chassis when a specific unit is specified. More information about updating firmware can be found in "Updating Firmware" on page 31.

Note that writing certain configuration changes to a PowerDNA system will bring up a password dialog box. PowerDNA Cube and RACK systems come with the default password set to "powerdna".



Figure 4-9. Password Dialog Box for "Store Config" and "Store All Configs"



Figure 4-10. Password Dialog Box for "Update Firmware . . . "

4.2.1.3 View Menu

This section describes items under the View Menu.

4.2.1.3.1 Obtaining a Hardware Report *View >> Show Hardware Report* displays hardware information for your PowerDNA system..

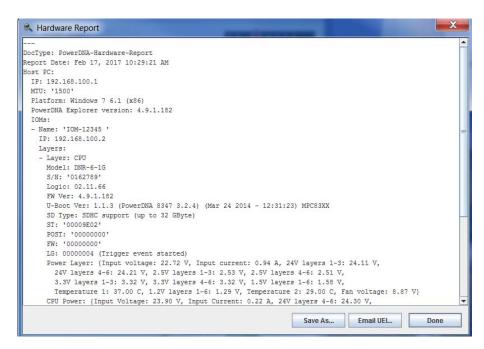


Figure 4-11. Example of a Hardware Report

4.2.1.3.2 Showing the Wiring Diagram for an I/O Board

View >> Show Wiring Diagram displays connector pins for a specific board. All boards have this feature. The AI-207 is displayed below as an example.

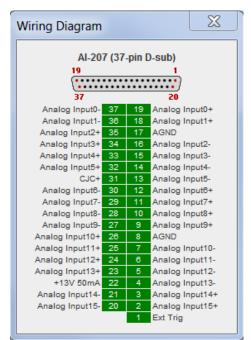


Figure 4-12. Example of a Wiring Diagram Display



4.2.1.4 Help Menu

This section describes items under the Help Menu.

Help >> About PowerDNA Explorer shows the **About** ... box, which shows the program icon, program name, version number, company name, and copyright notice.

4.2.2 Toolbar

The toolbar contains the following buttons:

- Scan Network, Show Hardware Report, Reload Config, Store Config, Store All Configs (shown in Figure 4-13)
- Start Reading Input Data, View User Manual, Visit Documentation Download Page, and View Wiring Diagram (shown in Figure 4-14)

Toolbar buttons duplicate the functionality of the corresponding menu items described in the Menu Bar sections above.

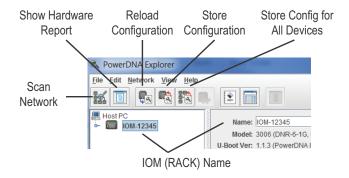


Figure 4-13. PowerDNA Explorer Toolbar Buttons (Config Level)

Start Reading Visit Documentation View User Input Data Manual Download Page (Live Data) <u>File Edit Network</u> View Wiring • Diagram Model: Al-207 IOM-12345 Info: A-In 16 differential [0] AI-207 S/N: 0151694 (1] AO-308 Mfg. Date: Feb 1, 2016 [2] DIO-403 Cal. Date: May 24, 2016

Figure 4-14. PowerDNA Explorer Toolbar Buttons (Board Level)

4.2.3 Device Tree

When the application is first launched, the tree contains a single root item representing the host computer (see **Figure 4-4**).

When you select **Scan Network** from the Network menu or the toolbar, the device tree is populated with all central controllers, IOMs (racks and cubes), and device boards accessible from the network, as filtered through the *Network* >> *Address Ranges* dialog.

Central controllers, if any, appear as children of the Host PC item. IOMs that are connected to the PC without use of a central controller also appear as direct children of the Host PC item.

Each item has an icon indicating whether it is a central controller, IOM (rack or Cube), or board. The text label for each item is the device's model number, name, and serial number.

Boards are also labeled with their position number in brackets.

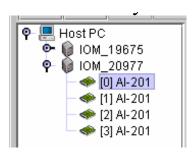


Figure 4-15. Example of the Device Tree

When an item is selected in the tree, the settings panel changes to reflect the settings for that device. The first time an item is selected, the device is queried as though you had invoked the **Start Reading Input Data** command.

On subsequent selections of the same item, the last settings are re-displayed. Thus, if you made changes but did not write them to the device, the changes are remembered. Invoking the **Start Reading Input Data** command will re-read the device and overwrite the current settings in the settings panel.

Devices whose settings have changed, but have not been written, are displayed in bold italics in the tree to provide a visual cue. Changed devices that become missing on a subsequent invocation of **Scan Network** turn red in the tree. (Unchanged items that become missing are simply removed from the tree.)

- **4.2.4 Settings Panel** The settings panel presents a set of controls that allows you to change the settings of the device currently selected in the device tree or allows you to view acquired input data for the device selected.
- **4.2.4.1 IOM Settings** The settings panel provides the following fields when an IOM is selected in the tree.

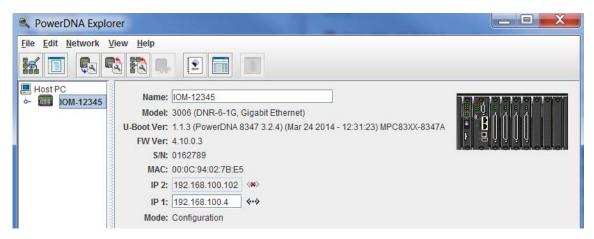


Figure 4-16. Example of IOM Settings Panel for HalfRACK DNR-6-1G

Field	Description
Name	shows the IOM name. Users can enter a custom name
Model	shows the model number of the IOM.
U-Boot Ver	shows the U-Boot version installed on the PowerDNA system
FW Ver	shows the version of the firmware installed on the PowerDNA system
S/N	shows the serial number of the IOM
MAC	shows the MAC address. It cannot be changed and is informational only
IP Address	shows the IP addresses of the IOM. IP 1 can be changed. See Section 3.3.3 for instructions on changing IP 2
Mode	shows the mode the IOM is in: <i>Initialization</i> , <i>Configuration</i> , <i>Operation</i> , or <i>Shutdown</i> .

Table 4-1 Fields and Descriptions for IOM Settings Panel

4.2.4.2 I/O Device / Board Settings

Figure 4-17 provides an overview of the screen for displaying I/O device settings. Setting options vary for I/O boards on a per-board basis. The example below show settings for the AI-217 analog input board.

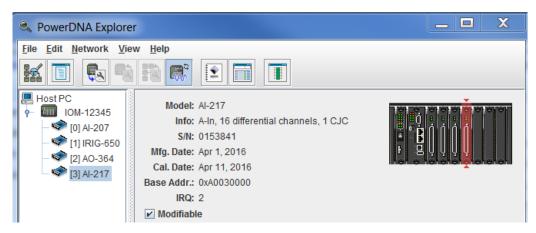


Figure 4-17. Example of I/O Device Settings

Field	Description
Model	shows the model number of the device
Info	shows summary of key features of the device: A for analog, D for digital, In for input, Out for output, and the number of channels available
S/N	shows the serial number of the device
Mfg. Date	shows the manufacturing date
Cal. Date	shows the date of the last calibration done
Base Address	shows the base address of the board in the IOM system
IRQ	shows which interrupt is assigned to the board
Modifiable	provides a checkbox which, when unchecked, prevents parameters from being changed

Table 4-2 Fields and Descriptions for I/O Device Settings Panel

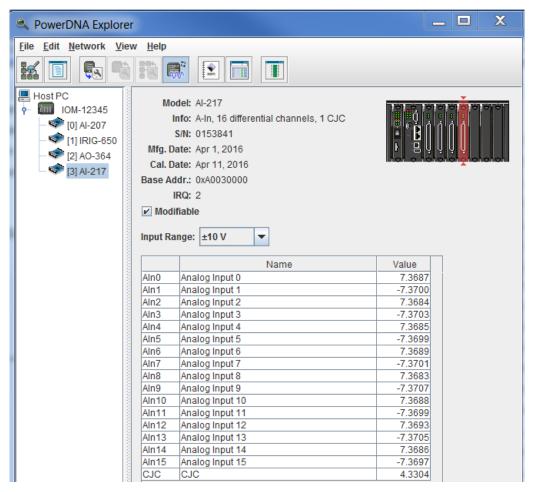


Figure 4-18. Screen from Network >> Start Reading Input Data

4.2.4.2.1 Interacting with I/O Boards

To read data from an I/O board, select *Network* >> *Start Reading Input Data*. The **Value** column for any inputs will update, as shown above in the settings panel.

Also in the settings panel, you can add or edit channel names. After editing names, choose *Network* >> *Store Config* to save changes to the board. This is true for all boards.

Additionally, if you have changed a configuration value, but have not chosen Network >> Store Config to save them, previous values can be re-read from the board, using Network >> Reload Config.

4.3 Exploring I/O Boards with PowerDNA Explorer

Settings available through PowerDNA Explorer will be dependent on the settings specific to each board types.

Examples of settings for several types of I/O boards are provided in subsections below:

- Digital Input/Output Board Settings (Section 4.3.1)
- Analog Output Board Settings (Section 4.3.2)
- Analog Input Board Settings (Section 4.3.3)
- Counter/Timer Board Settings (Section 4.3.4)

NOTE: Examples in this section are an introduction to PowerDNA Explorer capabilities; please note PowerDNA Explorer provides a communication link with all types of UEI I/O boards, not just the board-types listed in this section.

4.3.1 Digital Input/ Output Board Settings

This section provides an overview of PowerDNA Explorer settings for digital input/output boards. Each type of I/O board will have displays specific to the features offered with that board. In this section, we use the DIO-403 as an example.

NOTE: Use *Network* >> *Start Reading Input Data* to see immediate input values in Input tabs. Use *Network* >> *Store Config* to save values to the board.

The DIO-403 board is a 48-bit DIO board. It is different from other digital I/O boards because it groups 8-bits at a time into ports, and three ports into two "channels". This means that bit 0 in port 0 in channel 0 corresponds to DIO pin 0; bit 1 in port 1 in channel 0 corresponds to DIO pin 9; bit 2 in port 2 in channel 0 corresponds to DIO pin 18, etc.

For the sake of abstraction in PowerDNA Explorer, we'll call all ports channels.

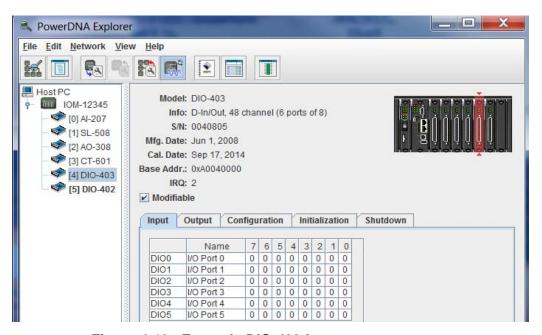


Figure 4-19. Example DIO-403 Inputs

Input/Output/Configuration/Initialization/Shutdown tabs switch between displaying DIO pin reading of input state data, setting DIO output state, configuring DIO as output or input, and settings for initial and shutdown states.

The Input tabs contain the following columns:

- Name is the channel (port) name, or a user-defined string.
- 7:0 Input Values consist of 0 or 1 as read from the input pin.

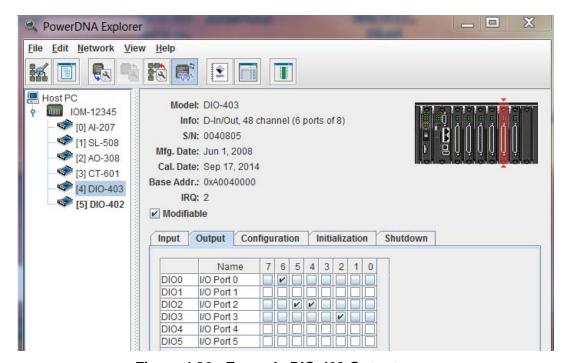


Figure 4-20. Example DIO-403 Outputs

Output tab sets the output value driven from the pin.

The Output tab contains the following columns:

- Name is the channel (port) name, or a user-defined string.
- 7:0 Output values consist of the output state to be driven from the I/O pin: select 0 (unchecked) or 1 (checked).

The settings in Figure 4-20 will cause output high values on DIO pin 6, pin 20, pin 21, and pin 26. The settings will cause output low values on DIO pins 0, 1, 2, 3, 4, 5, 7, 16, 17, 18, 19, 22, 23, 24, 25, 27, 28, 29, 30, 31.

The rest of the pins are configured as inputs; input vs output configuration is set under the Configuration tab.

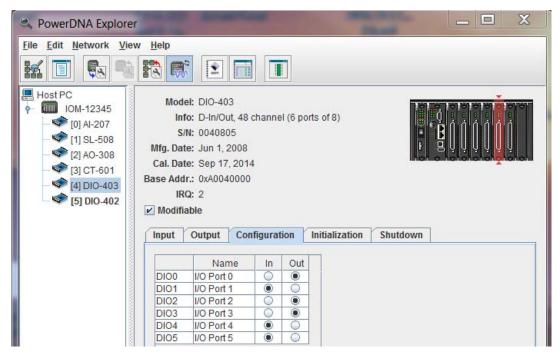


Figure 4-21. Example of DIO-403 Configuration

The **Configuration** tab gets/sets the current input/output directions per port. It contains the following columns:

- Name is the channel (port) name, or a user-defined string.
- In/Out contains toggle switches to select whether all the channels in that port are to be used as inputs or outputs.

Initialization/Shutdown tabs allow you to set initialization and shutdown states on pins, as well as operation mode configuration. They contain the following columns:

- Name is the channel (port) name, or a user-defined string.
- Mode specifies whether the channel is input or output.
- **7 through 0** contain the values 0 or 1. They are checkmarks for output channels that allow you to select 0 (unchecked) or 1 (checked).

Board Settings

4.3.2 Analog Output This section provides an overview of PowerDNA Explorer settings for analog output boards. Each type of analog output board will have displays specific to the features offered with that board. In this section, we use the AO-308 as an example.

NOTE: Use *Network* >> *Store Config* to save values to the board.

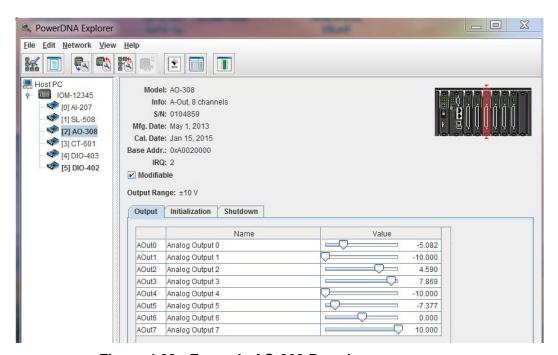


Figure 4-22. Example AO-308 Board

Controls for changing output, initialization, and shutdown values are available under each of the tabs in the settings panel. You can then choose Network >> Store Config to apply all changes to the board.

Output Range is displayed above the tabs. In this example, the output range cannot be changed and is informational only (the AO-308 output range is ±10 V). On other boards, **Output Range** is a popup allowing you to choose between board-supported ranges.

The Initialization and Shutdown tabs contain controls for setting initial and shutdown states:

- Name is the channel name or a user-defined string.
- Value contains a slider to set the voltage to output for the channel and the numerical voltage value, which you can input directly.

4.3.3 Analog Input Board Settings

This section provides an overview of PowerDNA Explorer settings for analog input boards. Each type of analog input board will have displays specific to the features offered with that board. In this section, we use the AI-207 as an example.

NOTE: Use *Network* >> *Start Reading Input Data* to see immediate input values. Use *Network* >> *Store Config* to save values to the board.

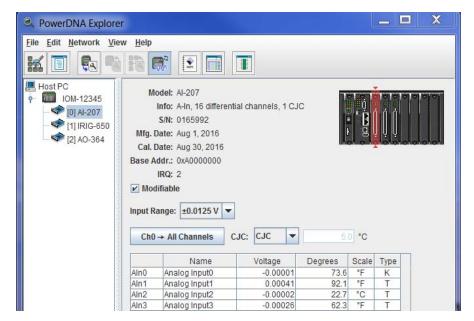


Figure 4-23. Example AI-207 Board

Input Range provides a pulldown menu of the range of expected input voltages to be measured by the board. On this board, the range can be specified as ± 10 V to ± 0.0125 V. Note if the actual voltage is outside of the range specified, the value displayed will clip at the maximum input range value.

The Data table contains the values currently read by the device. The table is initially blank until you refresh the data by clicking **Start Reading Input Data** (refer to Section 4.2.2).

The table for the AI-207 board in this example has the following columns:

- Name is the channel name or a user-defined string.
- Value shows the measured input value.
- Degrees shows the temperature converted from the measured input value.
- Scale provides a pulldown menu to select temperature scale (°C, °F, °K, °R) on a per channel basis.
- **Type** provides a pulldown menu to select thermocouple type (B, C, E, J, K, N, R, S, T) on a per channel basis.

4.3.4 **Board** Settings

Counter/Timer This section provides an overview of PowerDNA Explorer settings for counter/ timer boards. Each type of I/O board will have displays specific to the features offered with that board. In this section, we use the CT-601 as an example.

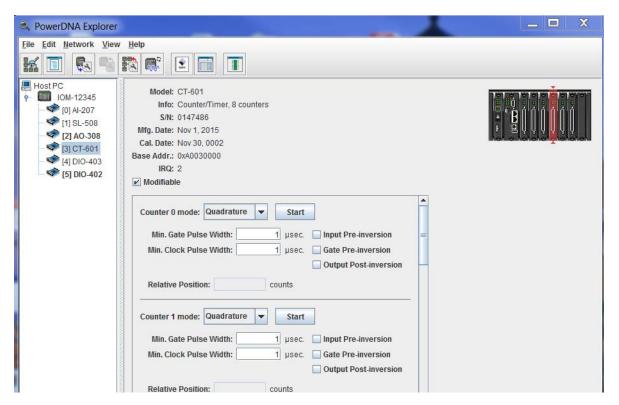


Figure 4-24. Example CT-601 Module

The CT-601 board has 8 counters. Each counter can be set to one of the different modes: Quadrature, Bin Counter, Pulse Width Modulation (PWM), Pulse Period, or Frequency.

When you change the mode of a counter using the mode pulldown menu, the controls for that counter will change to those appropriate for the mode.

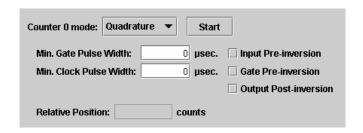


Figure 4-25. Example Quadrature Controls

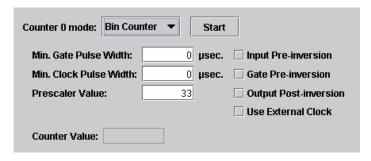


Figure 4-26. Example Bin Counter Controls

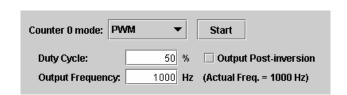


Figure 4-27. Example Pulse Width Modulation (PWM) Controls

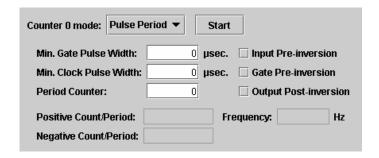


Figure 4-28. Example Pulse Period Controls

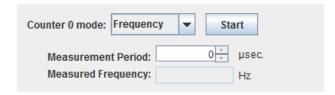


Figure 4-29. Example Frequency Controls

After setting the configuration for a counter, you can choose Network >> Store Config to store the settings on the device. Clicking the **Start** button will also write your configuration to the board.

Clicking the **Start** button for a counter will start that counter on the board. After clicked, the **Start** button will turn into a **Stop** button, and the other controls for that counter will become disabled until you click **Stop**.

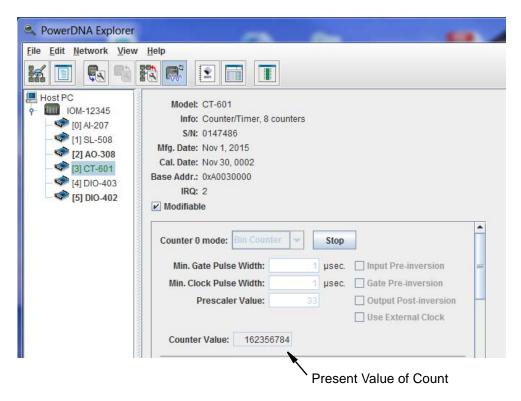


Figure 4-30. Example of Started Counter

While the board is running, you can choose *Network* >> *Store Config* to retrieve runtime values from the counter, which will display in the read-only text field(s) of the counter control panel.

Chapter 5 Programming CPU Board-specific Functions

5.1 Overview

This chapter provides information about programming DNF-4-1G CPU Core modules:

- Memory Map Overview (Section 5.2)
- Startup Sequence (Section 5.3)
- Setting and Reading CPU Core Parameters via Serial Port (Section 5.4)

NOTE: This chapter primarily provides descriptions of DNF-4-1G CPU Core commands that can be issued over a serial terminal.

Example code and additional documentation for programming your application, (e.g., getting started guides, API reference, synchronization documentation) are provided with the installation.

5.2 Memory Map Overview

The following section describes the memory map for the DNF-CPU/NIC core modules (DNF-CPU-1000/DNF-CPU-1000-XX).

NOTE: DNF-CPU/NIC board revisions align with product versions. For a list of for DNF-4-1G Series product versions, refer to Section 1.2 on page 3.

Table 5-1 Memory Map for DNF-4-1G CPU (DNF-CPU-1000)

	Start			
Device	Address	End Address	Size	Description
SDRAM	0x0	0x7FFFFFF	128MB	SDRAM_ADDRESS
Exception table	0x0	0x3000	12 kB	Processor address map
CPU card address	0xA00E0000	0xA00EFFFC	64 kB	EXT_SRAM_ADDRESS
Processor	0xE0000000			
RAMBAR				
Module – CS2	0xA0000000	0xA00FFFFC	1 MB	EXT_DEV_ADDRESS2
Module – CS3	0xA0100000	0xA01FFFFC	1 MB	EXT_DEV_ADDRESS3
Flash	0xFE000000	0xFF7FFFF	up to 24 MB	Linux kernel
(Linux kernel)				
Flash (firmware)	0xFF800000	0xFFEFFFF	up to 7 MB	Firmware
Flash (U-Boot)	0xFFF00000	0xFFF5FFF	approximately	U-Boot
			320 kB	
Flash	0xFFF60000	0xFFFFFFF	64 kB	Parameters (1 sector)
(parameters)				

Table 5-2 Memory Map for DNF-4-1G-02 CPU (DNF-CPU-1000-02)

Device	Start Address	End Address	Size	Description
SDRAM	0x0	0xFFFFFF	256MB	SDRAM_ADDRESS
Exception table	0x0	0x3000	12 kB	Processor address map
CPU card address	0xA00E0000	0xA00EFFFC	64 kB	EXT_SRAM_ADDRESS
Processor RAMBAR	0xE0000000			
Module – CS2	0xA0000000	0xA00FFFFC	1 MB	EXT_DEV_ADDRESS2
Module – CS3	0xA0100000	0xA01FFFFC	1 MB	EXT_DEV_ADDRESS3
Flash (Linux kernel)	0xFE000000	0xFF7FFFF	up to 24 MB	Linux kernel
Flash (firmware)	0xFF800000	0xFFEFFFF	up to 7 MB	Firmware
Flash (U-Boot)	0xFFF00000	0xFFF5FFF	approximately 320 kB	U-Boot
Flash (parameters)	0xFFF60000	0xFFFFFFF	64 kB	Parameters (1 sector)

Table 5-3 Memory Map for DNF-4-1G-03 CPU (DNF-CPU-1000-03)

Device	Start Address	End Address	Size	Description
SDRAM	0x0	0xFFFFFF	256MB	SDRAM_ADDRESS
Exception table	0x0	0x3000	12 kB	Processor address map
CPU card address	0xA00E0000	0xA00EFFFC	64 kB	EXT_SRAM_ADDRESS
Processor RAMBAR	0xE0000000			
Module – CS2	0xA0000000	0xA00FFFFC	1 MB	EXT_DEV_ADDRESS2
Module – CS3	0xA0100000	0xA01FFFFC	1 MB	EXT_DEV_ADDRESS3
Flash (Linux kernel & ROM drive)	0xF8000000	0xFF7FFFF	up to 120 MB	Linux kernel
Flash (firmware)	0xFF800000	0xFFEFFFFF	up to 7 MB	Firmware
Flash (U-Boot)	0xFFF00000	0xFFF5FFF	approximately 320 kB	U-Boot
Flash (parameters)	0xFFF60000	0xFFFFFFF	64 kB	Parameters (1 sector)

Two address ranges are notable for host software:

Module Address Space (0xA0000000 – 0xA00FFFFC and 0xA0100000 – 0xA01FFFFC). The first address range is dedicated for devices located on the CS2 line and it accommodates sixteen modules with 64k memory map each. The second address range is designated for fast devices located in the CS3 line and it accommodates fifteen devices with 16MB memory map each.

5.3 Startup Sequence

After reset, the processor reads the boot-up sequence located at the address shown in **Table 5-1**. The U-boot monitor initializes the processor and the address map, retrieves information from the parameter sector of the flash memory and tests system memory and other system resources.

When the DNF-4-1G starts rebooting, you have the option of interrupting the reboot via a serial terminal connection between the DNF-4-1G and a host PC. In the serial terminal window, if you type <Return> as U-Boot starts executing, the U-Boot sequence will be interrupted. The U-Boot monitor aborts loading firmware into memory and brings up the U-Boot command prompt => (to load new firmware, for example).

Otherwise, U-Boot reads the firmware from the flash memory and stores it in RAM. Then, the monitor executes the firmware.

After initializing, U-Boot performs a command list stored in its environment sector under the bootcmd entry. A standard command to launch DNF-4-1G firmware is "go 0xff800100". U-Boot then gives up control to the firmware code located at 0xFF800100. Firmware self-expands into the DDRAM, initializes the exception table, and starts execution.

5.4 Setting and Reading CPU Core Parameters via Serial Port

There are two ways to set CPU Core Module (CM) parameters. The first one is to use the serial interface and enter commands at the DQ> prompt, and the second one is to use DaqBIOS calls by running an application on the host PC.

To connect through the serial interface, do the following:

- a. Connect a 9-wire serial extender cable between the DNF-4-1G CPU/ NIC module (male plug connector) and your PC COM serial port (female connector). Some cables have female-to-female connectors, so you may have to use a gender-changer.
- b. Set up your terminal to the proper serial port, 57600 bit rate, no parity, eight data bits, and one stop bit.

NOTE: To use the MTTTY executable included with the UEI installation, open mttty.exe in the following directory on Windows machines, and then click **Connect**:

\Program Files(x86)\UEI\PowerDNA\Firmware\mttty.exe

- c. Once a connection to the DNF-4-1G system is established, press <Enter> on the keyboard once. The DNF-4-1G should respond with a "DQ>" prompt (this is a firmware prompt). If you see a "=>" prompt, you are still in U-Boot.
- d. Once you see the "DQ>" prompt, you can type "help <Enter>" to receive a list of all available commands.

5.4.1 Help The help command provides a list of available commands: **Command**

DQ> help

```
help Display this help message
                                        help
    set Set parameter
                                        set option value
   show Show parameters
                                        show
  store Store parameters (flash)
                                        store
   flrd Re-read flash (flash)
                                        flrd
     mw Write wr <addr> <val> [width,b] mw
     mr Read rd <addr> [width,b] [size] mr
   time Show/Set time
                                        time [mm/dd/yyyy] [hh:mm:ss]
   pswd Set password
                                        pswd {user|su}
     ps Show process state #
                                        ps [value]
                                        test [test number]
   test Test something
  simod System Init/Module Cal
                                        simod [routine]
default Default parameters
                                        default
                                        reset [all]
  reset Reset system
 dqping Send DQ_ECHO to <mac addr>
                                        daping
                                       mode {init|config|oper|shutdown} [ID]
  mode Set current mode
    log Display log content
                                        log [start [end]] -1 = clear
   logf Find entry in the log
                                        logf marker [start [end]]
    ver Show firmware version
                                        ver [all]
 devtbl Show all devices/layers
                                        devtbl [logic|verbose]
netstat Show network statistics
                                        netstat
    pdj Print device object
                                        pdj <devno> cl
     sd SD Card Commands
                                        sd <command> <arguments>
   stat Display status
                                        stat [log]
    nif Display nif object
                                        nif
  clear Clear terminal
                                        clear
```

5.4.2 Show System Parameters Command

The **show** command is one of the most frequently used commands. show provides a list of DNF-4-1G system parameters:

DQ> show

name: "IOM-174257" model: 3004 serial: 0174257 fwct: 1.2.0.0 mac: 00:0C:94:02:A8:B1 srv: 192.168.100.2 ip: 192.168.100.2 (1Gbit) gateway: 192.168.100.1 netmask: 255.255.255.0 mac2: 00:0C:94:F2:A8:B1 srv2: 192.168.100.102 ip2: 192.168.100.102 (DOWN) gateway2: 192.168.100.1 netmask2: 255.255.255.0 udp: 6334 license: "" Manufactured 4/6/2017 Calibrated 4/6/2017 DQ>

To change parameters, use the "set" command (type set <Enter> for "set" command syntax).

5.4.3 Set and Store Commands

The set command allows you to change DNF-4-1G system parameters and store allows you to save them to system memory (flash).

Typing set <Enter> provides a list of parameter names that can be changed.

```
DQ> set
Valid 'set' options:
       name: <Device name>
       model: <Model id>
      serial: <Serial #>
        fwct: <autorun.runtype.portnum.umports>
         mac: <ethernet address port 1>
         srv: <Default IP address port 1>
          ip: <IOM IP address port 1>
     gateway: <gateway IP address port 1>
     netmask: <netmask port 1>
        mac2: <ethernet address port 2>
        srv2: <Default IP address port 2>
         ip2: <diagnostic port IP address>
    gateway2: <diagnostic port gateway IP>
    netmask2: <diagnostic port netmask>
         udp: <udp port (dec)>
     license: license string
```

NOTE: The set command may require a password. The default password for DNF-4-1G systems is "powerdna".

The following are examples of setting DNF-4-1G parameters:

• To set a new Primary IP address (NIC1), type:

```
DQ> set ip 192.168.1.10
```

To set a new Secondary Diagnostic Port IP address (NIC2), type:

```
DQ> set ip2 192.168.100.3
```

Other parameters can be changed the same way. Refer to Section 5.4.3.1 for more information about each of the set parameters.

Once parameters are set, you must store them into non-volatile flash memory:

```
DQ> store

CRC: crc=0x625660CF flcrc=625660CF

Flash: 1244 bytes of 1244 stored! CRC=0x625660CF

Old=0x88EB57ED

Configuration stored

DQ>
```

After parameters are stored, reset the firmware.

DQ>

5.4.3.1 Setting
Parameters
Via Serial
Interface

Refer to **Table 5-4** for descriptions of DNF-4-1G system parameters that can be read or modified with the set command.

Table 5-4 Set Parameters

Set Parameter <argument></argument>	Description
name <device name=""></device>	Sets the device name (up to 32 characters)
<model></model>	Device model (factory programmed, do not change)
<serial></serial>	DNF-4-1G serial number (factory programmed, do not change)
<mac mac2="" or=""></mac>	DNF-4-1G MAC Ethernet address (factory programmed, do not change)
fwct <autorun.runtype.portnum.umports></autorun.runtype.portnum.umports>	Defines the behavior of the U-Boot upon boot-up. The following are valid values for each field. • for "autorun": 1 - copy firmware to SDRAM memory location and execute from there • for "runtype": 2 for the DNF • for "portnum" and "umports" should be 0 (zero)
srv <host address="" ip=""></host>	Sets the host IP address for connection with the IOM primary port (NIC1). You have to set the host IP address only if raw Ethernet protocol is in use (used in homogenous IOM networks only.) This parameter is ignored when the DNF-4-1G system is used over the UDP protocol or from the host.
ip <iom address="" ip=""></iom>	Specifies the IOM primary IP address (NIC1). This is a critical parameter the user must change to allow the DNF-4-1G system to be visible on the network. The DNF-4-1G responds to every UDP packet containing a DaqBIOS prolog sent to this address. Since the current release does not support DHCP, the user should set up the IP address.
gateway <gateway address="" ip=""></gateway>	Specifies where the DNF-4-1G (NIC1) should send an IP packet if a requested IP packet exists outside of the DNF-4-1G network (defined by the network mask).
netmask <network mask=""></network>	Specifies what type of subnet the DNF-4-1G (NIC1) is connected to. The factory sets netmask to Type C IP network – 254 nodes maximum
srv2 <host address="" ip=""></host>	Sets the host IP address for connection with the IOM diagnostic (secondary) port (NIC2).
ip2 <iom address="" ip=""></iom>	Specifies the IOM diagnostic (secondary) IP address (NIC2).
gateway2 <gateway address="" ip=""></gateway>	Specifies the IOM diagnostic (secondary) gateway (NIC2).
netmask2 <network mask=""></network>	Specifies the IOM diagnostic (secondary) subnet mask (NIC2).

NOTE: More information about changing the IP address and other network settings is provided in "IP Address Overview & Update Procedures" on page 21.

5.4.4 Reset DNF-4-1G Command

The **reset** command performs a physical reset of the CPU and initiates the full startup sequence on the DNF-4-1G system:

DQ> reset
Stopping DaqBIOS

U-Boot 1.1.3 (PowerDNA 8347 3.2.4) (Mar 24 2014 - 12:31:23) MPC83XX

Clock configuration:

<...many U-Boot messages deleted...>

Net: Freescale TSEC0:- PHY is Realtek RTL8212 (1cc912)

PHY is Freescale TSEC0

W:9140 rg:0 Gig-E controller found

W:1140 rg:0 EthController Freescale TSEC0

Hit any key to stop autoboot: 0

Starting application at 0xFF800100 ...

Welcome to PowerDNA!

PowerDNA (C) UEI, 2001-2017. Running PowerDNA Firmware on MPC8347 (128MB)

Built on 09:45:43 Jul 7 2017

Initialize uC/OS-II (Real-Time Kernel v.280)

os...

CM-4 PPC8347 detected

5 devices detected

Address	Irq	Model	Option	Phy/V	irt S/N	Pri D	evN
0xA0000000	2	553	1	phys	0180348	10	0
0xA0010000	2	208	1	phys	0159249	20	1
0xA0020000	2	501	1	phys	0173904	30	2
0xA0030000	2	650	1	phys	0175203	40	3
0xA00D0000	0	46	1	phys	0174269	50	4
0xA00E0000	2	5	1	cpu	0174257	0	14

Current time: 11:56:30 11/21/2017

Starting filesystem... (H)

SD card is not present.

Power DNA version 4.8.0 release build 81

Built on 09:45:43 Jul 7 2017

396MHz MPC8347 DCache:32k uC/OS v.280 is running

Enter 'help' for help.

DQ>

5.4.5 Password Command

Some commands (such as mr, mw, set, and store) require entering a user password. Once the password is entered, these commands become enabled until firmware reset.

There are two levels of password protection available. The first is user level and the second is super-user level. Super-user level is currently used only for updating firmware over the Ethernet link.

- DQ> pswd user sets up a user level password. First, you'll be asked about your old password and then (if it matches) to enter the new password twice.
- DQ> pswd su sets up super-user level password. First, you'll be asked about old super-user password and then (if it matches) to enter the new super-user password twice.

DNF-4-1G systems come with both default passwords set to "powerdna".

Some DaqBIOS commands require clearing up user or super-user password. Use **DqCmdSetPassword()** before calling these functions. The *PowerDNA API Reference Manual* notes which functions are password-protected.

5.4.6 Display Table of Installed Boards & Logic Version Command

The devtb1 command is another of the more frequently used commands. This command displays all I/O boards found and initialized by firmware along with assigned device numbers.

Use these device numbers in host software to address the I/O devices.

DQ> devtbl

Address	Irq	Model	Option	Phy/V	irt S/N	Pri	DevN
0xA0000000	2	553	1	phys	0180348	10	0
0xA0010000	2	208	1	phys	0159249	20	1
0xA0020000	2	501	1	phys	0173904	30	2
0xA0030000	2	650	1	phys	0175203	40	3
0xA00D0000	0	46	1	phys	0174269	50	4
0xA00E0000	2	5	1	cpu	0174257	0	14

DQ>

The devtbl command with the logic option added displays the CPU logic version on each installed I/O board:

DQ> devtbl logic Logic information:

DevN Mod-opt		CLI	CLO	LogOption	
0 553-001	02.11.B0	0	0	83000404	
1 208-001	02.12.2D	512	512	10127E0	
2 501-001	02.11.08	0	0	9008004	
3 650-001	02.11.36	1024	0	43000040	
13 046-001	02.10.EE	0	0	1010081	
14 3004-001	02.12.3E	0	0	30303720	

DQ>



The **devtbl** command with the **verbose** option added displays detailed information about each installed I/O board:

DQ> devtbl verbose Logic capabilities: Device:0 model:553-001

- 2-wire interface is used
- Disabled NIS-->IS selector in cli_sync module

Device:1 model:208-001

- Logic compiled for CYCLONE family
- 16.5MHz serial isolation interface speed based on 66MHz system clock
 - 2-wire interface is used
 - Includes NIS-->IS serializer
 - Includes IS-->NIS deserializer
 - PWM output enabled for the TMR0/TMR1 timers in SYNC module
 - Standard input channel list implementation used
 - Standard output channel list implementation used

Device: 2 model: 501-001

- IS-->NIS selector is disabled in cli_sync module
- Disabled NIS-->IS selector in cli_sync module

Device:3 model:650-001

- Standard input channel list implementation used

Device: 4 model: 046-001

- Logic compiled for CYCLONE family
- PWM output enabled for the TMR0/TMR1 timers in SYNC module
- 8-bit output test port is unavailable

5.4.7 Display Power Diagnostics Command

Typing simod 5 at the serial prompt displays diagnostic information about the DNF-4-1G CPU board. This diagnostic information includes actual voltage readings on each of the 2.5V, 24V, 1.2V, 3.3V, and 1.5V supplies, as well as actual temperature and current measurements.

```
DO> simod 5
DNF_PWR_1G layer diagnostics
   2.5DNx= 2.516*
                      GND1 = 0.000*
   3.3DNx = 3.313*
                     U-Cap= 0.022*
    24DNx=24.221*
                       Vin=23.886*
   1.5DNx= 1.575*
                    1.2DNx= 1.275*
    VfanX= 0.022!
                      Iin= 0.201*
    I 3.3= 0.896*
                     I 1.5= 0.231*
    Temp1=23.343*
                     Temp2=23.436*
Unit logged 38.6 hours
DQ>
```

5.4.8 Memory Test/ Memory Clear Command

Typing simod 7 performs a memory test on the DNF-4-1G CPU address space.

The test writes standard memory test bit patterns to each memory location and then reads each location back and verifies. At the end, it reports any bit mismatches.

Note that this memory test writes over any content in that memory space; therefore, it can be used to clear memory, as needed.

```
DQ> simod 7
Memory test/clear
Clear memory and reboot? y/[n]>n
CPU layer memory test
Start addr=0x00200000 End addr=0x07FFFFC (125MB)
Total errors: 0
DQ>
```

Typing "y" after "Clear memory and reboot? y/[n]>" causes the chassis to automatically reboot.

```
DQ> simod 7
Memory test/clear
Clear memory and reboot? y/[n]>y
CPU layer memory test
Start addr=0x00200000 End addr=0x07FFFFFC (125MB)
ADDR: 0x04C00000 (76MB) errors=0
```

<...memory test completes and then system reboots...>

5.4.9 Monitor CPU and Pbuf

and Pbuf Usage Command Entering simod 15 at the serial command prompt causes the CPU and packet buffer load to continuously print to the serial console.

simod 15 can be used to monitor the DNF-4-1G serial port while your application is sending and receiving control words and data over Ethernet.

```
DQ> simod 15
Printing statistics
+cpu:1 pbuf:avail:576 used:20 max:20 err:0
+cpu:12 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
```

5.4.10 Clock and Watchdog Access

The time command shows and sets up the date and time on the DNF-4-1G system:

DQ> time

Command Current time: 14:56:17 09/01/2017

To set up time of the time of day, enter:

DQ> time 17:40:00

To set up date, enter:

DQ> time 11/03/2017

Date and time are stored in the battery-backed real-time clock chip.

Appendix A

Network Interface Card Configuration

A.1 Configuring an Ethernet Card Under Windows 7

A.1 Configuring an To configure an Ethernet card for your system, use the following procedure:

A. Set Up Your Ethernet Network Interface Card (NIC).

If you already have an Ethernet card installed, skip ahead to the next section, "Configure TCP/IPv4".

If you have just added an Ethernet card, to install it, do the following:

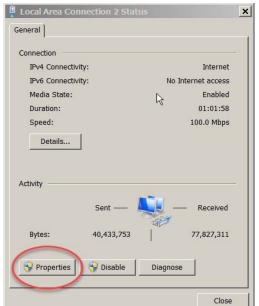
- **STEP 1:** From the *Start* menu, and select *Control Panel*.
- **STEP 2:** Under *Printers and Other Hardware*, click *Add a device* and follow the on-screen instructions.

NOTE: We recommend that you allow Windows to search for and install your Ethernet card automatically. If Windows does not find your Ethernet card, you will need to install it manually by following the manufacturer's instructions.

Once your Ethernet card has been installed, continue to the next section.

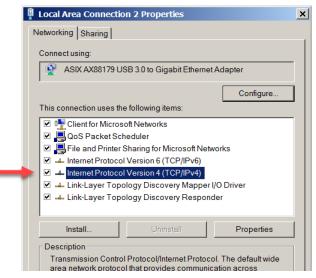
B. Configure TCP/IPv4.

- STEP 1: From the Start menu, select Control Panel.
- STEP 2: In the Control Panel window, click Network and Internet.
- STEP 3: In the Network and Internet window, click Network and Sharing Center.
- **STEP 4:** In the left sidebar of the Network and Sharing Center window, click *Change adapter settings*.
- **STEP 5:** Double-click the icon for the network interface you are connecting as your NIC. This is typically under a *Local Area Connection* heading.



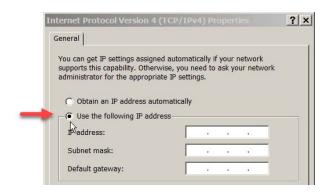
STEP 6: In the Local Area Connection Status window, click Properties:

STEP 7: In the Local Area Connection Properties window, verify the Networking tab is selected, and double-click *Internet Protocol Version 4 (TCP/IPv4)*.



STEP 8: If Internet Protocol (TCP/IPv4) is not listed, click **Install** and follow directions on the screen.

STEP 9: Click the *Use the following IP address* button (see Figure below). Note any addresses listed in the *IP Address*, *Subnet Mask*, *Default Gateway*, *Preferred DNS Server* or *Alternate DNS Server* fields. You may want to re-enter them later to reconfigure your PC, if needed.



In the *IP address* field, type the IP address for the host PC NIC port (e.g., 192.168.100.1).

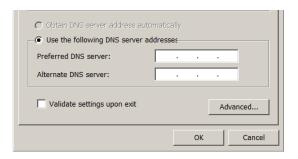
In the Subnet mask field, type 255.255.25.0.

Leave the Default Gateway field blank.

NOTE: In the above example, setting the host PC NIC address to 192.168.100.1 with a subnet mask of 255.255.255.0 allows the host PC to communicate with components having IP addresses from 192.168.100.2 through 192.168.100.254 via that NIC port.

All UEI cubes and racks on this network will need to have IP addresses unique and in that range. (The default IP address of the UEI FLATRACK is 192.168.100.2.)

STEP 10: Select *Use the following DNS server addresses* and verify the *Preferred DNS server* fields and the *Alternate DNS server* fields are blank.



Internet Protocol Version 4 (TCP/IPv4) Properties ? × General You can get IP settings assigned automatically if your network supports this capability. Otherwise, you need to ask your network administrator for the appropriate IP settings. Obtain an IP address automatically Use the following IP address-192 . 168 . 100 . 1 255 . 255 . 255 . 0 Subnet mask: Default gateway: Obtain DNS server address automatically Use the following DNS server addresses Preferred DNS server: Alternate DNS server: Validate settings upon exit Advanced.. Cancel ОК

STEP 11: Click **OK** in the *TCP/IPv4 Properties* window (see figure below).

- **STEP 12:** Click **OK** in the *Local Area Connection 2 Properties* window, and click **Close** in the *Local Area Status* window.
- STEP 13: Close the Control Panel window.



For instructions on setting the IP address, subnet mask, and default gateway on a UEI chassis, refer to "IP Address Overview & Update Procedures" on page 21.

Appendix B

Field Replacement of Fuses on DNx Boards

Some boards used in UEI DAQ I/O systems require field replacement of fuses when unexpected overloads occur. Locations of these fuses are shown in **Figure B-1** through **Figure B-3**. Part numbers for the replacement fuses are listed **Table B-1**.

Table B-1 DNA/DNR Replacement Fuses

UEI Fuse	Detino	UEI Part	Description	BAC.	Mr. DAI
ID (Board)	Rating	No.	Description	Mfr.	Mfr P/N
F1	5A	925-5125	FUSE 5A 125V SLO SMD SILVER T/R	Littlefuse	0454005.MR
F2	5A	925-5125	FUSE 5A 125V SLO SMD SILVER T/R	Littlefuse	0454005.MR
F3 (DC)	5A	925-5125	FUSE 5A 125V SLO SMD SILVER T/R	Littlefuse	0454005.MR
F3 (1GB)	10A	925-1125	FUSE 10A 125V FAST NAN02 SMD	Littlefuse	0451010.MRL
F4	5A	925-5125	FUSE 5A 125V SLO SMD SILVER T/R	Littlefuse	0454005.MR

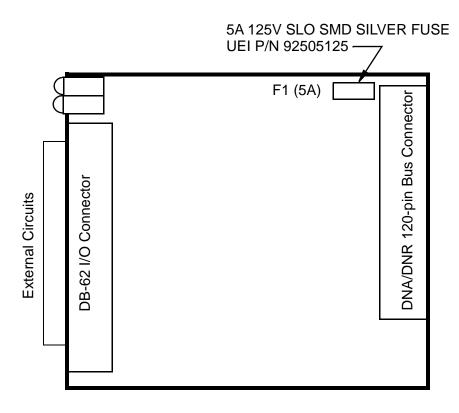


Figure B-1. Location of Fuse for Base Boards Equipped with a Fuse

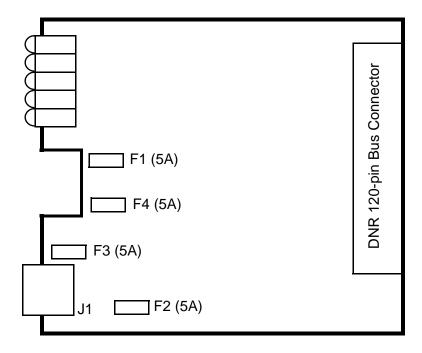


Figure B-2. Location of Fuses for DNR-POWER-DC Board

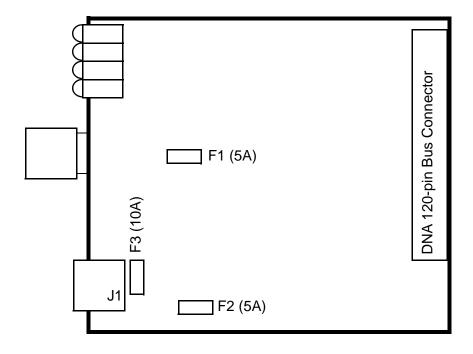


Figure B-3. Location of Fuses for DNR-POWER-1GB Board

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