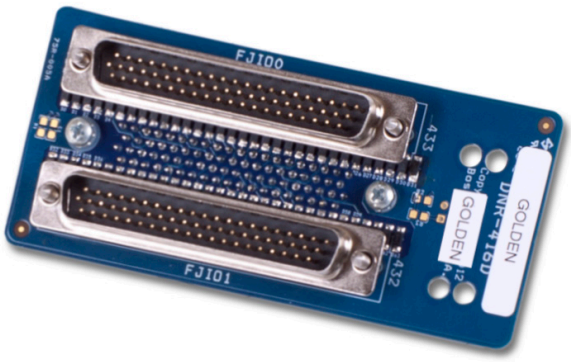
DNR-DIO-416-32

32-Channel Solenoid Drive Output System

- For use with RACKtangle™ I/O chassis
- 32 digital output pairs
- 500 mA per channel maximum current drive
- 125Hz per channel max. output rate
- Ideal for driving solenoids and other inductive loads
- FET transistors for high- and low-side outputs
- Resettable overload circuit breaking on every channel
- Output current monitoring for short/open detection and state confirmation
- Switches 3.3 to 48 V loads



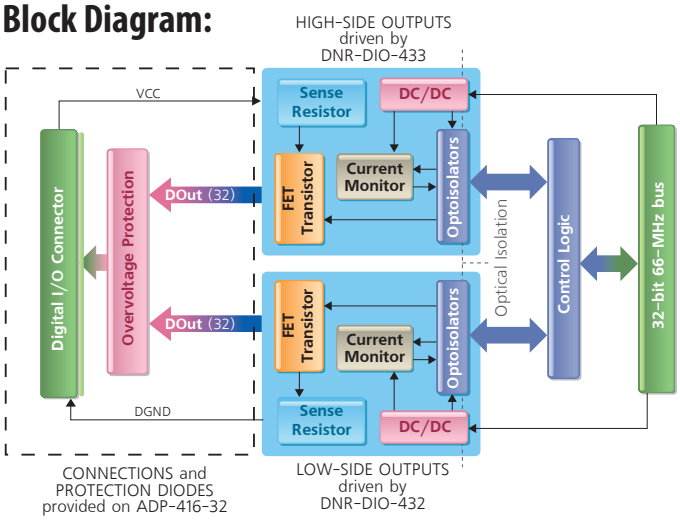
General Description:

The DNR-DIO-416-32 is a 32-channel digital output product designed for driving solenoids or other inductive loads. The product is created by combining a DNR-DIO-432, DNR-DIO-433 and ADP-416-32. The DIO-432/433 provides all the switching and system monitoring capability while the ADP-416-32 provides protection diodes as well as makes the appropriate interconnections.

The digital outputs are controlled by FETs (field effect transistors) and provide FET control on both the high side and low side of the load. DNA/DNR-DIO-416 features redundant support diodes on every channel and provides overvoltage (kickback) and overcurrent protection. Output current monitor offers 0.5% accuracy and may be used to trigger an automatic overload shut down, detect output short/open circuits and to confirm each channels output state The user may select the current and duration of an overload (as short as 10 mS) required for channel turn off. The layer is designed to switch loads from 3.3 up to 48 Volts DC.

Software is included, providing a comprehensive, yet easy-to-use API that supports all popular operating systems, including Windows, Linux, and most real-time operating systems—such as QNX, Intime, VXworks, and more. Additionally, the UEIDAQ Framework—an even higher level Windows driver—supplies complete support for those creating applications in many popular Windows programming languages, as well as data acquisition software packages such as LabVIEW and MATLAB/Simulink.

Block Diagram:



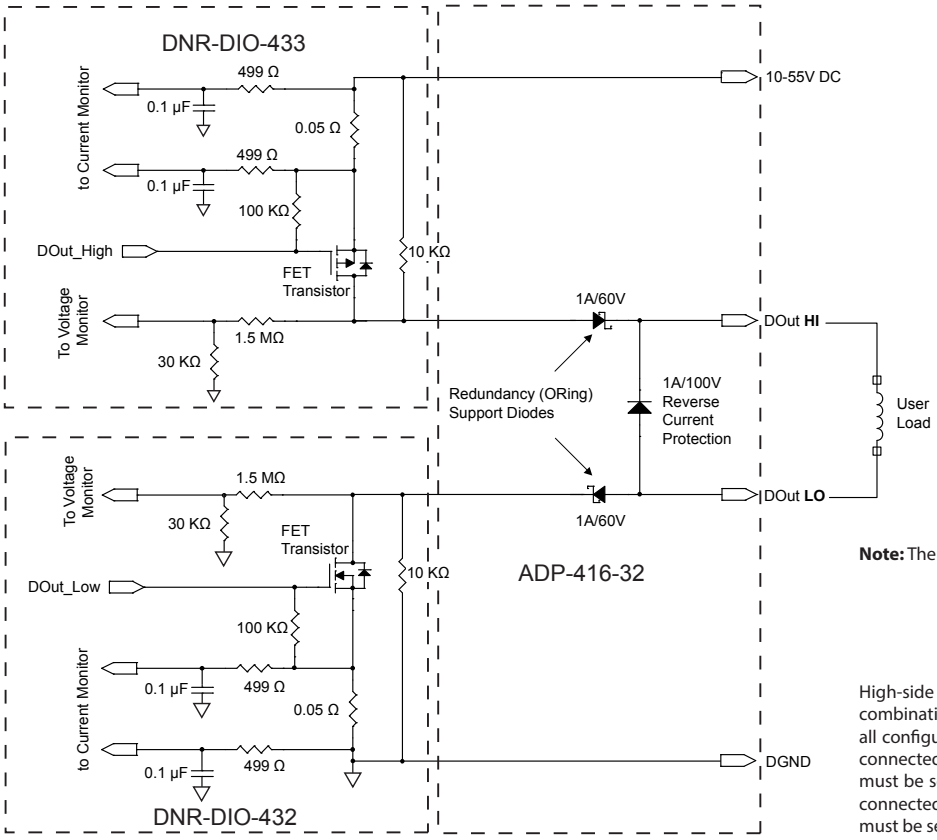
Technical Specifications:

Number of channels	32 digital outputs (32 pairs or 32 high- or 32 low-side)
Drive Capacity	500mA per channel continuous max; 1A per channel max peak (1 sec max)
Output Rate	125Hz per channel max
Off leakage current	< 25 µA
Output Protection	±90V peak; 2kV ESD
Circuit Breaker: Current limit Overload Response time	 50mA - 1A (user-programmable) 10-5000ms (user programmable)
Current/Voltage Monitor: Resolution ADC Speed Sense Resistor Over-current shut down Current measurement range Accuracy Noise Interrupts (maskable) Limit Override Voltage monitor range Voltage montor accuracy	(each channel) 24-bit ADC 0.6 to 293 Hz 0.025Ω may be set from 0-2A 0-2A 0.5% of full scale < 1 mA 2 per channel (over/under-current) Programmable per channel 0 to Vcc (55 V max) ±10 mV
Normal Operating Range	3.3-48V
Absolute Max Voltage	55 V
Power Consumption	< 4W from RACKtangle backplane
Power Dissipation	< 24W including IR dissipation in switches
Isolation	350Vrms
Power up / reboot state	All outputs OFF
Operating Temp. Range	Tested -40 to 85°C
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500 Hz, broad-band random
Shock *IEC 60068-2-27* *IEC 60068-2-64*	100 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations
Altitude	120,000 ftv
MTBF (Hours)	130,000
Operating Humidity	0 - 95%, non-condensing

Cables and Screw Terminal Panels

Part Number	Description
DNA-CBL-78	78-conductor, 3 foot ribbon cable

High-Low Channel Pair Diagram:



Note: There are three possible channel configurations.

- High-side and Low-side pair (Shown)
- High-side only
- Low-side only

High-side and Low-side outputs cannont both be used except in the paired combination shown. Vcc (10-55 VDC) must be supplied at the connector in all configurations. When configured as high side only, the load should be connected between Out0 pin (or 2, 4, ... 14) and GND, and the low side FET must be set as OFF. When configured as low-side only the load should be connected between Out1 pin (or 3, 5, ... 15) and VCC and the high-side FET must be set as OFF.

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Pinout Diagram