United Electronic Industries

The High-Performance Alternative

DNR-MIL and DNR-MIL-6 Series RACKtangle™ Data Acquisition Systems User Manual

December 2020 Edition
PN Man-DNR-MIL

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Specifications in this document are subject to change without notice. Check with UEI for current status.

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Chapter 1 Introduction

This document describes the features, performance specifications, and operating functions of the DNR-MIL and DNR-MIL-6 Series RACKtangle™ data acquisition systems.

Chapter 1 provides the following information about the DNR-MIL:

- Organization of This Manual (Section 1.1)
- Product Versions Described in This Manual (Section 1.2)

1.1 Organization of This Manual

The DNR-MIL User Manual is organized as follows:

- **Chapter 1 – Introduction**
  This chapter describes the organization of the document, the conventions used throughout the manual, and product versions described in this manual.
- **Chapter 2 – DNR-MIL RACKtangle™ System**
  This chapter provides an overview of a DNR-MIL system, component modules, features, accessories, and a list of all items you need for initial operation.
- **Chapter 3 – DNR-MIL-6 RACKtangle™ System**
  This chapter provides an overview of a DNR-MIL-6 system, component modules, features, accessories, and a list of all items you need for initial operation.
- **Chapter 4 – Installation and Configuration**
  This chapter summarizes the recommended procedures for installing, configuring, starting up, and troubleshooting a DNR-MIL system.
- **Chapter 5 – PowerDNA Explorer**
  This chapter provides a general description of the menus and screens of UEI's GUI-based communication application, PowerDNA Explorer, when used with a DNR-MIL system.
- **Chapter 6 – The DNR-MIL-x CPU**
  This chapter describes the device architecture of the DNR-MIL-x CPU module.
- **Chapter 7 – CPU Programming in PowerDNA Mode**
  This chapter describes tools and facilities used for programming CPU board-specific functions in hosted deployments.
- **Appendix A – Configuring Additional Ethernet Cards**
  The appendix describes procedures for configuring Ethernet cards on the host PC for use with Windows operating systems.

Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:

Tips are designed to highlight quick ways to get the job done, or reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.

CAUTION! *advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

Text formatted in **bold** typeface generally represents text that should be entered verbatim. For instance, it can represent a filenames, as in the following example: "You can instruct users how to run setup using **setup.exe** executable."

Bold typeface will also represent button names, as in "Click **Scan Network**."

Text formatted in `fixed` typeface generally represents commands, source code, or other text that should be entered verbatim into the source code, initialization, or other file or at a command prompt.

Before plugging any I/O connector into the Cube or Board, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

Usage of Terms

Throughout this manual, the term "Cube" refers to either a PowerDNA Cube product or to a PowerDNA *RACKtangle*™ or *HalfRACK*™ or *FLATRACK*™ rack mounted system, whichever is applicable.

1.2 Product Versions Described in This Manual

This user manual provides documentation for the DNR-MIL and DNR-MIL-6 series RACKtangle data acquisition system hardware. Electronically, the DNR-MIL RACKtangle is identical to the standard DNR series RACKtangle except for the added hold-up and protection circuitry added to the power supply inputs. The main difference between DNR-MIL and DNR-MIL-6 is the number of slots available for I/O boards. When applicable to both systems, this manual refers to them collectively as DNR-MIL-x.

Table 1-1 summarizes the features of the different MIL hardware options. Each hardware option can be deployed in either PowerDNA hosted mode or UEIPAC/SIM/Modbus/OPCUA stand-alone mode. While this manual will focus on DNR-MIL-x hosted deployments, the hardware information in DNR-MIL(Chapter 2) and DNR-MIL-6 (Chapter 3) also applies to UEIPAC/SIM/Modbus/OPCUA-1200-MIL and UEIPAC/SIM/Modbus/OPCUA-600-MIL products respectively.

For more information about stand-alone deployments, please see the following manuals:

- UEIPAC-x-MIL
  - -00/02/03: “UEIPAC Software Manual”
  - -11/12: “UEIPAC SoloX Hardware Manual”, “UEIPAC SoloX Software Manual”
- UEIModbus-x-MIL: “UEIMOD User Manual”
- UEISIM-x-MIL: “UEISim User Manual”
- UEIOPCUA: “UEIOPCUA Manual”

Table 1-1 Summary of DNR-MIL Products

Option	Part Number (Hosted mode)	Part Number (Standalone mode)	Features
-00	DNR-MIL-x	UEIPAC-x-MIL UEISIM-x-MIL UEIModbus-x-MIL UEIOPCUA-x-MIL	• NXP-Freescale MPC8347 CPU • 10/100/1000Base-T Ethernet interface • 1PPS synchronization[1] • 256 MB RAM[2] • 32 MB flash memory[2]
-02	DNR-MIL-x-02	UEIPAC-x-MIL-02 UEISIM-x-MIL-02 UEIModbus-x-MIL-02 UEIOPCUA-x-MIL-02	Same as -00 plus optional solid-state hard drive[3]
-03	DNR-MIL-x-03	UEIPAC-x-MIL-03 UEISIM-x-MIL-03 UEIModbus-x-MIL-03 UEIOPCUA-x-MIL-03	• NXP-Freescale MPC8347E CPU (encryption-ready, IPSec support pending) • 10/100/1000Base-T Ethernet interface • 1PPS/IEEE-1588 synchronization[1] • 256 MB RAM[2] • 128 MB flash memory[2] • Optional solid-state hard drive[3]
-11	not available	UEIPAC-x-MIL-11 UEISIM-x-MIL-11 UEIModbus-x-MIL-11 UEIOPCUA-x-MIL-11	• NXP i.MX6 SoloX Series ARM CPU (dual core: Cortex-A9 & Cortex-M4) • 10/100/1000Base-T Ethernet interface • 1PPS/IEEE-1588 synchronization[1] • 1 GB RAM • 8 GB flash memory (& U-boot QSPI flash) • Optional solid-state hard drive[3] • Optional GSM / Wireless support
-12	not available	not available in MIL chassis	Same as -11 plus HDMI interface

1. 1PPS and IEEE-1588 synchronization support is described in the PowerDNx 1PPS Sync Interface Manual.
2. RAM and flash memory are not user-accessible for PowerDNA applications (hosted deployment). Portions of RAM and flash are available for user applications for UEIPAC-based systems (stand-alone deployments).
3. On UEIPAC-based systems (stand-alone deployment), solid state drives are used for data and/or root file system storage.

Chapter 2 The DNR-MIL RACKtangle System

This chapter provides the following information about the DNR-MIL Series RACKtangle™ system:

- The DNR-MIL System (Section 2.1)
- Specifications (Section 2.2)
- Key Features (Section 2.3)
- DNR-MIL System Enclosure (Section 2.4)
- DNR-MIL CPU/NIC Module (Section 2.5)
- DNR-MIL Backplane & Power (Section 2.6)
- DNR-MIL I/O Boards (Section 2.7)
- Pinouts, Connectors & Cables (Section 2.8)

NOTE: Information in this chapter applies to all 12-slot DNR-MIL-series RACKtangle systems unless otherwise noted. This includes UEIPAC-1200-MIL, which shares the same hardware as DNR-MIL. For a list of CPU options, refer to Section 1.2 on page 3.

2.1 The DNR-MIL System

The UEI DNR-MIL RACKtangle™ system is a compact, rugged and highly integrated Ethernet I/O data acquisition platform. The DNR-MIL series is a military version of the PowerDNA Ethernet-based Data Acquisition System that provides a rugged chassis for military applications that require up to twelve I/O boards per chassis. All standard DNA I/O boards are also available in DNR versions for use in DNR-MIL systems.

Figure 2-1. Typical DNR-MIL RACKtangle System

The PowerDNA-based RACKtangle system consists of the following boards:

- DNR-MIL-ENCL rack mounted enclosure
- DNR-CPU-x module (includes CPU and 1-GB Ethernet 1000 Base-T Network Interface Board)

To configure a complete data acquisition system, install up to 12 DNR I/O boards into each DNR-MIL rack enclosure, which may be specified in any combination of the following types:

- DNR-AI-series for Analog Inputs (incl. Strain, TC, RTD, ICP, LVDT, ...)
- DNR-AO-series for Analog Outputs (voltage, current, strain gage, ...)
- DNR-DIO-series for Digital Inputs/Outputs and Relays
- DNR-CT-series for Counters/Timers/PWM/Quadrature, IRIG
- Serial & HDLC (DNR-SL), CAN bus, Synchronous Serial Interface (SSI)
- Avionics for ARINC 429, DNR-MIL-1553, and more

Refer to www.ueidaq.com for a description of each I/O board and a catalog of the most recent set of boards. The website also lists PowerDNA™ accessories available for use in a DNR-MIL system.

NOTE: Though it is possible to replace various boards within the DNR-MIL, it is recommended that the modification be done and tested by UEI.

The DNR-MIL system can be configured in the following modes of operation:

- PowerDNA Mode - Host-controlled Operation
- UEIPAC - Programmable Automation Controller
- UEISIM - Simulink / Simulink Coder Target
- UEIModbus - Modbus TCP-based Controller
- UEIOPCUA - OPC-UA Server, accessed by any OPC-UA client

2.2 Specifications

Figure 2-2 lists the specifications of the DNR-MIL system for PowerDNA hosted deployments options -00, -02, and -03.

Computer Interface	**DNR-MIL-00/02/03**
Primary Ethernet Port	10/100/1000Base-T, 38999 connector
Diagnostic Port	10/100/1000Base-T, 38999 connector
Config/Serial Port	RS-232, 38999 connector
Sync	1. DNR-SYNC-1G series cables and boards provide both clock and trigger sync signals. 2. DNR-IRIG-650 board provides IRIG and GPS time synchronization
I/O Board Support	
Series supported	All DNR-series boards
Processor/system	
CPU	Freescale 8347, 400 MHz, 32-bit
Memory (RAM)	256 MB
Memory (Flash)	32 MB
Host Communications	
Distance from host	100 meters max, CAT5 cable
Ethernet data transfer rate	20 megabyte per second
Analog data transfer rate	>6 megasample per second. Capable of sustained transfer in any RACKtangle configuration
DMAP I/O mode	update >1,000 I/O channels at 4 kHz, guaranteed
Physical Dimensions / Weight	
12 I/O slots	17.5" x 8.1" x 7.0", 22 lbs incl. I/O boards
Environmental*	
Electrical Isolation	350 Vrms
Temp (operating)	-40 °C to 70 °C
Temp (storage)	-40 °C to 85 °C
Humidity	0 to 95%, non-condensing
Vibration	MIL-STD-810G plus the IEC specs below
(IEC 60068-2-64)	10–500 Hz, 5 *g* (rms), Broad-band random
(IEC 60068-2-6)	10–500 Hz, 5 *g*, Sinusoidal
Shock	MIL-STD-810G plus the IEC stds below
(IEC 60068-2-27)	100 *g*, 3 ms half sine, 18 shocks at 6 orientations; 30 *g*, 11 ms half sine, 18 shocks at 6 orientations
Altitude	70,000 feet, maximum
EMI / RFI	Designed to meet MIL-STD-461
Power Requirements	
Voltage	9 - 36 VDC (115/220 VAC adaptor available)
Power	12 Watts (not including I/O boards)
Power Quality requirement	Designed to meet MIL-STD-1275
Reliability	
MTBF	130,000 hours

Figure 2-2. DNR-MIL-00/02/03 Technical Specifications (PowerDNA mode)

Figure 2-3 lists the specifications of the DNR-MIL system for stand-alone deployments options -00, -02, and -03. UEIPAC specifications also apply to UEISIM, UEIModbus, and UEIOPCUA configurations.

Computer Interface	**UEIPAC 1200-MIL-00/02/03**
Primary Ethernet Port	10/100/1000Base-T, 38999 connector
Diagnostic Port*	10/100/1000Base-T, 38999 connector *Alternatively can be teamed/bonded with primary port.
Config/Serial Port	RS-232, 38999 connector
USB Port	USB 2.0 fully supported
Synchronization Options	1. DNR-SYNC-1G series cables and boards provide both clock and trigger sync signals. 2. DNR-IRIG-650 board provides IRIG and GPS time synchronization 3. PTP client provides software implementation of IEEE-1588
I/O Board Support	
Series supported	All DNR-series boards
Software / Operating System	
Embedded OS	Linux, kernel 2.6.x (VxWorks Available)
Real-time support	Xenomai RTOS support
Dev Language	C/C++, Eclipse IDE support,
Dev Environments	Linux PC or Cygwin Windows environment
EPICS CAS interface	Yes
SNMP Library	Yes
OS royalties	none
Processor/system	
CPU	Freescale 8347, 400 MHz, 32-bit
Memory	256 MB (128 MB avail for application SW)
FLASH memory	32 MB (16 MB available for user apps)
SD card interface	SD cards up to 32 GB
USB drive interface	Standard USB 2.0 port
Physical Dimensions	
12 I/O slots	17.5" x 8.1" x 7.0", 22 lbs incl. I/O boards
Environmental	
Electrical Isolation	350 Vrms
Temp (operating)	-40 °C to 70 °C
Temp (storage)	-40 °C to 85 °C
Humidity	0 to 95%, non-condensing
Vibration	MIL-STD-810G plus the IEC specs below
(IEC 60068-2-64)	10–500 Hz, 5*g* (rms), Broad-band random
(IEC 60068-2-6)	10–500 Hz, 5 *g*, Sinusoidal
Shock	MIL-STD-810G plus the IEC stds below
(IEC 60068-2-27)	100 *g*, 3 ms half sine, 18 shocks at 6 orientations; 30 *g*, 11 ms half sine, 18 shocks at 6 orientations
Altitude	70,000 feet, maximum
EMI / RFI	Designed to meet MIL-STD-461
Power Requirements	
Voltage	9 - 36 VDC (115/220 VAC adaptor available)
Power	12 Watts (not including I/O boards)
Power Quality requirement	Designed to meet MIL-STD-1275
Reliability	
MTBF	130,000 hours

Figure 2-3. UEIPAC-1200-MIL-00/02/03 Technical Specifications

Figure 2-4 lists the specifications of the DNR-MIL system for stand-alone deployments option -11. UEIPAC specifications also apply to UEISIM, UEIModbus, and UEIOPCUA configurations.

Computer Interface	**UEIPAC 1200-MIL-11**
Primary Ethernet Port	10/100/1000Base-T, 38999 connector
Diagnostic Port	10/100/1000Base-T, 38999 connector
M2 PCIe slot (internal)	1 slot, 22 or 30 width, 42, 60 or 80 length, B key
Net Teaming/bonding	Supported in both Linux and VxWorks deployments
Config/Serial Port	RS-232 port on LAN/COM 38999
USB Port	USB 2.0 fully supported
Synch Options	Sync input/output port or IEEE-1588
I/O Board Support	
Series supported	All DNR/DNA-series boards as appropriate
Software / Operating System	
Embedded OS	Linux, kernel 4.9.x or VxWorks 7.x
Real-time support	4.9.88 kernel based Real-time Linux, VxWorks is a real-time OS
EPICS CAS interface	Yes (Linux version)
SNMP Library	Yes
Processor/system	
CPU	SoloX / i.MX6 series ARM processor Cortex A9 core @ 1Ghz
Memory	1 Gbyte RAM
FLASH memory	8 Gbyte
Solid-State Hard Drive	Optional 8 or 16 GB drives available
µSD card interface	µSD cards up to 128 GB
USB drive interface	Standard USB 2.0 port
Physical Dimensions	
12 I/O slots	17.5" x 8.1" x 7.0", 22 lbs incl. I/O boards
Environmental	
Temp (operating) UEIPAC 1200-MIL UEIPAC 600-MIL	-40 °C to 85 °C (power dissipation of actual system may require derated max temp.)
Temp (operating) UEIPAC 400-MIL	-40 °C to 70°C (power dissipation of actual system may require derated max temp.)
Temp (storage)	-40 °C to 85 °C
Humidity	0 to 95%, non-condensing
Vibration	MIL-STD-810G plus the IEC specs below
(IEC 60068-2-64)	10–500 Hz, 5*g* (rms), Broad-band random
(IEC 60068-2-6)	10–500 Hz, 5 *g*, Sinusoidal
Shock	MIL-STD-810G plus the IEC specs below
(IEC 60068-2-27)	100 *g*, 3 ms half sine, 18 shocks at 6 orientations; 30 *g*, 11 ms half sine, 18 shocks at 6 orientations
EMI / RFI	Designed to meet MIL-STD-461
Altitude	70,000 feet, maximum
Sealing	Default unit sealed to IP 66 or better. Pressure relief valves support continuous altitude changes of 5000 fpm.
Power Requirements	
Voltage	9 - 36 VDC designed to meet MIL--1275 / 704
Reliability	
MTBF	>130,000 hours

Figure 2-4. UEIPAC-1200-MIL-11 Technical Specifications

2.3 Key Features

The following table is a list of key features of a DNR-MIL system.

- Military/Rugged D38999 connectivity
- 100% COTS solution
- Supported by over 60 standard DNR-series I/O boards
- Dual Independent GigE ports
- Designed for MIL-STD-461/810/1275 compliance
- Extensive built-in system diagnostics
- PowerDNA, UEIPAC, UEISIM, UEIModbus, and UEIOPCUA configurations
- No rotary cooling devices
- Extensive software support including Windows, Linux, QNX, RTX and more
- VxWorks support available in embedded or hosted configurations

2.4 DNR-MIL System Enclosure

The DNR-MIL provides a simple-to-use system that is rugged and water resistant in the field but is easy to program, configure and maintain otherwise.

The DNR-MIL enclosure is a rigid mechanical chassis with complete EMI shielding, meeting FCC and CE compliance. It is designed to be water-resistant, with D38999 connectors providing power and input/output signal lines. Each DNR-MIL system enclosure contains a GigE CPU and two independent Network Interface Control (NIC) boards, one can be used for controlling up to 12 I/O boards mounted in the enclosure and the other for diagnostic functions.

Refer to the figure below for a diagram of the DNR-MIL enclosure:

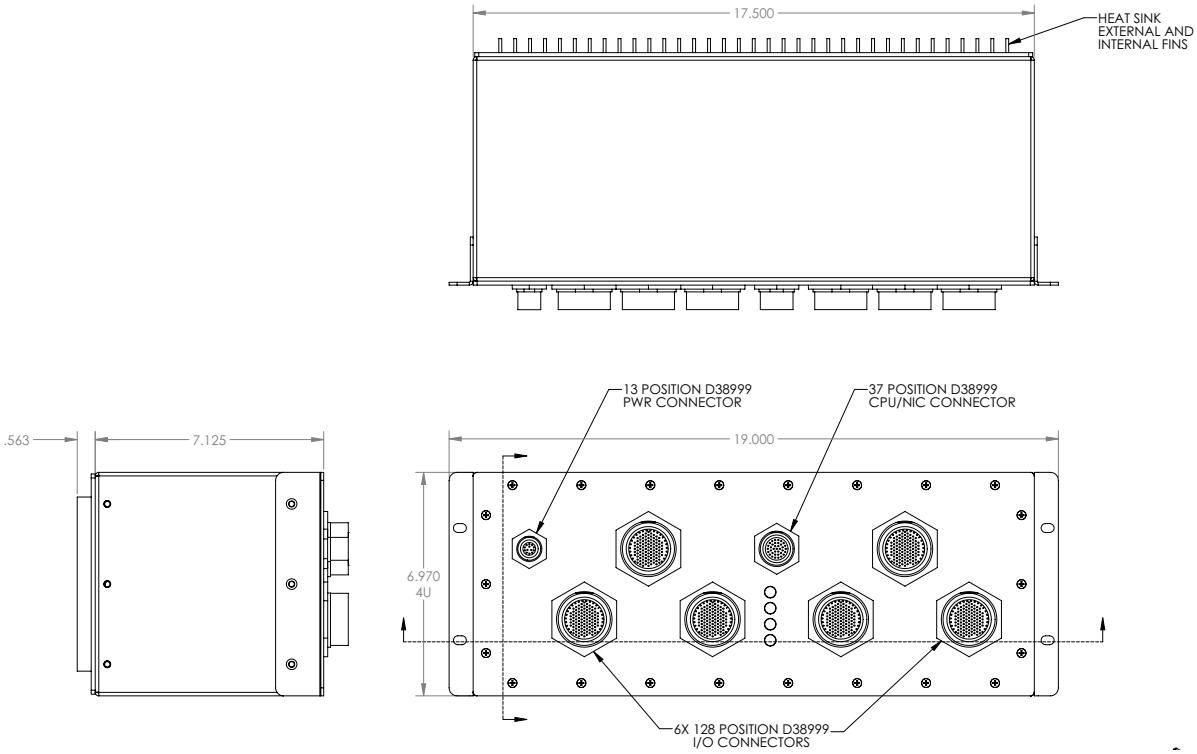


Figure 2-5. DNR-MIL Chassis Diagram

The DNR-MIL enclosure houses the following items:

- One DNR-CPU-x CPU/NIC module with four LED indicators, a D38999 connector providing access to the two independent Ethernet ports, a SYNC port, USB controller/slave ports, and serial debug port.
- One DNR-BP-12M Backplane with temperature sensors and an integrated DC/DC power supply with power conditioning to distribute for 24, 3.3, 2.5, 1.5, 1.2 VDC for the logic/CPU
- Up to 12 DNR I/O boards that are functionally identical to DNA I/O boards but designed to mount within a DNR-MIL enclosure's backplane

Two sensors mounted on the backplane over the Power board and over the CPU board monitor internal temperatures.

2.5 DNR-MIL CPU/NIC Module

The DNR-CPU-x module includes a CPU, a dual 1Gbps Ethernet board, and a associated Network Interface Control (NIC) logic that controls all Ethernet communication functions. This is commonly referred to as the Input Output Module (IOM).

- Refer to Chapter 6, “The DNR-MIL-x CPU ”, for detailed information regarding CPU/NIC board components and LEDs
- Refer to Section 2.8 for the 27-pin D38999 CPU/NIC connector pinout, (e.g., pin mapping for NIC1, NIC2, USBs, serial port, etc.) and for more information about connectors and cabling

2.6 DNR-MIL Backplane & Power

The DNR-BP-12M backplane provides busing for power and data, which are distributed between I/O boards and transferred from and to the CPU/NIC module.

Power flows into the backplane as 9-36 VDC from the PWR connector to the DC-DC power supplies that provide 24 V, 3.3 V, 2.5 V, 1.5 V, 1.2 V to power distribution rails connected to all I/O boards.

The voltage and current, both at the inflow and distributed to each rail, are measured for two purposes: to be read by the user software and to illuminate the Power Good and Failure LEDs on the front panel of the chassis

- Refer to **Table 6-1** in Chapter 6 for LED descriptions
- Refer to Section 2.8 for the 13-pin D38999 power connector pinout and for more information about connectors and cabling

2.6.1 Input Power Protection

The DNR-MIL has reverse polarity, brownout, over-voltage, and over-current protection that cuts power under certain conditions:

- Under-voltage protection when the 9-36 V_{DC} source is below 8.7 V
- Over-voltage protection triggers when 9-36 V_{DC} is above 37.2 V
- Input over-current protection when above 5 A
- Power interruption protection: using a hold-up circuit that will power the DNR-MIL for up to 75 msec at 75 W (longer if using less power)
- Surge protection: depends on the length of the surge; is designed to handle 100 V for at least 100 µsec.
- Transistor-based reverse polarity protection

2.7 DNR-MIL I/O Boards

All standard PowerDNA Cube or RACKtangle I/O boards are also available as DNR-MIL boards.

A DNR-MIL board is functionally identical to its corresponding DNA version. The only difference between them is the physical mounting arrangement. DNR-MIL boards are designed for insertion into the DNR-MIL-x-ENCL enclosure; DNA I/O boards are designed for insertion into a cube chassis.

UEI I/O boards are accessed through either a 37-pin interface or a 62-pin interface, depending on the board. Each 128-pin D38999 I/O board connector on the DNR-MIL chassis accesses up to 2 I/O boards.

Boards installed in the left I/O slot of the pair map to pins 1-62 on the 128-pin D38999. The right I/O slot maps to pins 65-126 on the D38999. Note that for 37-pin based boards, pins 38-62 or pins 102-126 are simply not used.

- Refer to Section 2.8 for the 128-pin D38999 I/O board connector pinout and for more information about connectors and cabling

2.8 Pinouts, Connectors & Cables

All connections to DNR-MIL systems are made through standard, COTS, nickel-plated D38999 connectors.

All D38999 connectors installed in the DNR-MIL are female connectors. Pin numbers are labeled on the face of the connector.

2.8.1 Power Connector Pinout

The pinout for the 13-position D38999 power connector is illustrated in Figure 2-6 and described in Table 2-1:

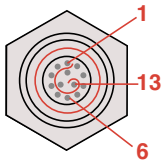


Figure 2-6. Drawing of the 13-pin D38999 Power Connector

Pin(s)	Primary Mode
1-3	Ground Reference
4-6	9-36 VDC Input
7	Reserved
8	IP Selector: 0-3
9	
10	Reserved
11	Reserved
12	Reserved
13	Reserved

Table 2-1 Pinout of the 13-pin D38999 Power Connector

All pins are isolated using opto-couplers or by DC/DC PSU.

DNR-MIL systems provide an option of configuring alternate IP addresses via pin 8 and 9 of the power connector, which select the IP address pair to use (preset by the user in software) by pull-down of the line across pin 10 as follows:

- IP Group #1: 00 (pin 8 and pin 9 floating or pulled up across pin 12)
- IP Group #2: 01 (pin 8 floating and pin 9 pulled-down)
- IP Group #3: 10 (pin 8 pulled-down and pin 9 floating)
- IP Group #4: 11 (pin 8 and pin 9 pulled-down)

Contact support@ueidaq.com for more information regarding the details of this functionality.

The **recommended mating connector** for creating cabling for the PWR connector is the 15-pin Souriau D38999/26FB35PN (male) or equivalent plug.

2.8.2 CPU/NIC Connector Pinout

The pinout for the 37-position D38999 CPU/NIC connector is illustrated in Figure 2-7 and described in Table 2-2:

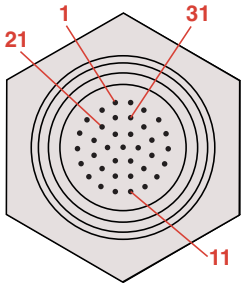


Figure 2-7. Drawing of the 37-pin D38999 LAN/CPU Connector

Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation
1	LAN0 TX+ / DA+	14	USB2 P+	26	Misc Out
2	LAN0 RX+ / DB+	15	USB2 P-	27	USB1 P-
3	LAN0 nc / DC-	16	USB2 D+	28	USB1 D-
4	LAN0 nc / DD+	17	USB2 D-	29	Sync Clock Out
5	Shield	18	LAN0 TX- / DA-	30	Sync Trig Out
6	LAN1 TX+ / DA+	19	LAN0 nc / DC+	31	RS232 TX
7	LAN1 RX+ / DB+	20	LAN0 RX- / DB-	32	RS232 RX
8	LAN1 nc / DC-	21	LAN0 nc / DD-	33	RS232 GND
9	LAN1 nc / DD+	22	LAN1 TX- / DA-	34	Sync Clock In
10	Shield	23	LAN1 nc / DC+	35	Sync Trig In
11	Misc In	24	LAN1 RX- / DB-	36	Sync +5V
12	USB1 P+	25	LAN1 nc / DD-	37	Sync Gnd
13	USB1 D+				

Table 2-2 Pinout of the 37-pin CPU / LAN Connector

The **recommended mating connector** for creating custom cabling is the 37-pin Souriau D38999/26WD35PN (male) nickel plug or equivalent.

2.8.3 I/O Board Pinout

Each pair of DNR-MIL I/O boards share a D38999 connector, shown below. The left board of the pair uses pins 1-64; the right board uses pins 65-128.

The pinout for the right board of the 128-pin D38999 I/O board connector is illustrated in Figure 2-6. (The left board maps to pins 1 to 64).

Pin numbers are printed onto the connector.

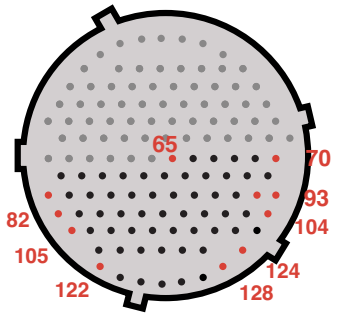


Figure 2-8. Drawing of the 128-pin D38999 I/O Board Connector

UEI I/O boards are accessed through a 37-pin interface or a 62-pin interface, depending on the board.

Table 2-3 describes how each 37-pin and/or 62-pin I/O board pair maps to the D38999 128-pin connector:

I/O Board Configuration		Left I/O Board	Right I/O Board
Left	**Right**	**D38999 128-pin Connector Pin No.**	**D38999 128-pin Connector Pin No.**
37-pin	37-pin	1-37	65-101
37-pin	62-pin	1-37	65-126
62-pin	37-pin	1-62	65-101
62-pin	62-pin	1-62	65-126

Table 2-3 Pin Mapping of the 128-pin D38999 I/O Board Connector

For detailed electrical specifications and user instructions for each DNR-MIL I/O board, refer to the datasheets and user manuals for the specific I/O board.

Datasheets and user manuals are available on the UEI website at www.ueidaq.com.

NOTE: I/O board datasheets and manuals show 37or 62-pin pinouts:

- pinouts for 37-pin boards correlate to pins 1-37 if a board is on the left of the connector and/or 65-101 on the right
- pinouts for 62-pin boards correlate to pins 1-62 if a board is on the left of the connector and/or 65-126 on the right
- Any remaining pins are left unconnected, (e.g., pin 63, 64, 127, 128, etc.)

The **recommended mating connector** for creating custom cabling is the 128-pin Souriau D38999/26FJ35PN (male) nickel plug or equivalent.

2.8.4 Optional Cables

For customers who don't wish to make their own cables, UEI offers the following cables, organized by DNR-MIL port:

Port	Cable Name	Cable Length	Connectors	
			D38999 Connector (Chassis side):	To:
LAN/CPU/USB/SYNC	DNA-CBL-LAN-06	6 ft	D38999/26WD35PN 37-pin male	2 RJ-45 (LANs), DB-9 female (COM), 2 4-pin USBs, 1 RJ-50 (SYNC)
Power	DNA-CBL-1315-03	3 ft	D38999/26FB35PN 13-pin male	a DB-15 male
I/O Boards	DNA-CBL-12862-5	5 ft	D38999/26FJ35PN 128-pin male	2x DB-62 male
I/O Boards	DNA-CBL-12837-3	3 ft	D38999/26FJ35PN 128-pin male	2x DB-37 female
I/O Boards	DNA-CBL-12837-5	5 ft	D38999/26FJ35PN 128-pin male	2x DB-37 female
I/O Boards	DNA-CBL-6237M-3	3 ft	D38999/26FJ35PN 128-pin male	DB-62 male, DB-37 female (62-pin I/O board in left slot, 37-pin in right)
I/O Boards	DNA-CBL-62M-03	3 ft	D38999/26FJ35PN 128-pin male	1x DB-62 male (62-pin I/O board in left slot, no board in right)
I/O Boards	DNA-CBL-37M-03	3 ft	D38999/26FJ35PN 128-pin male	1x DB-37 female (37-pin I/O board in left slot, no board in right)

Table 2-4 Cables

Chapter 3 The DNR-MIL-6 RACKtangle System

This chapter provides the following information about the DNR-MIL-6 Series RACKtangle™ system:

- The DNR-MIL-6 System (Section 3.1)
- Specifications (Section 3.2)
- Key Features (Section 3.3)
- DNR-MIL-6 System Enclosure (Section 3.4)
- DNR-MIL-6 CPU/NIC Module (Section 3.5)
- DNR-MIL-6 Backplane & Power (Section 3.6)
- DNR-MIL-6 I/O Boards (Section 3.7)
- Pinouts, Connectors & Cables (Section 3.8)

NOTE: Information in this chapter applies to all DNR-MIL-6 series RACKtangle systems unless otherwise noted. This includes UEIPAC-600-MIL, which shares the same hardware as DNR-MIL-6. For a list of product versions, refer to Section 1.2 on page 3.

3.1 The DNR-MIL-6 System

The UEI DNR-MIL-6 RACKtangle™ system is a compact, rugged and highly integrated Ethernet I/O data acquisition platform. The DNR-MIL-6 series is a military version of the PowerDNA Ethernet-based Data Acquisition System that provides a rugged chassis for military applications that require up to six I/O boards per chassis. All standard DNA I/O boards are also available in DNR versions for use in DNR-MIL-6 systems.

Figure 3-1. Typical DNR-MIL-6 RACKtangle System

The PowerDNA-based RACKtangle system consists of the following boards:

- DNR-MIL-6-ENCL rack mounted enclosure
- DNR-CPU-x module (includes CPU and 1-GB Ethernet 1000 Base-T Network Interface Board)

To configure a complete data acquisition system, install up to 6 DNR I/O boards into each DNR-MIL-6 rack enclosure, which may be specified in any combination of the following types:

- DNR-AI-series for Analog Inputs (incl. Strain, TC, RTD, ICP, LVDT, ...)
- DNR-AO-series for Analog Outputs (voltage, current, strain gage, ...)
- DNR-DIO-series for Digital Inputs/Outputs and Relays
- DNR-CT-series for Counters/Timers/PWM/Quadrature, IRIG
- Serial & HDLC (DNR-SL), CAN bus, Synchronous Serial Interface (SSI)
- Avionics for ARINC 429, DNR-MIL-1553, and more

Refer to www.ueidaq.com for a description of each I/O board and a catalog of the most recent set of boards. The website also lists PowerDNA™ accessories available for use in a DNR-MIL-6 system.

NOTE: Though it is possible to replace various boards within the DNR-MIL-6, it is recommended that the modification be done and tested by UEI.

The DNR-MIL-6 system can be configured in the following modes of operation:

- PowerDNA Mode - Host-controlled Operation
- UEIPAC - Programmable Automation Controller
- UEISIM - Simulink / Simulink Coder Target
- UEIModbus - Modbus TCP-based Controller
- UEIOPCUA - OPC-UA Server, accessed by any OPC-UA client

3.2 Specifications

Figure 3-2 lists the specifications of the DNR-MIL-6 system for PowerDNA hosted deployments options -00, -02, and -03.

Computer Interface	**DNR-MIL-6-00/02/03**
Primary Ethernet Port	10/100/1000Base-T, 38999 connector
Diagnostic Port	10/100/1000Base-T, 38999 connector
Config/Serial Port	RS-232, 38999 connector
Sync	1. IEEE-1588/PTP 2. DNR-SYNC-1G series cables and boards provide both clock and trigger sync signals. 3.. DNR-IRIG-650 board provides IRIG and GPS time synchronization
I/O Board Support	
Series supported	All DNR-series boards
Processor/system	
CPU	Freescale 8347, 400 MHz, 32-bit
Memory (RAM)	256 MB
Memory (Flash)	32 MB
Host Communications	
Distance from host	100 meters max, CAT5/6 cable
Ethernet data transfer rate	20 megabyte per second
Analog data transfer rate	>6 megasample per second. Capable of sustained transfer in any RACKtangle configuration
DMAP/VMAP real-time I/O mode	update >1,000 I/O channels at 4 kHz, guaranteed
Physical Dimensions / Weight	
6 I/O slots	10.6 ”x 7.0” x 6.4”/ 16 lbs. incl I/O boards
Environmental*	
Electrical Isolation	350 Vrms
Temp (operating)	-40 °C to 70 °C
Temp (storage)	-40 °C to 85 °C
Humidity	0 to 95%, non-condensing
Vibration	MIL-STD-810G plus the IEC specs below
(IEC 60068-2-64)	10–500 Hz, 5 *g* (rms), Broad-band random
(IEC 60068-2-6)	10–500 Hz, 5 *g*, Sinusoidal
Shock	MIL-STD-810G plus the IEC stds below
(IEC 60068-2-27)	100 *g*, 3 ms half sine, 18 shocks at 6 orientations; 30 *g*, 11 ms half sine, 18 shocks at 6 orientations
Altitude	70,000 feet, maximum
EMI / RFI	Designed to meet MIL-STD-461
Power Requirements	
Voltage	9 - 36 VDC (115/220 VAC adaptor available)
Power	12 Watts (not including I/O boards)
Power Quality requirement	Designed to meet MIL-STD-1275
Reliability	
MTBF	100,000 hours

Figure 3-2. DNR-MIL-6-00/02/03 Technical Specifications (PowerDNA Mode)

Figure 3-3 lists the specifications of the DNR-MIL-6 system for stand-alone deployments options -00, -02, and -03. UEIPAC specifications also apply to UEISIM, UEIModbus, and UEIOPCUA configurations.

Computer Interface	**UEIPAC 600-MIL-00/02/03**
Primary Ethernet Port	10/100/1000Base-T, 38999 connector
Diagnostic Port*	10/100/1000Base-T, 38999 connector *Alternatively can be teamed/bonded with primary port.
Config/Serial Port	RS-232, 38999 connector
USB Port	USB 2.0 fully supported
Synchronization Options	1. DNR-SYNC-1G series cables and boards provide both clock and trigger sync signals. 2. DNR-IRIG-650 board provides IRIG and GPS time synchronization 3. PTP client provides software implementation of IEEE-1588
I/O Board Support	
Series supported	All DNR-series boards
Software / Operating System	
Embedded OS	Linux, kernel 4.4.x (VxWorks Available)
Real-time support	Xenomai, Linux RT or VxWorks support
Dev Language	C/C++, Eclipse IDE support,
Dev Environments	Linux PC or Cygwin Windows environment
EPICS CAS interface	Yes
SNMP Library	Yes
OS royalties	none
Processor/system	
CPU	Freescale 8347, 400 MHz, 32-bit
Memory	256 MB (128 MB avail for application SW)
FLASH memory	32 MB (16 MB available for user apps)
Solid State Hard Drive	up to 64 GByte
SD card interface	SD cards up to 32 GB
USB drive interface	Standard USB 2.0 port
Physical Dimensions	
6 I/O slots	10.6 ″ x 7.0″ x 6.4″/ 16 lbs. incl I/O boards
Environmental	
Electrical Isolation	350 Vrms
Temp (operating)	-40 °C to 70 °C
Temp (storage)	-40 °C to 85 °C
Humidity	0 to 95%, non-condensing
Vibration	MIL-STD-810G plus the IEC specs below
(IEC 60068-2-64)	10–500 Hz, 5*g* (rms), Broad-band random
(IEC 60068-2-6)	10–500 Hz, 5 *g*, Sinusoidal
Shock	MIL-STD-810G plus the IEC stds below
(IEC 60068-2-27)	100 *g*, 3 ms half sine, 18 shocks at 6 orientations; 30 *g*, 11 ms half sine, 18 shocks at 6 orientations
Altitude	70,000 feet, maximum
EMI / RFI	Designed to meet MIL-STD-461
Power Requirements	
Voltage	9 - 36 VDC (115/220 VAC adaptor available)
Power	12 Watts (not including I/O boards)
Power Quality requirement	Designed to meet MIL-STD-1275
Reliability	
MTBF	100,000 hours

Figure 3-3. UEIPAC-600-MIL-00/02/03 Technical Specifications

Figure 3-3 lists the specifications of the DNR-MIL-6 system for stand-alone deployments option -11. UEIPAC specifications also apply to UEISIM, UEIModbus, and UEIOPCUA configurations.

Computer Interface	**UEIPAC 600-MIL-11**
Primary Ethernet Port	10/100/1000Base-T, 38999 connector
Diagnostic Port	10/100/1000Base-T, 38999 connector
M2 PCIe slot (internal)	1 slot, 22 or 30 width, 42, 60 or 80 length, B key
Net Teaming/bonding	Supported in both Linux and VxWorks deployments
Config/Serial Port	RS-232 port on LAN/COM 38999
USB Port	USB 2.0 fully supported
Synch Options	Sync input/output port or IEEE-1588
I/O Board Support	
Series supported	All DNR/DNA-series boards as appropriate
Software / Operating System	
Embedded OS	Linux, kernel 4.9.x or VxWorks 7.x
Real-time support	4.9.88 kernel based Real-time Linux, VxWorks is a real-time OS
EPICS CAS interface	Yes (Linux version)
SNMP Library	Yes
Processor/system	
CPU	SoloX / i.MX6 series ARM processor Cortex A9 core @ 1Ghz
Memory	1 Gbyte RAM
FLASH memory	8 Gbyte
Solid-State Hard Drive	Optional 8 or 16 GB drives available
µSD card interface	µSD cards up to 128 GB
USB drive interface	Standard USB 2.0 port
Physical Dimensions	
6 I/O slots	10.6" x 7.0" x 6.4", 16 lbs incl. I/O boards
Environmental	
Temp (operating) UEIPAC 1200-MIL UEIPAC 600-MIL	-40 °C to 85 °C (power dissipation of actual system may require derated max temp.)
Temp (operating) UEIPAC 400-MIL	-40 °C to 70°C (power dissipation of actual system may require derated max temp.)
Temp (storage)	-40 °C to 85 °C
Humidity	0 to 95%, non-condensing
Vibration	MIL-STD-810G plus the IEC specs below
(IEC 60068-2-64)	10–500 Hz, 5*g* (rms), Broad-band random
(IEC 60068-2-6)	10–500 Hz, 5 *g*, Sinusoidal
Shock	MIL-STD-810G plus the IEC specs below
(IEC 60068-2-27)	100 *g*, 3 ms half sine, 18 shocks at 6 orientations; 30 *g*, 11 ms half sine, 18 shocks at 6 orientations
EMI / RFI	Designed to meet MIL-STD-461
Altitude	70,000 feet, maximum
Sealing	Default unit sealed to IP 66 or better. Pressure relief valves support continuous altitude changes of 5000 fpm.
Power Requirements	
Voltage	9 - 36 VDC designed to meet MIL--1275 / 704
Reliability	
MTBF	>130,000 hours

Figure 3-4. UEIPAC-600-MIL-11 Technical Specifications

3.3 Key Features

The following table is a list of key features of a DNR-MIL-6 system.

- Military/Rugged D38999 connectivity
- 100% COTS solution
- Supported by over 60 standard DNR series I/O boards
- Dual GigE ports (control and diagnostic)
- Designed for MIL-STD-461/810/1275 compliance
- Extensive built-in system diagnostics
- PowerDNA, UEIPAC, UEISIM, UEIModbus, and UEIOPCUA configurations
- No rotary cooling devices
- Extensive software support including Windows, Linux, QNX, RTX and more
- VxWorks support available in embedded or hosted configurations

3.4 DNR-MIL-6 System Enclosure

The DNR-MIL-6 provides a simple-to-use system that is rugged and water resistant in the field but is easy to program, configure and maintain otherwise.

The DNR-MIL-6 enclosure is a rigid mechanical chassis with complete EMI shielding, meeting FCC and CE compliance. It is designed to be water-resistant, with D38999 connectors providing power and input/output signal lines. Each DNR-MIL-6 system enclosure contains a GigE CPU and two independent Network Interface Control (NIC) boards, one can be used for controlling up to 6 I/O boards mounted in the enclosure and the other for diagnostic functions.

Refer to the figure below for a diagram of the DNR-MIL-6 enclosure:

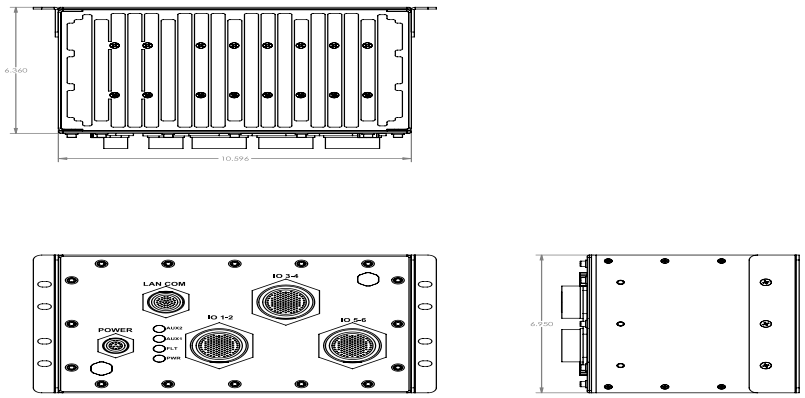


Figure 3-5. DNR-MIL-6 Chassis Diagram

The DNR-MIL-6 enclosure houses the following items:

- One DNR-CPU-x CPU/NIC module with four LED indicators, a D38999 connector providing access to the two independent Ethernet ports, a SYNC port, USB controller/slave ports (future use), and serial debug port
- One DNR-BP-6M Backplane with temperature sensors and an integrated DC/DC power supply with power conditioning to distribute for 24, 3.3, 2.5, 1.5, 1.2 VDC for the logic/CPU
- Up to 6 DNR I/O boards that are functionally identical to DNA I/O boards but designed to mount within a DNR-MIL-6 enclosure's backplane

Two sensors mounted on the backplane over the Power board and over the CPU board monitor internal temperatures.

3.5 DNR-MIL-6 CPU/NIC Module

The DNR-CPU-x module includes a CPU, a dual 1Gbps Ethernet board, and a associated Network Interface Control (NIC) logic that controls all Ethernet communication functions. This is commonly referred to as the Input Output Module (IOM).

- Refer to Chapter 6, “The DNR-MIL-x CPU ”, for detailed information regarding CPU/NIC board components
- Refer to Section 3.8 for the 27-pin D38999 CPU/NIC connector pinout, (e.g., pin mapping for NIC1, NIC2, USBs, serial port, etc.) and for more information about connectors and cabling

3.6 DNR-MIL-6 Backplane & Power

The DNR-BP-6M backplane provides busing for power and data, which are distributed between I/O boards and transferred from and to the CPU/NIC module.

Power flows into the backplane as 9-36 VDC from the PWR connector to the DC-DC power supplies that provide 24 V, 3.3 V, 2.5 V, 1.5 V, 1.2 V to power distribution rails connected to all I/O boards.

The voltage and current, both at the inflow and distributed to each rail, are measured for two purposes: to be read by the user software and to illuminate the Power Good and Failure LEDs on the front panel of the chassis

- Refer to **Table 6-1** in Chapter 6 for LED descriptions.
- Refer to Section 3.8 for the 13-pin D38999 power connector pinout and for more information about connectors and cabling.

3.6.1 Input Power Protection

The DNR-MIL-6 has reverse polarity, brownout, over-voltage, and over-current protection that cuts power under certain conditions:

- Under-voltage protection when the 9-36 V_{DC} source is below 8.7 V
- Over-voltage protection triggers when 9-36 V_{DC} is above 37.2 V
- Input over-current protection when above 5 A
- Power interruption protection: using a hold-up circuit that will power the DNR-MIL for up to 75 msec at 75 W (longer if using less power)
- Surge protection: depends on the length of the surge; is designed to handle 100 V for at least 100 µsec
- Transistor-based reverse polarity protection

3.7 DNR-MIL-6 I/O Boards

All standard PowerDNA Cube or RACKtangle I/O boards are also available as DNR-MIL.

NOTE: DNR-MIL I/O boards are identical between DNR-MIL and DNR-MIL-6 and are simply referred to as DNR-MIL.

A DNR-MIL board is functionally identical to its corresponding DNA version. The only difference between them is the physical mounting arrangement. DNR-MIL boards are designed for insertion into the DNR-MIL-x-ENCL enclosure; DNA I/O boards are designed for insertion into a cube chassis.

UEI I/O boards are accessed through either a 37-pin interface or a 62-pin interface, depending on the board. Each 128-pin D38999 I/O board connector on the DNR-MIL-6 chassis accesses up to 2 I/O boards.

Boards installed in the left I/O slot of the pair map to pins 1-62 on the 128-pin D38999. The right I/O slot maps to pins 65-126 on the D38999. Note that for 37-pin based boards, pins 38-62 or pins 102-126 are simply not used.

- Refer to Section 3.8 for the 128-pin D38999 I/O board connector pinout and for more information about connectors and cabling

3.8 Pinouts, Connectors & Cables

All connections to DNR-MIL-6 systems are made through standard, COTS, nickel- plated D38999 connectors.

All D38999 connectors installed in the DNR-MIL-6 are female connectors. Pin numbers are labeled on the face of the connector.

3.8.1 Power Connector Pinout

The pinout for the 13-position D38999 power connector is illustrated in Figure 3-6 and described in Table 3-1:

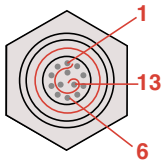


Figure 3-6. Drawing of the 13-pin D38999 Power Connector

Pin(s)	Primary Mode	Secondary Mode
1-3	Ground Reference	
4-6	9-36 VDC Input	
7	Reserved, do not connect	SYNC-IN 2: RESET-IN
8	IP Selector: 0-3	SYNC-IN 0: CLK-IN
9		SYNC-IN 1: TRIGGER-IN
10	Reserved, do not connect	SYNC-GND
11	Reserved, do not connect	SYNC-OUT 1: CLK-OUT
12	Reserved, do not connect	SYNC-+5V
13	Reserved, do not connect	SYNC-OUT 0: TRIG-OUT

Table 3-1 Pinout of the 13-pin D38999 Power Connector

Pins 7-13 of the PWR connector can be configured in one of two software-selectable modes. All pins are isolated using opto-couplers or by DC/DC PSU. In the primary mode, pins 8 and 9 select the IP address pair to use (preset by the user in software) by pull-down of the line across pin 10 as follows:

- IP Group #1: 00 (pin 8 and pin 9 floating or pulled up across pin 12)
- IP Group #2: 01 (pin 8 floating and pin 9 pulled-down)
- IP Group #3: 10 (pin 8 pulled-down and pin 9 floating)
- IP Group #4: 11 (pin 8 and pin 9 pulled-down)

In the secondary mode, pins 7-13 provide redundancy for the SYNC and RESET lines.

The **recommended mating connector** for creating cabling for the PWR connector is the 15-pin Souriau D38999/26FB35PN or equivalent plug.

3.8.2 CPU/NIC Connector Pinout

The pinout for the 37-position D38999 CPU/NIC connector is illustrated in Figure 3-7 and described in Table 3-2:

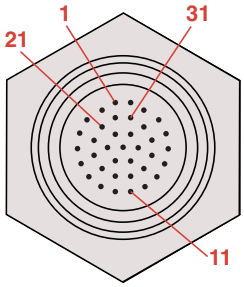


Figure 3-7. Drawing of the 37-pin D38999 LAN/CPU Connector

Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation
1	LAN0 TX+ / DA+	14	USB2 P+	26	Misc Out
2	LAN0 RX+ / DB+	15	USB2 P-	27	USB1 P-
3	LAN0 nc / DC-	16	USB2 D+	28	USB1 D-
4	LAN0 nc / DD+	17	USB2 D-	29	Sync Clock Out
5	Shield	18	LAN0 TX- / DA-	30	Sync Trig Out
6	LAN1 TX+ / DA+	19	LAN0 nc / DC+	31	RS232 TX
7	LAN1 RX+ / DB+	20	LAN0 RX- / DB-	32	RS232 RX
8	LAN1 nc / DC-	21	LAN0 nc / DD-	33	RS232 GND
9	LAN1 nc / DD+	22	LAN1 TX- / DA-	34	Sync Clock In
10	Shield	23	LAN1 nc / DC+	35	Sync Trig In
11	Misc In	24	LAN1 RX- / DB-	36	Sync +5V
12	USB1 P+	25	LAN1 nc / DD-	37	Sync Gnd
13	USB1 D+				

Table 3-2 Pinout for the 37-pin CPU / LAN Connector

The **recommended mating connector** for creating custom cabling is the 37-pin Souriau D38999/26WD35PN nickel plug or equivalent.

3.8.3 I/O Board Pinout

Each pair of DNR-MIL-6 I/O boards share a D38999 connector, shown below. The left-most board of the pair uses pins 1-64; the right-most board uses pins 65-128.

The pinout for the right board of the 128-pin D38999 I/O board connector is illustrated in Figure 3-6. (The left board maps to pins 1 to 64).

Pin numbers are printed onto the connector.

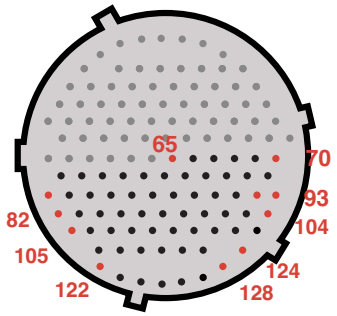


Figure 3-8. Drawing of the 128-pin D38999 I/O Board Connector

UEI I/O boards are accessed through a 37-pin interface or a 62-pin interface, depending on the board.

Table 3-1 describes how each 37-pin and/or 62-pin I/O board pair maps to the D38999 128-pin connector:

I/O Board Configuration		Left I/O Board	Right I/O Board
Left	**Right**	**D38999 128-pin Connector Pin No.**	**D38999 128-pin Connector Pin No.**
37-pin	37-pin	1-37	65-101
37-pin	62-pin	1-37	65-126
62-pin	37-pin	1-62	65-101
62-pin	62-pin	1-62	65-126

Table 3-3 Pin Mapping for the 128-pin D38999 I/O Board Connector

For detailed electrical specifications and user instructions for each DNR-MIL-6 I/O board, refer to the datasheets and user manuals for the specific I/O board.

Datasheets and user manuals are available on the UEI website at www.ueidaq.com.

NOTE: I/O board datasheets and manuals show 37 or 62-pin pinouts:

- pinouts for 37-pin boards correlate to pins 1-37 if a board is on the left of the connector and/or 65-101 on the right
- pinouts for 62-pin boards correlate to pins 1-62 if a board is on the left of the connector and/or 65-126 on the right
- Any remaining pins are left unconnected, (e.g., pin 63, 64, 127, 128, etc.)

The **recommended mating connector** for creating custom cabling is the 128-pin Souriau D38999/26FJ35PN nickel plug or equivalent.

3.8.4 Optional Cables

For customers who don't wish to make their own cables, UEI offers the following cables, organized by each DNR-MIL-6 port:

Port	Cable Name	Cable Length	Connectors	
			D38999 Connector (Chassis side):	To:
LAN/CPU/USB/SYNC	DNA-CBL-LAN-06	6 ft	D38999/26WD35PN 37-pin male	2 RJ-45 (LANs), DB-9 female (COM), 2 4-pin USBs, 1 RJ-45 (SYNC)
Power	DNA-CBL-1315-03	3 ft	D38999/26FB35PN 13-pin male	a DB-15 male
I/O Boards	DNA-CBL-12862-5	5 ft	D38999/26FJ35PN 128-pin male	2x DB-62 male
I/O Boards	DNA-CBL-12837-3	3 ft	D38999/26FJ35PN 128-pin male	2x DB-37 female
I/O Boards	DNA-CBL-12837-5	5 ft	D38999/26FJ35PN 128-pin male	2x DB-37 female
I/O Boards	DNA-CBL-6237M-3	3 ft	D38999/26FJ35PN 128-pin male	DB-62 male, DB-37 female (62-pin I/O board in left slot, 37-pin in right)
I/O Boards	DNA-CBL-62M-03	3 ft	D38999/26FJ35PN 128-pin male	1x DB-62 male (62-pin I/O board in left slot, no board in right)
I/O Boards	DNA-CBL-37M-03	3 ft	D38999/26FJ35PN 128-pin male	1x DB-37 female (37-pin I/O board in left slot, no board in right)

Table 3-4 Cables

Chapter 4 Installation and Configuration

This chapter provides the following installation and configuration information for the DNR-MIL-x Series RACKtangle™ systems:

- Initial Installation Guide (Section 4.1)
- Initial Boot-up (Section 4.2)
- IP Address Overview & Update Procedures (Section 4.3)
- Improving Network Performance (Section 4.4)
- Updating Firmware & PowerDNA Explorer Quick-Start (Section 4.5)
  - Getting Started with PowerDNA Explorer (Section 4.5.1)
  - Firmware Update Overview (Section 4.5.2)
  - Firmware Update Instructions (Section 4.5.3)
- Peripheral Terminal Panel Wiring (Section 4.6)
- Repairing (and Upgrading) Your DNR-MIL-x System (Section 4.7)
- Configuring a NIC Port for Diagnostic Mode (Section 4.8)

NOTE: Information in this chapter applies to all hosted versions of the DNR-MIL-x series RACKtangle systems unless otherwise noted. For a list of product versions available for the DNR-MIL-x series, refer to Section 1.2 on page 3.

4.1 Initial Installation Guide

The following section describes the procedure recommended for performing an initial hardware and software setup when you first receive a DNR-MIL-x system.

Installation consists of:

- DNR-MIL-x hardware setup
- Software package installation
- Configuration

NOTE: Throughout this chapter, several figures display graphical representations of PowerDNA-based systems. Note that information about the display is identical for the DNR-MIL-x.

4.1.1 Inspect Package

With a standard DNR-MIL-x system, the following items are included with your shipment:

- A DNR-MIL-x system, pre-installed with a DNR-CPU-1GBM CPU and your selection of I/O boards, ready to run when powered on
- CD or USB with support software

NOTE: Depending on your application, you may also need to provide the following optional items not normally included with your order:

- 37-pin DNA-CBL-LAN-06 cable for the CPU/NIC/COM/USB/SYNC interface between the host PC and DNR-MIL-x
- 13-pin DNA-CBL-1315-03 cable for LAN_ID/24VDC power
- 128-pin D38999 cabling:
  - DNA-CBL-12862-5: 5 ft male 128-pin D38999 to 2x DB-62M
  - DNA-CBL-12837-5: 5 ft male 128-pin D38999 to 2x DB-37F
  - DNA-CBL-6237M-3: 3 ft male 128-pin D38999 to DB-37F & DB-62M
  - DNA-CBL-62M-03: 3 ft male 128-pin D38999 to 1x DB-62M
  - DNA-CBL-37M-03: 3 ft male 128-pin D38999 to 1x DB-37F

NOTE: Please refer to Section 2.8 on page 14 for more information about DNR-MIL-x connectors and cabling.

4.1.2 Install Software

This section describes how to load the PowerDNA software suite onto a Windows- or Linux-based computer (i.e. host PC) and run some initial tests.

The latest PowerDNA-based software is online at www.ueidaq.com/download; a copy is also on the provided CD or USB.

A. Software Install: Windows

The PowerDNA CD/USB provides one installer that contains the UEI low-level driver and UEIDAQ Framework.

The installer automatically searches for third-party IDE and testing suites, and adds them as tools to the suites found. Be sure to install third-party applications (such as LabVIEW, MATLAB, or Microsoft Visual Studio) ***before*** installing the PowerDNA Software Suite to allow the installer to auto-detect them.

To install the PowerDNA Software Suite, do the following:

STEP 1: Run Setup as an Administrator

a. Insert the provided CD/USB. Windows should automatically start the PowerDNA Setup program. An installer with the UEI logo should display, and then the PowerDNA Welcome screen. If neither appear, run setup.exe from the CD drive:

Start >> Run >> d:\setup.exe >> OK.

If you downloaded the most recent executable from www.ueidaq.com, double-click on the filename to run the executable.

b. Choose the PowerDNA Software Suite option.

c. Unless you are an expert user and have specific requirements, select *Typical Installation* and accept the default configuration.

NOTE: The Software Suite installs plugins/examples for any data acquisition programs detected at install-time, as well as stand-alone diagnostic tools. If a 32-bit Java VM is not detected, then Java JRE will automatically be installed for the PowerDNA Explorer diagnostic tool.

As an alternative, use the *Custom* option to display and ensure that all of the necessary packages are installed.

- Companion Documentation:
  Quick Start Guide, Configuration and Core,
  I/O Board Manuals, Low-Level Programming Guide
- SDK: includes/lib for C/Java, examples, and JRE;
  (The SDK is not the UeiDaq Framework)
- PowerDNA Apps: PowerDNA Explorer, MTTTY
- PowerDNA Components (incl. DLL files)
- PowerDNA Firmware

d. Click **Next** to continue through the dialogs.

e. Click **Finish** to complete the installation.

STEP 2: Restart the computer.

The Software Suite installs the minimum set of tools needed in later steps: MTTTY, PowerDNA Explorer, and the low-level driver.

Windows installations include the UEIDAQ Framework, which provides the structure for developing applications under C/C++, C#, VB.NET, ActiveX, MATLAB, LabVIEW, LabWindows/CVI, OPC, and more.

NOTE: Because the installation process modifies your Windows registry, you should always install or uninstall the software using the appropriate utilities. Never remove PowerDNA software from your PC directly by deleting individual files; always use the Windows Control Panel Add/Remove Programs utility.

B. Software Install: Linux

The PowerDNA_*.tgz file in the CD/USB Linux folder contains the software package for Linux. To extract the file to a local directory:

```
tar -xzvf /path/to/powerdna*.tgz
```

Follow the instructions in the `readme.txt` file included in the tar file.

4.2 Initial Boot-up

Perform an initial boot up in preparation for configuring the network using the following procedure:

STEP 1: Familiarize yourself with the layout of your DNR-MIL-x system front-panel. Note that all connections are made on the front of the unit.

STEP 2: Optionally, set up communication over the serial port by attaching the serial cable between the host PC and the DNR-MIL-x connector (refer to Chapter 2 for connector location and pinout).
Note that a generic serial cable should not be used because signal pinouts differ and will cause the unit to malfunction.

a. Run a terminal-emulation program (e.g. MTTTY) on the PC. Any terminal-emulation program, except HyperTerminal, may be used (MTTTY, Minicom, TeraTerm, etc.).

b. Verify that COM parameters are set to 57600 baud, 8 bits, no parity, 1 stop bit.

c. Click **Connect** in MTTTY, or use the commands on one of the other terminal-emulation programs to establish communication with the DNR-MIL-x system.

STEP 3: Connect power to the system.

STEP 4: As soon as the system powers up, it runs through self-diagnostic mode and generates output on the terminal program, if connected.
A typical readout is shown in **Figure 4-1**:

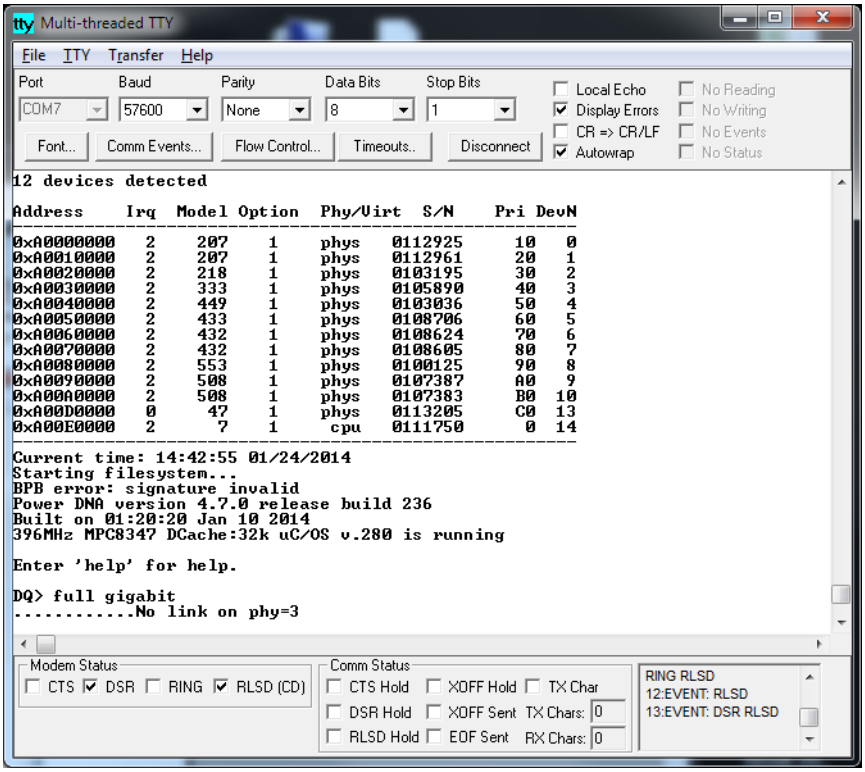


Figure 4-1. Typical MTTTY Screen

The boot process displays the model, serial number, and slot positions of boards in the rack enclosure.

The serial connection can be used to display information on system configuration by typing `show` in the terminal window and pressing the Return key, as shown below:

```
DQ> show
        name: "IOM-111111"
       model: 3212
      serial: 0111111
        fwct: 1.2.0.0
         mac: 00:0C:94:01:B4:86
         srv: 192.168.100.2
          ip: 192.168.100.20
     gateway: 192.168.100.1
     netmask: 255.255.255.0
        mac2: 00:0C:94:F1:B4:86
        srv2: 192.168.100.102
         ip2: 192.168.100.120
    gateway2: 192.168.100.1
    netmask2: 255.255.255.0
         udp: 6334
     license: "b994efd6"
    Manufactured 12/1/2013
    Calibrated 12/12/2013
DQ>
```

All parameters can be changed, including the IP address, gateway, and subnet mask (netmask) configured for this system. Refer to Chapter 7 for more information about changing parameters via the serial port using the `set` command.

4.3 IP Address Overview & Update Procedures

The DNR-MIL-x ships with preconfigured factory default IP addresses for NIC1 and NIC2, which are stored in nonvolatile memory (usually 192.168.100.2 for NIC1 and 192.168.100.102 for NIC2). These are static IP addresses.

The DNR-MIL-x (hosted deployment) does not support dynamically assigned IP addresses, only static. Stand-alone deployments, such as the UEIPAC-x-MIL, include a built-in DHCP client and can retrieve IP addresses from a network DHCP server. For more information about configuring standalone deployments, refer to the respective user manuals.

The following subsections provide more information about changing the default IP addresses in DNR-MIL-x systems.

4.3.1 When Should You Change the IP Address?

You can change the IP address when you connect a DNR-MIL-x system to a local area network (LAN).

When connecting your DNR-MIL-x to your host PC, generally, a network cable between the host PC's network adapter and DNR-MIL-x chassis is a standard configuration that ensures that there are no problems caused by outside interference or added latency.

In most situations a dedicated LAN using a Gigabit switch is recommended. Note the following considerations when connecting your rack to the general-purpose (company domain) network:

- high sampling rate measurements consume a lot of the available bandwidth
- some samples or commands can be significantly delayed or entirely dropped (lost) due to network congestion, collisions, or a slow switch
- the system can be accessed by multiple parties on the LAN
- multiple RACKs/systems operate (and interact) on the same network

See "Improving Network Performance" on page 39 for more information.

4.3.2 How to Change the Primary IP Address (NIC1)

Instructions for changing the IP address are provided in this section.You can use PowerDNA Explorer (a UEI-developed GUI application) or a serial terminal program to change the IP address.

As a first step, you may need to consult your system or network administrator to obtain unused IP addresses.

You can change the IP address from the default using the procedure in Section 4.3.2.1 (via PowerDNA Explorer) or Section 4.3.2.2 (via the serial port).

4.3.2.1 Update IP Address via PowerDNA Explorer

PowerDNA Explorer allows you to change IP addresses over your Ethernet connection. To update your DNR-MIL-x IP address using PowerDNA Explorer, you must first establish communication between your host PC and chassis.

If this is not already set up, refer to “Updating Firmware & PowerDNA Explorer Quick-Start” on page 45 for additional information about how to setup and use PowerDNA Explorer.

To update your IP address, do the following in the PowerDNA Explorer window:

a. Click **Scan Network** to explore your system (see Figure below)

b. Click the RACKtangle you want to update, (e.g., IOM-12345 in left sidebar device tree)

c. Enter the new IP address in the **IP 1** and press <Return>

d. Click **Store Configuration** to save your change and reset the DNR-MIL-x.

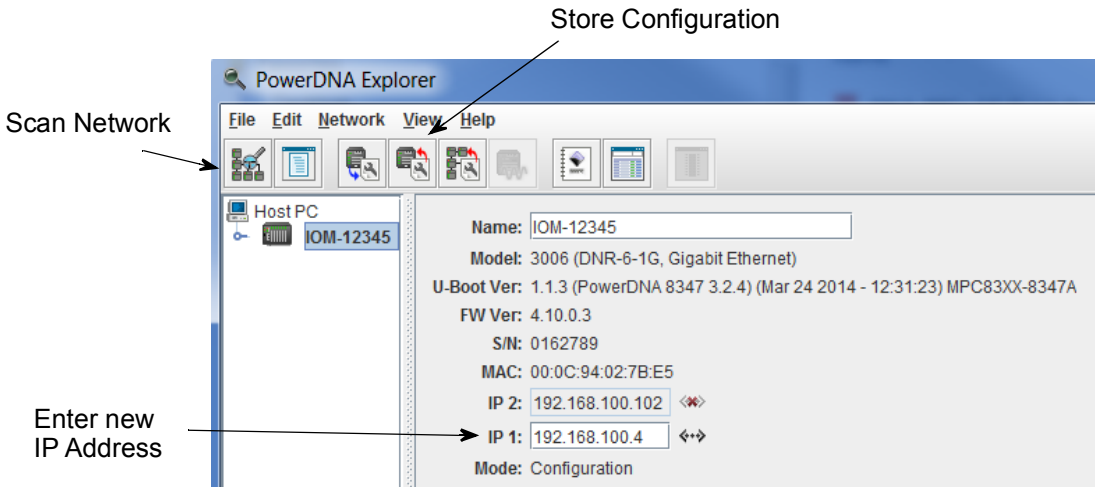


Figure 4-2. Using PowerDNA Explorer to Change IP Address

Storing the configuration downloads the new IP address into the system’s non-volatile memory.

You might also need to change the gateway and network mask to match settings on your LAN. These can be changed via the serial port: refer to Chapter 7 “CPU Programming in PowerDNA Mode” for more information.

4.3.2.2 Update IP Address via Serial Port

To change the IP address on your DNR-MIL-x system using the serial port, you must first establish serial communication between your host PC and chassis.

For more information about how to connect to the serial port, refer to the Initial Boot-up procedure in Section 4.2.

To update the IP address on your DNR-MIL-x chassis over the serial prompt, enter the following commands in the serial terminal window:

```
DQ> set ip 192.168.200.65        // Sets this system IP to 192.168.200.65
Enter user password >            // The default password is "powerdna"
powerdna

DQ> store                        // Saves the newly changed configuration
DQ> reset                        // Reboots the system for new IP to
                                 //  take effect
```

To verify, you can type `show` to display the new IP address. Refer to Chapter 7 "CPU Programming in PowerDNA Mode" for descriptions of commands you can issue via the serial application, such as the `set` and `store` commands.

Note that after your IP address is set, you can connect to your switch with a CAT5e/CAT6 cable and communicate with the DNR-MIL-x via Ethernet.

4.3.3 How to Change the Secondary (Diagnostic) IP Address (NIC2)

To change the IP address of the secondary port (NIC2), you use a serial terminal program as with the primary port, but instead use the command:

```
set ip2 aaa.bbb.ccc.ddd
```

where aaa.bbb.ccc.ddd is the new IP address for the secondary port.

Type '`store`' to save your settings and '`reset`' to reset the device.

Note that NIC2 IP addresses cannot be changed using PowerDNA Explorer.

4.3.4 How to Change the Host PC's MTU

Hosted PowerDNA-based systems such as the DNR-MIL-x require an Ethernet frame's payload, called the Maximum Transmission Unit or MTU, to be ≥ 1500 bytes. PowerDNA Explorer will warn you if your MTU is below 1500. Having an MTU that is too low will cause errors in communication.

In Windows XP, set the MTU value for the adapter connected to the DNR-MIL-x RACKtangle located at this address:

[HKEY_LOCAL_MACHINE\System\CurrentControlSet\Services\Tcpip\Parameters\Interfaces\[Adapter ID]\MTU] as a DWORD value to 0x5DC (1500 decimal).

In Windows Vista and higher, run Command Prompt as Administrator and type **netsh interface ipv4 show subinterfaces** to show the MTUs, and then type **netsh interface ipv4 set subinterface "***Local Area Connection***" mtu=1500 store=persistent**, where "*Local Area Connection*" is the name of the network interface that is connected to the DNR-MIL-x.

To avoid conflicts with your corporate LAN, ask your system administrator to change the MTU for you.

4.4 Improving Network Performance

To improve network performance, we recommend that instead of connecting to a company-wide network, you use a separate commercially-available network interface controller (NIC) card to, where possible, set up a single dedicated mini-network for DNR-MIL-x RACKs for operation & diagnostics, as shown in **Figure 4-4**.

As an alternative, you can configure two separate networks, one for operation and one for diagnostic purposes, as shown in **Figure 4-5**.

If you do not need to connect to a company LAN and only have a single DNR-MIL-x in your system, you can connect it directly to your host as shown in **Figure 4-3**. Note that for 1000BASE-T networks your cable may not exceed 100 meters.

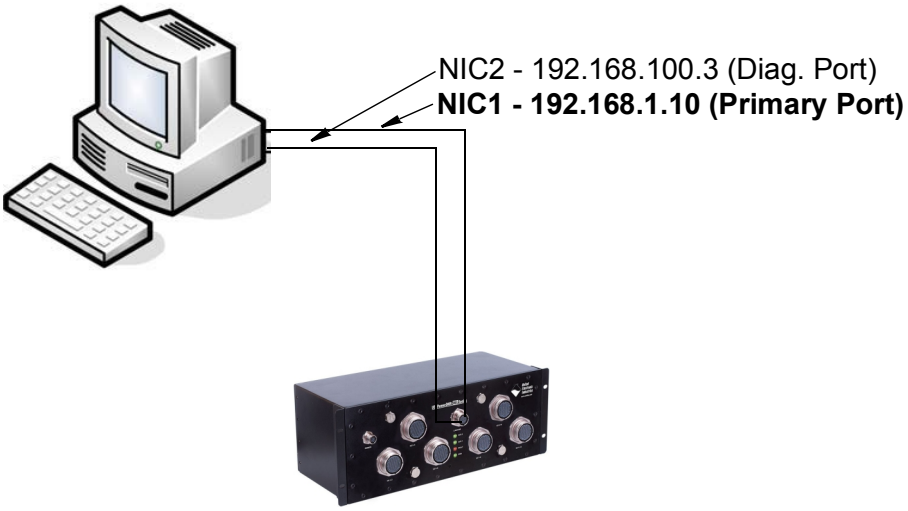


Figure 4-3. DNR-MIL direct-connected to Host without LAN Switch

Figure 4-4 shows a two-rack single network system with a LAN switch that performs both data acquisition and diagnostic functions. Diagnostic network is optional and can be used for either diagnostics or redundancy functionality.

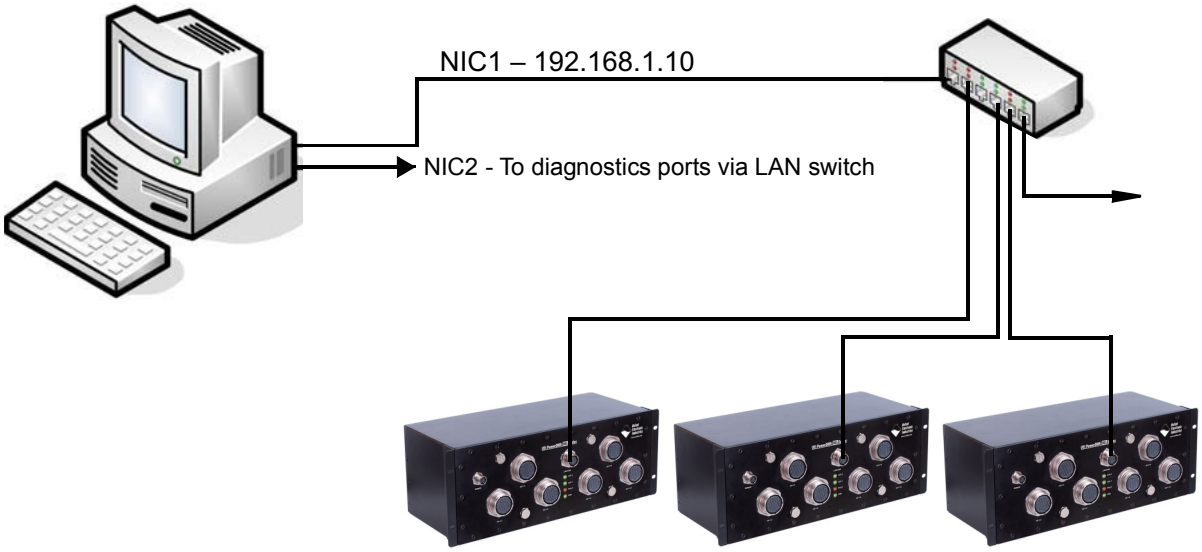


Figure 4-4. Single Network for Both Operation and Diagnostics Using DNR-MIL Racks and LAN Switch

Figure 4-5 shows a two-RACK dual network system with two LAN switches that perform both data acquisition and diagnostic functions.

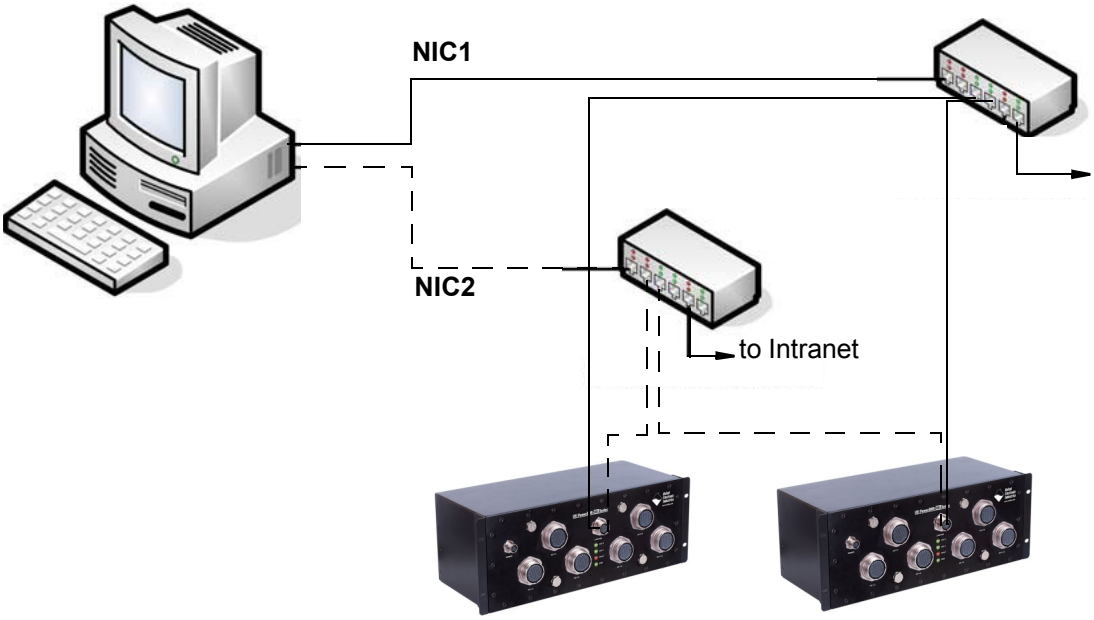


Figure 4-5. Separate Networks for Operation and Diagnostics Using Two DNR-MIL Racks and Two LAN Switches

As an example of setting up the above configuration, assume that your office uses a Class C network (the class intended for small networks with fewer than 256 devices) and your host PC is configured with a static IP or dynamically (via DHCP).

STEP 1: Obtain your networking configuration:

- On Windows systems, open the command prompt and type `ipconfig` to display the configuration:

Start>>Programs>>(Accessories>>) Command Prompt

```
C:\> ipconfig
Ethernet adapter NIC1 - Local Area Connection:
      Connection-specific DNS Suffix  . :
      IP Address. . . . . . . . . . . . : 192.168.1.10
      Subnet Mask . . . . . . . . . . . : 255.255.255.0
      Default Gateway . . . . . . . . . : 192.168.1.1
```

- On Linux systems, type the “`ifconfig`” command for configuration.

In the above example, the subnet range 192.168.1.0 through 192.168.1.255 is used by NIC1.

IP Addressing

The range of usable addresses is defined by the IP address and subnet mask. An IP address is a number that lies within the range of 0.0.0.0 and 255.255.255.255. In the example in the previous step, the IP address is 192.168.1.10.

The subnet mask indicates where an address range starts and stops. For example, a subnet mask 255.255.255.240 has 15 usable addresses (255.255.255.255 – 255.255.255.240 = 15).

In the example in step 1, the subnet is 255.255.255.0 for 255 addresses.

The subnet limits from anything.anything.anything.0 up to the max.

- The usable range for 192.168.1.10/255.255.255.0 is 192.168.1.1 to 192.168.1.254 (192.168.1.0 and 192.168.1.255 are reserved for Router and Broadcast messages).
- The usable range for 192.168.100.2/255.255.255.0 is 192.168.100.1 to 192.168.100.254

Note: Readily available “subnet calculators” can be accessed online, if needed.

Not every IP address from 0.0.0.0 to 255.255.255.255 is usable; however, these three ranges of IP addresses are guaranteed to be open for private use:

- 10.0.0.0 – 10.255.255.255
- 172.16.0.0 – 172.31.255.255
- 192.168.0.0 – 192.168.255.255

When possible, ask your system administrator to help you - this ensures that the network you’ve created does not conflict with your corporate network.

STEP 2: Install the secondary NIC card (if required).

STEP 3: Set up a network that does not overlap the existing one.

In this example, the address space 192.168.1.0-192.168.1.255 is used. The IP address block, 192.168.100.1 to 192.168.100.255 is available and is in the private range.

Let us choose 192.168.100.1-192.168.100.255 for the PC’s secondary NIC:

```
IPv4: 192.168.100.3
Netmask: 255.255.255.0
Gateway:192.168.100.3
```

On your host PC, open the Network and Internet section in the Control Panel:

Start >> Programs >> Control Panel >> Network and Internet >> View network status and tasks

Click *Change adapter settings* to bring up the Network Connections window.

Right-click the adapter to bring up the Properties window.

Open the TCP/IPv4 properties of the adapter and edit to the network settings noted above.

NOTE: If needed, refer to Appendix A for step-by-step instructions for setting up TCP/IPv4 properties.

Open the command prompt and confirm the network configuration using `ipconfig`:

Start >> Programs >> (Accessories >>) Command Prompt

```
C:\> ipconfig

Ethernet adapter NIC1 - Local Area Connection:
        Connection-specific DNS Suffix  . :
        IPv4 Address. . . . . . . . . . . : 192.168.1.10
        Subnet Mask . . . . . . . . . . . : 255.255.255.0
        Default Gateway . . . . . . . . . : 192.168.1.1

Ethernet adapter NIC2 - Local Area Connection 2:
        Connection-specific DNS Suffix  . :
        IPv4 Address. . . . . . . . . . . : 192.168.100.3
        Subnet Mask . . . . . . . . . . . : 255.255.255.0
        Default Gateway . . . . . . . . . : 192.168.100.3
```

STEP 4: Use a serial terminal application (e.g. MTTTY) on the host to configure the DNR-MIL-x system to use the same subnet as the host PC.
For example:

```
RACK IP: 192.168.100.2
RACK Gateway:192.168.100.1
Netmask: 255.255.255.0
```

From a serial terminal, enter the following commands when you see the `DQ>` command prompt:

```
DQ> set ip2 192.168.100.2          // Sets DNR-MIL diag IP to 192.168.100.2

DQ> set gateway2 192.168.100.1     // Sets this Gateway to 192.168.100.1
DQ> set netmask2 255.255.255.0     // Sets the subnet mask to 255.255.255.0

DQ> store                          // Saves the newly changed configuration,
DQ> reset                          //   the default password is 'powerdna'.
                                   // Reboots the system for the new IP to
                                   //   take effect.
```

STEP 5: Connect the DNR-MIL-x to your PC's second NIC, using a CAT5e/CAT6 cable. The green LEDs should light up to indicate that a link is active.

STEP 6: Ping the system to make sure that the DNR-MIL-x IP configuration is correct.

```
C:\> ping 192.168.100.2
Pinging 192.168.100.2 with 32 bytes of data:

Reply from 192.168.100.2: bytes=32 time<1ms TTL=128
Ping statistics for 192.168.100.2:
Packets: Sent = 1, Received = 1, Lost = 0 (0% loss),
```

The above shows a successful response.

A “Request Timed Out” or “Host Unreachable” message indicates an error.

STEP 7: The system should now be configured as shown in **Figure 4-6** (assuming NIC1 was already configured). The host NIC2 IP is 192.168.100.3, and the DNR-MIL-x NIC2 diagnostic port is 192.168.100.2.

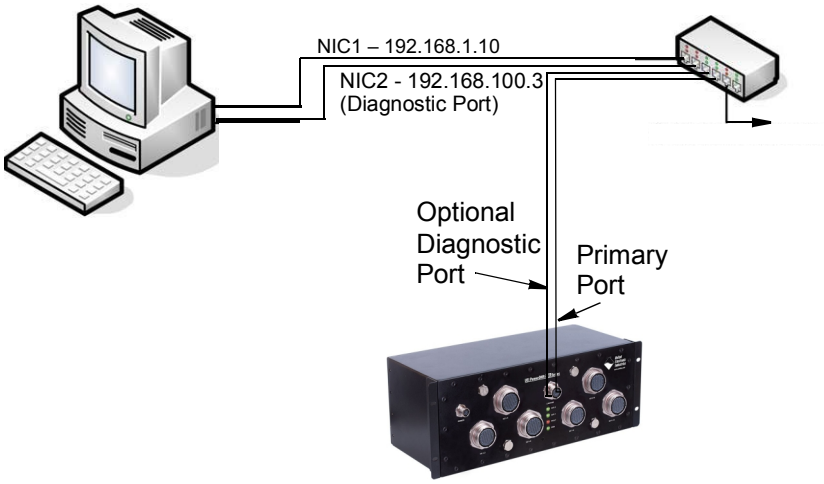


Figure 4-6. Typical Configuration for a DNR-MIL with a LAN Switch

STEP 8: You may now use PowerDNA Explorer to access the system. See Section 4.5 or Chapter 5 for more information about using PowerDNA Explorer.

4.4.1 Trouble-shooting

Refer to the following checklist when troubleshooting a system.

☑ Verify the Power Good LED is on: the 9-36V DC power supply is plugged into the DNA-CBL-1315-03 power cable connector. The red Failure LED is off and not blinking with a 400ms (overtemperature) or 200ms period (power rail). The Auxiliary LED is blinking at 1Hz to show a heartbeat.

☑ Verify the LED for the network is showing activity: the network cable(s) on the CPU/NIC are connected via the DNA-CBL-LAN-06 connector plug. If both NICs are down then the LED will blink with a 400ms period.

☑ Use the command prompt to ping <system IP>
(For example, `ping 192.168.100.2`)
If `ping` does not respond:

- Disable (temporarily) the firewall on the Host PC's NIC.
- Check the Host PC NIC's network settings.
- Check the DNR-MIL-x's network settings:
  - Use MTTTY and click **Connect**.
  - Press [Enter] to display the `DQ>` or `=>` prompt. (No prompt means not connected).
    - Verify that the serial cable is firmly connected to the RS-232 port.
    - Verify the settings: 57600 baud, no parity, 8 data bits, 1 stop bit.
    - Check the device manager on your PC to see which com port you are using. Enter that com port in your serial communications program, (e.g., COM1, COM2, COM3), click **Connect** and press [Enter].
  - Once at the `DQ>` prompt type "`show`" to verify the IP settings.

☑ Reboot the DNR-MIL-x system. Look for the text 'nif up' or 'nif down' in the serial debug console. 'nif up' indicates that the network interface has established a physical link with a switch or host PC, but does not indicate whether the IP settings are correct.

☑ Ensure that the computers are on a valid subnet and have valid IPs.

☑ Finally - contact UEI for support at support@ueidaq.com.

4.5 Updating Firmware & PowerDNA Explorer Quick-Start

This section provides instructions for updating firmware using PowerDNA Explorer or using the serial port (see “Firmware Update Instructions” on page 48) and an introduction to PowerDNA Explorer (see section below).

PowerDNA Explorer is a UEI-developed application that “explores” the LAN, looking for connected PowerDNA chassis, and provides an interface for viewing and manipulating system settings.

Chapter 5 covers the PowerDNA Explorer capabilities in detail. The following section provides a quick-start guide.

PowerDNA Explorer is available on Windows or Linux systems.

On Windows systems, access PowerDNA Explorer from the Start menu:

- *Start > All Programs > UEI > PowerDNA > PowerDNA Explorer*

On Linux systems, access PowerDNA Explorer under the UEI installation directory (`<PowerDNA-x.y.z>/explorer`) by typing:

- `java -jar PowerDNAExplorer.jar`

4.5.1 Getting Started with PowerDNA Explorer

PowerDNA Explorer identifies DNR-MIL-x and other PowerDNA systems on a selected network. The discovered systems are listed in the Device Tree in the left-hand panel of the display.

- To display pertinent hardware and firmware information, select a specific system in the Device Tree.
- To manipulate I/O board inputs or outputs, click to select a board of a specific system.

For PowerDNA Explorer to connect to DNR-MIL-x systems on your network, it must be programmed with an IP address range that includes the IP addresses of your DNR-MIL-x systems:

STEP 1: Select *Network >> Address Ranges* from the menu:

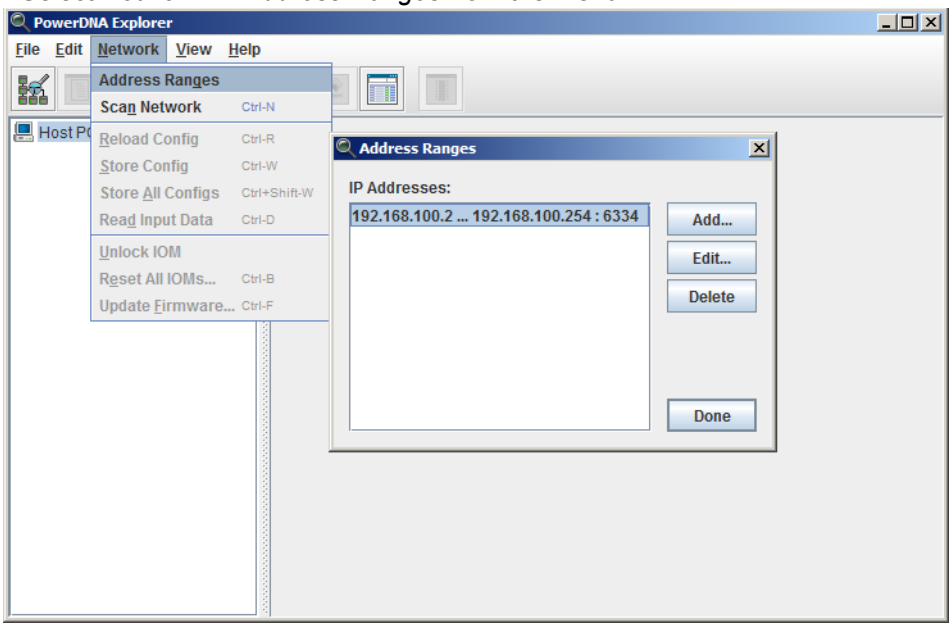


Figure 4-7. Address Ranges to be Scanned

STEP 2: Add the IP address of the DNR-MIL-x system (e.g. 192.168.100.2), and click **Done**.

STEP 3: Click *Network >> Scan Network* to scan the LAN for DNR-MIL-x systems within the range specified in the previous step.

One or more gray icons will display in the left-hand-side of the screen. If no icons are displayed, refer to the Troubleshooting note in the previous section.

STEP 4: Double-click an icon to display its information and list the I/O boards:

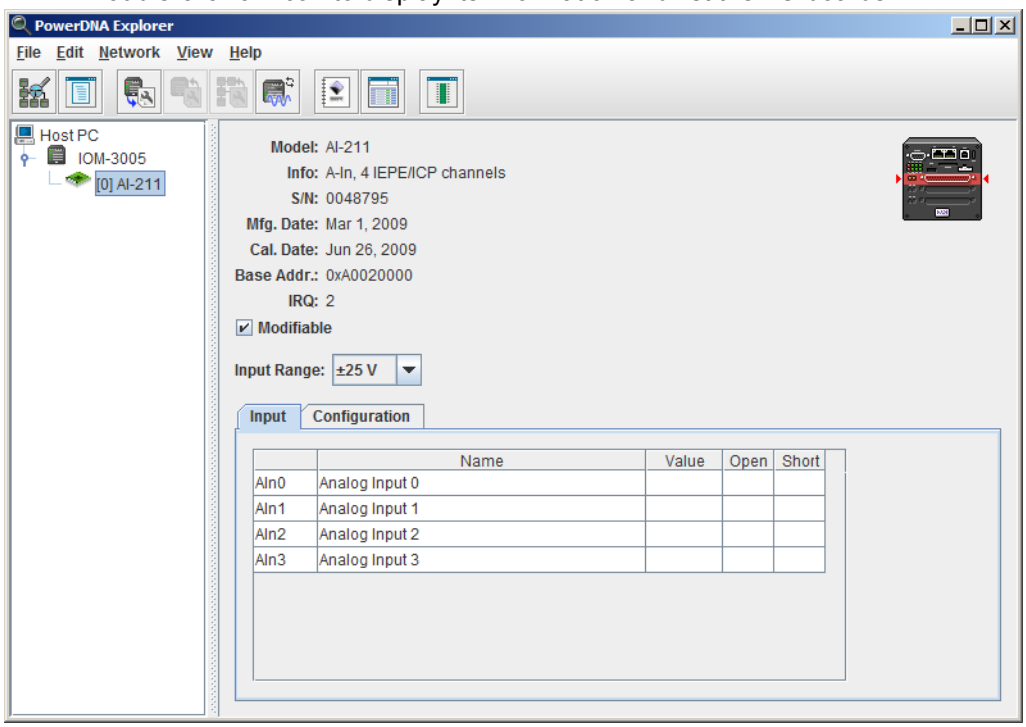


Figure 4-8. Typical Screen for Analog Input Board

The above screenshot is from the PowerDNA Explorer Demo. The “demo” version provides a simulator without any real hardware intended for new users who want to explore the PowerDNA Explorer program without reading/writing to real hardware. Run this program and hover your mouse over the buttons to read the tool-tips to learn by interacting with the program.

Some quick notes:

- ☑ To change the I/O board, the “Modifiable” check box should be set.
- ☑ To read from a board, click the fourth-to-last button: “Read Input Data”
- ☑ To write to the board, change the value and click the fourth (or fifth) button with the red arrow on top of the cube: “Store Configuration”. The icon with the blue arrow above it restores the configuration.
- ☑ To change the IP, change the number, deselect the field, and “Store Configuration”. Take care not to set the IP address to outside of the network’s configuration subnet or to an IP address that is currently in use, as the system will then become unreachable.

See Chapter 5 “PowerDNA Explorer” for additional information.

4.5.2 Firmware Update Overview

CPU firmware for the DNR-MIL-x system is stored on the DNR-CPU-1GBM CPU.

Updated firmware is periodically released to introduce new features and to improve the performance of existing features. Updated releases of the firmware are bundled with the entire PowerDNA Software Suite, available for download at any time from the UEI web site (www.ueidaq.com).

To locate the latest UEI firmware after installing the PowerDNA Software Suite, browse to the installation's Firmware directory,
(e.g. C:\Program Files\UEI\PowerDNA\Firmware).

The directory contains an MTTTY executable and two sub-directories containing the firmware.

Choose the sub-directory corresponding to the architecture of your system: for the DNR-MIL-x, this is the **Firmware_PPC_1G** sub-directory and the ROM image file with extension MOT.

On host PCs running Windows systems, you can check the version of firmware running on your DNR-MIL-x with the following procedure:

a. Turn on power.

b. Connect the system to its network.

c. Start PowerDNA Explorer on the Microsoft Windows desktop from

Start >> Programs >> UEI >> PowerDNA >> PowerDNA Explorer

d. In the PowerDNA Explorer menu, click *Network >> Scan Network.*

e. Select the DNR-MIL-x icon you wish to query (by clicking the icon).

f. Note the version shown in the **FW Ver** field (e.g. FW Ver: 4.6.0.1).
If the version of your PC's PowerDNA Software Suite is not the same as the firmware version on the RACK then a warning symbol will be displayed as shown below.

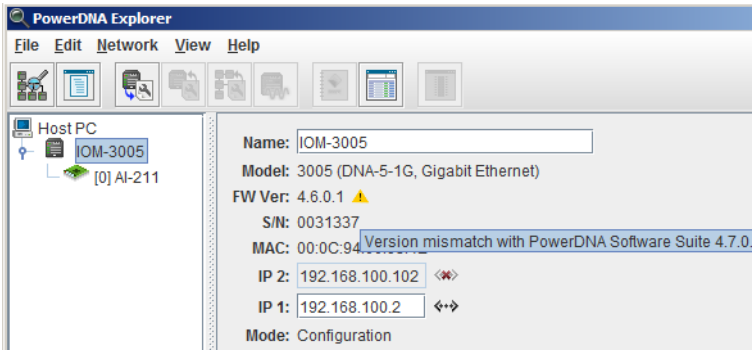


Figure 4-9. Displaying the Version of Your Firmware

For older versions of firmware (e.g. 3.x.x), refer to the user manual on the CD that accompanied your device when you purchased it for firmware update instructions.

4.5.3 Firmware Update Instructions

Before using a new release of the libraries and applications, you should install the latest version of the firmware onto the DNR-MIL-x CPU (DNR-CPU-1GBM). Operational errors can occur when the version of the firmware does not match the version of the PowerDNA Software Suite used.

Instructions for updating the DNR-MIL-x system via PowerDNA Explorer (over Ethernet LAN line), and over MTTTY (serial line) are provided below.

NOTE: The preferred method of updating firmware is using PowerDNA Explorer.

CAUTION!
If you update the firmware in a DNR-CPU-1GBM using PowerDNA Explorer, be sure to use PDNA Explorer from the same release as the new firmware.

Firmware Update via a LAN Ethernet Connection

To upload firmware with PowerDNA Explorer over LAN, do the following:

STEP 1: Turn on power on.

STEP 2: Connect the DNR-MIL-x system to its network.

STEP 3: Start PowerDNA Explorer. On the Microsoft Windows desktop:
Start >> Programs >> UEI >> PowerDNA >> PowerDNA Explorer

STEP 4: In the PowerDNA Explorer window, click *Network >> Scan Network*. All discovered UEI chassis will display in the left-side panel.

STEP 5: Click the DNR-MIL-x system to be updated.

STEP 6: Click *Network >>Update Firmware*…from the menu.

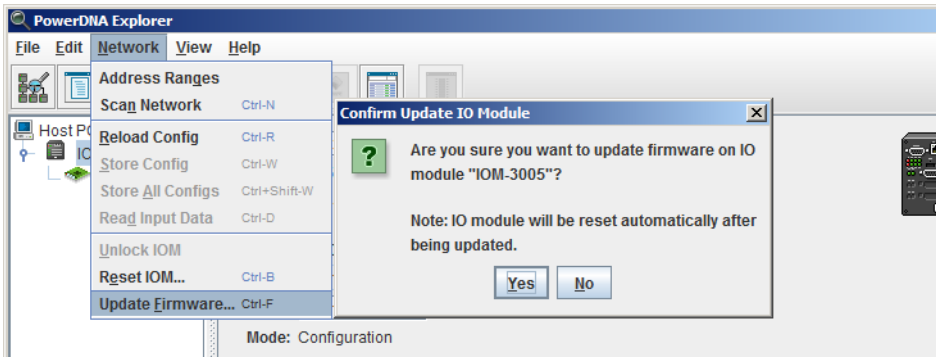


Figure 4-10. Update Firmware Menu Item

STEP 7: Click "Yes" when you see the prompt:
`"Are you sure you want to update firmware…"`

STEP 8: Double-click the **rom8347_4_X_X_X.mot** file.

STEP 9: If asked, enter the password to continue. More information about passwords can be found in Chapter 7 of this manual. DNR-MIL-x systems come with the default password set to `powerdna`.

Figure 4-11. Password Dialog Box

STEP 10: Wait for the progress dialog to complete. The system will then be updated and running the new firmware.

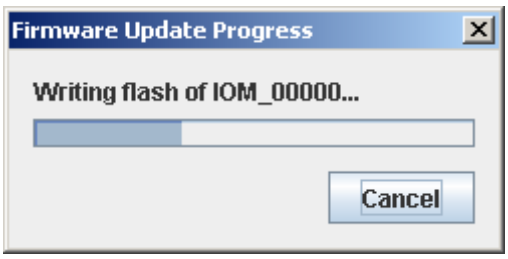


Figure 4-12. Firmware Update Progress Dialog Box

Each system is updated in three steps. First, the firmware is transferred to the system. Second, the firmware is written to the flash memory. Third, the system is reset. When the system is finished resetting, the PG light is lit.

Firmware Update via Serial Port

To upload firmware over the serial port using a terminal client (e.g. MTTTY), do the following:

STEP 1: Establish serial communication between the host PC and a DNR-MIL-x CPU over the serial link using your serial terminal client (refer to Initial Boot-up procedure on page 34, if needed).

STEP 2: Press <Return> until you see the `DQ>` prompt.

STEP 3: Type `reset` in the serial terminal window.

STEP 4: While the system is starting up again, press ESC to go into **U_Boot**.

STEP 5: Type the commands shown below to erase firmware storage area in the Flash memory and load the firmware:

```
=> erase FF800000 FF9FFFFF
=> loads
```

NOTE: The `loads` command stores firmware into flash while downloading it.

STEP 6: Do the following to transfer the Motorola firmware image file (refer to Figure 4-13):

a. In the MTTTY menu bar, select *Transfer » Send File*.

b. Navigate to your UEI installation, and select the image file:

```
\Program Files\UEI\PowerDNA\Firmware\Firmware_PPC_1G\rom8347_4_x_y.mot
```

NOTE: A progress bar will appear in the lower left corner of MTTTY, indicating progress.

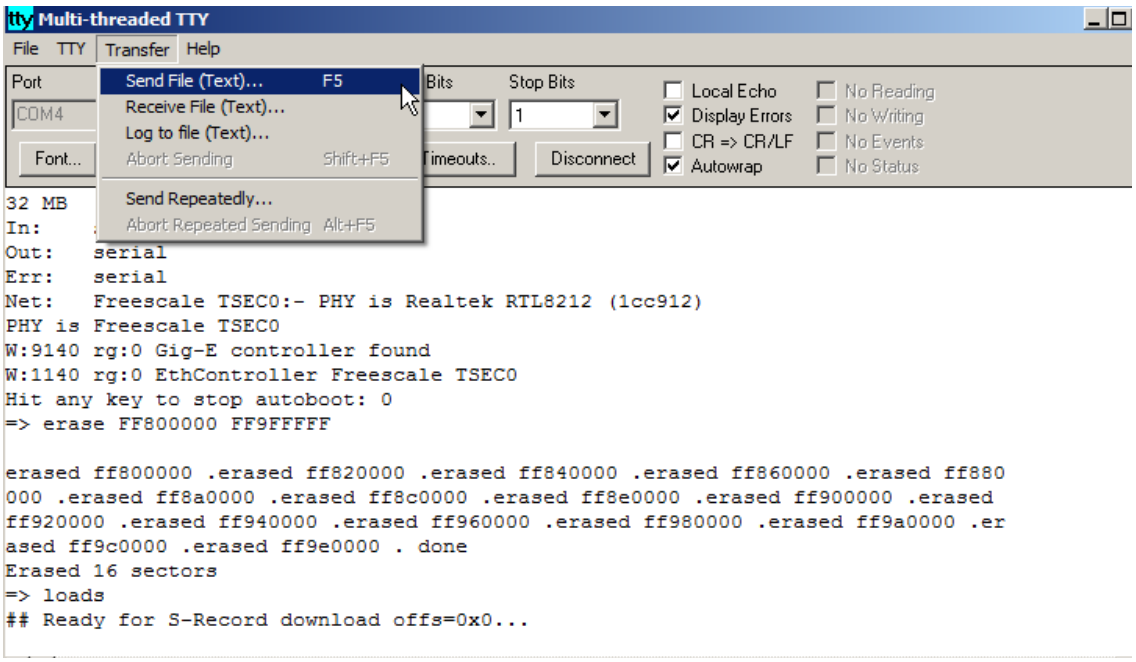


Figure 4-13. Firmware Update via Serial Port

STEP 7: Wait for the upload to complete (it may take a few minutes).

STEP 8: After the process finishes, enter the **`go ff800100`** command. The DNR-MIL-x system will then be updated and running the new firmware.

4.6 Peripheral Terminal Panel Wiring

Refer to the applicable I/O board manuals for proper wiring to boards. You can find your manual in the documentation that came with the PowerDNA Software Suite, or download documentation on www.ueidaq.com.

Refer to Section 2.8 on page 14 for more information about pinouts and connectors.

4.7 Repairing (and Upgrading) Your DNR-MIL-x System

DNR-MIL-x systems come from the factory fully configured and calibrated.

If you want to enhance, repair, or modify a specific I/O board, we recommend that you send the DNR-MIL-x system back to the factory or to your local distributor for repair/modification.

This process requires that you request an RMA number from UEI before shipping. To request an RMA, contact support@ueidaq.com and provide the following information:

1. Model Number of the unit
2. Serial Number of the unit
3. Reason for return
   - Calibrating the board(s)
   - Defective board for repair
   - Upgrade with additional board(s)

UEI will process the request and issue an RMA number.

4.8 Configuring a NIC Port for Diagnostic Mode

The CPU module has two Ethernet ports, NIC1 and NIC2. Either port can be assigned as the Main Operation Port or as a Diagnostics Port.

The main and diagnostics ports are interchangeable. The user application can open both ports independently and use separate handles to access each of them. A port becomes a diagnostics port, which prevents changes in the state of the ongoing operation, after it is configured and locked-in as a diagnostics port. This allows great flexibility in IOM wiring — if either port or its cabling fails, you can use the other port as the main port.

If all I/O boards are in configuration mode and the lock is not set, the diagnostics port functions as an equivalent of the main port. Any command that can be executed on the main port can be executed on the diagnostics port as well.

Refer to the PowerDNA API Reference Manual for API used with this section.

The following standard DAQBIOS commands are accessible on the diagnostics port whenever one or more I/O boards are in operating mode:

```
DQCMD_ECHO       // echo
DQCMD_RDCFG      // read configuration (new)
DQCMD_RDSTS      // read status
DQCMD_WRCHNL (selected)//write channel
DQCMD_RDCHNL (selected)// read channel
DQCMD_IOCTL (selected) // ioctl() - low priority command
DQCMD_SETLOCK    // set/release port lock
```

Commands that are capable of changing the state of the running I/O boards will not execute.

To switch a port into diagnostics mode, use the `DqCmdSetLock` API, as described below:

```
int DAQLIB DqCmdSetLock(int Iom, uint8 Mode,char Password,uint32 *IP)

Parameters:
  int Iom          // Pointer to the DQIOME structure
  uint8 Mode       // Function mode (lock/unlock/check/diagnostics)
  char *Password   // password string; ignored (and can be NULL)
                   //  if Mode is DQSETLOCK_CHECK
  uint32 *IP       // returns the IP address of the locking host
                   //  if Mode is DQSETLOCK_CHECK
```

<`Mode`> can be one of the following:

```
#define DQSETLOCK_LOCK   0    // Lock IOM to host
#define DQSETLOCK_UNLOCK 1    // Unlock IOM
#define DQSETLOCK_CHECK  2    // Get locking host IP
#define DQSETLOCK_DIAG   4    // Switch to diagnostics
```

To advance a port into diagnostics mode, call this function with the <`Mode`> parameter set to `DQSETLOCK_DIAG`. To return a port to normal mode, use the same function call with `DQSETLOCK_UNLOCK`.

The following table describes the possible states of both ports:

Table 4-1 Port States

Port	LOCK State	First Port (NIC1)	Second Port (NIC2)
First	`DQSETLOCK_UNLOCK`	Full functionality	Full functionality
	`DQSETLOCK_LOCK`	Full functionality, locked to the host	All but state change functions
	`DQSETLOCK_DIAG`	Diagnostic functionality only	Full functionality
Second	`DQSETLOCK_UNLOCK`	Full functionality	Full functionality
	`DQSETLOCK_LOCK`	All but state change functions	Full functionality, locked to the host
	`DQSETLOCK_DIAG`	Full functionality	Diagnostics functionality only

DQCMD_ECHO

This command returns information about the board(s) installed. Use of this command is described in the PowerDNA API Reference Manual.

DQCMD_RDCFG

This command returns the current configuration of the specified board(s):

```
int DAQLIB DqCmdReadCfg(int Iom, DQRDCFG pDQRdCfg[], uint32 maxsize, uint32*
entries)

  int Iom              // a pointer to the DQIOME structure
  DQRDCFG pDQRdCfg[]   // structure that contains board configuration
  uint32 maxsize       // number of DQRDCFG structures passed
  uint32* entries      // number of DQRDCFG structures returned
```

```
typedef struct (
    uint8 DEV;       // device (host fills this field)
    uint8 ss;        // subsystem (host)
    uint32 status;   // device status (device returns following fields)
    uine32 cfg;      // configuration, including clocks
    uint32 rate;     // clock divider in 15.5ns intervals
    uint32 clsize;   // size of the channel list
    uint32 cl[];     // channel list - variable size
) DQRDCFG, *pDQRDCFG;
```

Note: Use `device!=0x80` to indicate that this is the last device in the list.

DQCMD_RDSTS

This command returns the status of the IOM and each and every board in the stack (upon request):

```
int DAQLIB DqCmdReadStatus (int Iom, uint8 *DeviceNum, uint32 *Entries,
uint32 *Status, uint32 *StatusSize)

Parameters:
  int Iom             // A pointer to the DQIOME structure
  unit8 *DeviceNum    // Array of board numbers to retrieve status
  uint32 *Entries     // Number of entries in DeviceNum array
  uint32 *Status      // Buffer to store values received from device
  uint32 *StatusSize  // Size of buffer, 32-bit chunks.
                      //   Returns number of 32-bit values
                      //   copied into Status
```

There are special device numbers to access status of various boards:

`OxFE` – returns IOM status and status of all boards (note that each board status is expressed as four 32-bit words. Thus, the maximum size of status packets is (4 + 14*4)*sizeof(uint32) = 240 bytes).

`0x7F` – returns IOM status only (four bytes)

`0x0 . . .0xE` – returns status of one of the boards

The status for each board consists of four 32-bit words, as follows:

```
/* status offsets into devob].status array */
#define STS_STATE (0)  // state of the board
#define STS_POST  (1)  // post status
#define STS_FW    (2)  // firmware status
#define STS_LOGIC (3)  // logic status
```

The first word is the state of the board – what mode of operation it is in, and the lower 8-bits of the timestamp. If the 10 us timestamp does not change after each call, the logic is in the inoperative state, as:

```
/* state flags */
#define STS_STATE_TS_SH                (8)
#define STS_STATE_TS_SH_INS(S,TS,MD)
                              ((S & 0xffff00f0)|((TS<<8) & 0xff00)|(MD&0xf))
#define STS_STATE_STICKY               (0)
```

The second word describes the status of the board. It is written when the board enters initialization mode and remains unchanged until the next reboot. `STS_POST_SDCARD_FAILED`, `STS_POST_DC24` and `STS_POST_DCCORE` can be changed during operation if the corresponding failure occurs.

```
/* POST status flags */
#define STS_POST_MEM_FAIL       (1L<<0)   // Memory test failed
#define STS_POST_EEPROM_FAIL    (1L<<1)   // EEPROM read failed
#define STS_POST_LAYER_FAILED   (1L<<2)   // board failure
#define STS_POST_FLASH_FAILED   (1L<<3)   // Flash checksum error
#define STS_POST_SDCARD_FAILED  (1L<<4)   // SD card is not present
#define STS_POST_DC24           (1L<<5)   // DC->24 board failed
#define STS_POST_DCCORE         (1L<<6)   // Core voltage problem
#define STS_POST_BUSTEST_FAILED (1L<<7)   // Bus test failed (hwtest.c)
#define STS_POST_BUSFAIL_DATA   (1L<<8)   // Bus test failed on data tst
#define STS_POST_BUSFAIL_ADDR   (1L<<9)   // Bus test failed on addr tst
#define STS_POST_OVERHEAT      (1L<<10)   // Overheat detected

#define STS_POST_STICKY        (STS_POST_MEM_FAIL|STS_POST_BUSTEST_FAILED|
                                STS_POST_BUSFAIL_DATA|STS_POST_BUSFAIL_ADDR)
```

The third word contains the logic status flags. They are read and assembled from the various registers of the common board interface (CLI) upon request. Not all boards implement full functionality and boards operating normally should not show any flags set.

```
/*logic status flags */
#define STS_LOGIC_DC_OOR          (1UL<<0)   // DC/DC out of range (IOM
                                             //also)
#define STS_LOGIC_DC_FAILED       (1UL<<1)   // DC/DC failed (IOM also)
#define STS_LOGIC_TRIG_START      (1UL<<2)   // Trigger event started
                                             // (IOM also)
#define STS_LOGIC_TRIG_STOP       (1UL<<3)   // Trigger event stopped
                                             // (IOM also)
#define STS_LOGIC_CL0_NOT_RUNNING (1UL<<4)   // Output channel list not
                                             // running
#define STS_LOGIC_CLI_NOT_RUNNING (1UL<<5)   // Input channel list not
                                             // running
#define STS_LOGIC_CVCLK_CL0_ERR   (1UL<<6)   // CV clock error for CL0
#define STS_LOGIC_CVCLK_CLI_ERR   (1UL<<7)   // CV clock error for CLI
#define STS_LOGIC_CLCLK_CL0_ERR   (1UL<<8)   // CL clock error for CL0
#define STS_LOGIC_CVCLK_CLI_ERR   (1UL<<9)   // CL clock error for CLI

#define STS_LOGIC_NO_REPORTING    (1UL<<31)  // Installed logic does not
                                             // support error reporting

#define STS_LOGIC_STICKY          (STS_LOGIC_NO_REPORTING)
```

The fourth word contains the status of the firmware. A board operating normally does not have any flags set except `STS_FW_CONFIG_DONE`, which means the board was properly configured before entering operating mode (it is cleared upon re-entering configuration mode) and `STS_FW_OPER_MODE`, which means that the board switched into operating mode without any errors.

```
/* fw status flags */
#define STS_FW_CLK_OOR       (1UL<<0)   // Clock out of range (IOM
                                        // also)
#define STS_FW_SYNC_ERR      (1UL<<1)   // Synchronization interface
                                        // error (IOM also)
#define STS_FW_CHNL_ERR      (1UL<<2)   // Channel list is incorrect
#define STS_FW_BUF_SCANS_PER_INT
                             (1UL<<3)   // Buf setting error:
                                        //    scans/packet
#define STS_FW_BUF_SAMPS_PER_PKT
                             (1UL<<4)   // Buf setting error:
                                        //    samples/packet
#define STS_FW_BUF_RING_SZ   (1UL<<5)   // Buf setting error: FW
                                        // buffer ring size
#define STS_FW_BUF_PREBUF_SZ (1UL<<6)   // Buf setting error: Pre-
                                        // buffering size
#define STS_FW_BAD_CONFIG    (1UL<<7)   // Board cannot operate in
                                        // current config
#define STS_FW_BUF_OVER      (1UL<<8)   // Firmware buffer overrun
#define STS_FW_BUF_UNDER     (1UL<<9)   // Firmware buffer underrun
#define STS_FW_LYR_FIFO_OVER (1UL<<10)  // Board FIFO overrun
#define STS_FW_LYR_FIFO_UNDER(1UL<<11)  // Board FIFO underrun
#define STS_FW_EEPROM_FAIL   (1UL<<12)  // Board EEPROM failed
#define STS_FW_GENERAL_FAIL  (1UL<<13)  // Board general failure
#define STS_FW_ISO_TIMEOUT   (1UL<<14)  // Isolated part reply timeout
#define STS_FW_FIR_GAIN_ERR  (1UL<<15)  // Sum of fir coeffs is not correct
#define STS_FW_OUT_FAIL      (1UL<<16)  // Output CB tripped or over-
                                        // current
#define STS_FW_IO_FAIL       (1UL<<17)  // Messaging I/O failed (5xx
                                        // boards)
#define STS_FW_NO_MEMORY     (1UL<<18   //Error with memory allocation
#define STS_FW_BAD_OPER      (1UL<<19)  // Operation was not performed
                                        // properly
#define STS_FW_LAYER_ERR     (1UL<<20)  // Board entered operation
                                        // successfully

#define STS_FW_CONFIG_DONE   (1UL<<30)  //Configuration is completed
                                        // (no error)
#define STS_FW_OPER_MODE     (1UL<<31)          // Board entered operation
                                        // mode successfully

/* status helper macros/defines */
#define STS_FW_STICKY (STS_FW_EEPROM_FAIL|STS_FW_GENERAL_FAIL)
```

Status bits are divided into “conditional” and “sticky”. Conditional bits are set when a condition arises; they are cleared when the error condition expires. Sticky bits are persistent once set and are cleared by reading their status.

DQCMD_IOCTL

This command is used to retrieve data from the board. When a port is in diagnostic mode, it returns current data but cannot reprogram the channel list. The channel list is used to inform the handler the ID of the channel from which data should be retrieved.

Functions which rely on the DQCMD_IOCTL command for transport are listed in the PowerDNA API Reference Manual.

Sequence of Operation

To use the diagnostic port without affecting performance of the main port, UEI recommends that you use the following sequence of operations:

1. Open main port.
2. Open diagnostics port.
3. Perform hardware reset (optional) and re-open ports, if needed.
4. Lock diagnostic port into DQSETLOCK_DIAG.
5. When operation is configured on the main port, read the status of the diagnostics port to verify that the configuration was programmed correctly.
6. Once operation on the main port is started, the diagnostics port becomes available for data retrieval.
7. Read status of the diagnostics port to make sure that all layers of interest successfully entered operating mode without error.
8. In the cycle:
    a. Retrieve the current status once a second.
    b. Check the flags for error conditions.
    c. Retrieve additional data if any flags are set.
9. Stop operation and unlock diagnostics port.
10. Resume normal operation with main port.

Chapter 5 PowerDNA Explorer

PowerDNA Explorer is a UEI-developed Java application that simplifies configuration and quick testing of DNR-MIL-x RACKtangle™ systems.

This section describes the various menus/screens in PowerDNA Explorer.

- The Main Window (Section 5.1)
- Menu Bar (Section 5.2)
- Toolbar (Section 5.3)
- Device Tree (Section 5.4)
- Settings Panel (Section 5.5)
- Exploring I/O Boards with PowerDNA Explorer (Section 5.6)
  - Digital Input/Output Board Settings (Section 5.6.1)
  - Analog Output Board Settings (Section 5.6.2)
  - Analog Input Board Settings (Section 5.6.3)
  - Counter/Timer Board Settings (Section 5.6.4)

UEI provides a PowerDNA Explorer DEMO with the installation that allows you to safely explore the menus and I/O board screens without using actual hardware. DEMOs are located in the same directories as the PowerDNA Explorer executables.

For getting started information, refer to the “Updating Firmware & PowerDNA Explorer Quick-Start” on page 45.

NOTE: Throughout this chapter, several figures display graphical representations of Cube-based systems. Note that information about the display is identical for the DNR-MIL-x.

5.1 The Main Window

The Main Window of PowerDNA Explorer is shown in **Figure 5-1**.

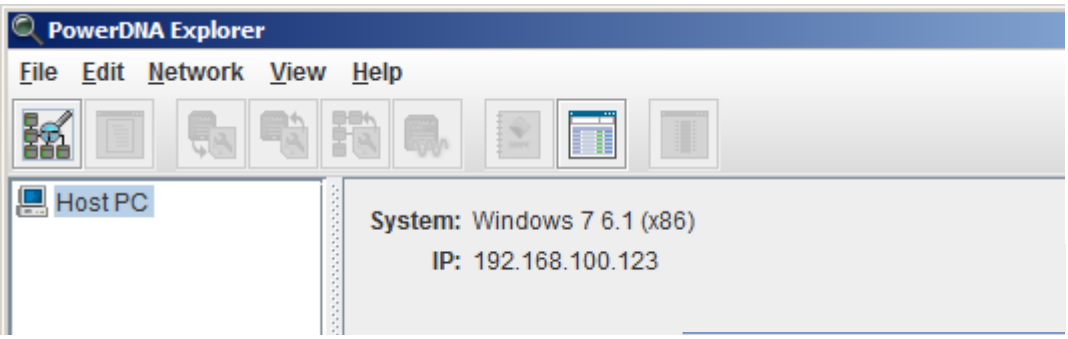


Figure 5-1. PowerDNA Explorer Main Window

The Main Window opens after PowerDNA Explorer is first launched and is where you do most of your work. It has four main parts: the Menu Bar, the Toolbar, the Device Tree, and the Settings panel.

5.2 Menu Bar

The Menu Bar contains the following menus and menu items.

5.2.1 File Menu

File >> Preferences brings up the preferences dialog.

The preferences dialog allows you to specify the network timeout interval. This is the length of time PowerDNA Explorer will wait for response from a CPU/NIC Core Module before giving up with an error. It defaults to 500 milliseconds.

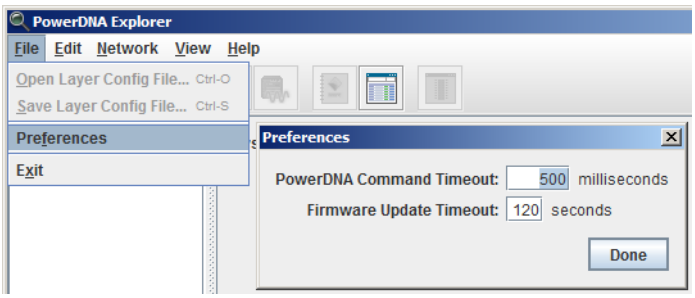


Figure 5-2. Preferences

File >> Exit exits the application. If there are unsaved device settings, you will be prompted for confirmation.

5.2.2 Network Menu

Network >> Address Ranges brings up the Address Ranges dialog, allowing you to specify a range of IP addresses to scan for devices.

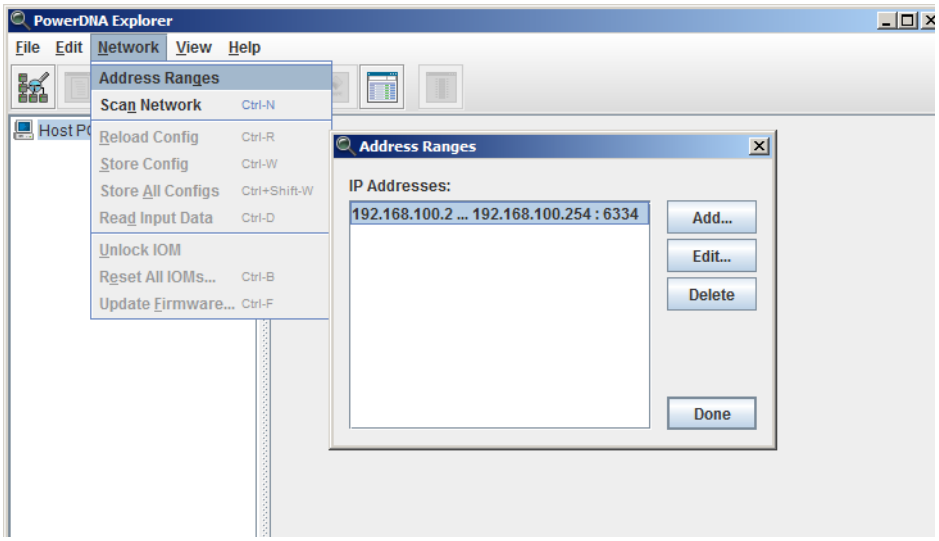


Figure 5-3. Address Ranges Dialog Box

The Address Ranges dialog allows you to specify the IP addresses and UDP port to use to find devices. You can specify individual addresses as well as address ranges. The specified items appear in a list to which you can add or delete. This list defaults to a single range item that specifies the range 192.168.100.2 ... 192.168.100.10.

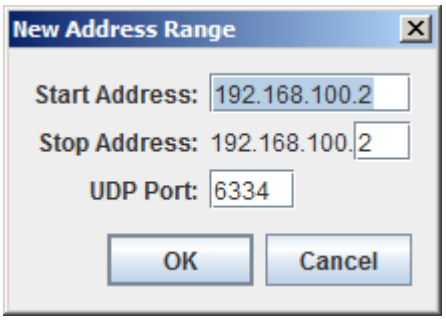


Figure 5-4. Edit Address Ranges Dialog Box

Network >> Scan Network scans the network for devices and populates the device tree. How much of the network is scanned depends on the settings in the Network Ranges dialog.

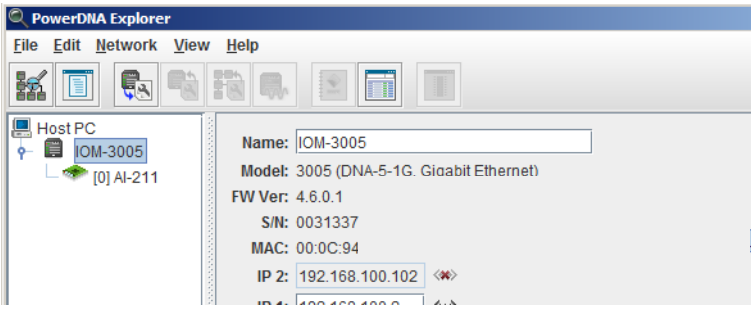


Figure 5-5. After a Network >>Scan Network

If you choose *Scan Network* when the device tree is already populated, any new devices discovered will be added to the tree. Any existing devices that are missing will be removed from the tree, unless you have made unsaved changes to such a device's configuration, in which case it will be marked in the tree as missing.

Network >> Reload Config re-reads the configuration of the current device selected in the Device Tree. If you have made changes to the settings in the settings panel for the current device, Read will replace those settings with the current settings for the device, after prompting for confirmation.

Network >> Store Config writes the changed settings for the currently selected device to the device. The button is disabled for devices that haven't been modified.

Network >> Store All Configs writes all of the changed device settings to the devices. The button is disabled if no devices have been modified.

Network >> Start Reading Input Data is enabled when the currently selected device is an input device board. It reads the current input values to the device and causes them to be displayed in the settings panel.

Network >> Update Firmware… loads a firmware update file to all connected DNR-MIL-x systems if Host PC is selected. It updates only one DNR-MIL-x system when a specific unit is specified.

Note that writing certain configuration changes to a PowerDNA system will bring up a password dialog box. More information about passwords can be found in “Setting and Reading CPU Core Parameters via Serial Port” on page 81.

DNR-MIL-x systems come with the default password set to “**powerdna**”.

Figure 5-6. Password Dialog Box for “Store Config” and “Store All Configs”

Figure 5-7. Password Dialog Box for “Update Firmware . . .”

5.2.3 View Menu

View >> Show Wiring Diagram provides a diagram of the connector pins for a specific board. All boards have this feature, and we display this one as an example. The wiring diagrams in PowerDNA Explorer match the wiring diagrams in this manual in the sections for each board.

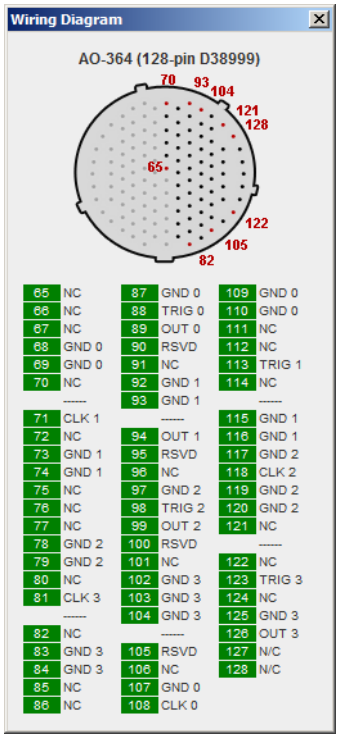


Figure 5-8. Example of a Wiring Diagram Display

5.2.4 Help Menu

Help >> About PowerDNA Explorer shows the **About ...** box, which shows the program icon, program name, version number, company name, and copyright notice.

5.3 Toolbar

The Toolbar contains the following buttons: **Scan Network**, **Reload Config**, **Store Config**, **Store All Configs**, **Read Input Data**, and **Show Wiring Diagram**. They duplicate the functionality of the corresponding menu items as described above.

5.4 Device Tree

When the application is first launched, the tree contains just a root item representing the host computer.

When you select **Scan Network** from the Network menu or the Toolbar, the device tree is populated with all central controllers, IOMs, and device boards accessible from the network, as filtered through the Network Ranges dialog. Central controllers, if any, appear as children of the Host PC item. IOMs that are connected to the PC without use of a central controller also appear as direct children of the Host PC item.

Each item has an icon indicating whether it is a central controller, IOM, or board. The text label for each item is the device's model number, name, and serial number. Boards are also labeled with their position number in brackets.

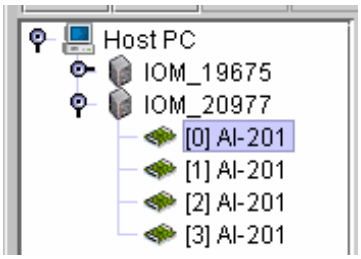


Figure 5-9. Example of the Device Tree

When an item is selected in the tree, the settings panel changes to reflect the settings for that device. The first time an item is selected, the device is queried as though you had invoked the **Start Reading Input Data** command. On subsequent selections of the same item, the last settings are re-displayed. Thus, if you made changes but did not write them to the device, the changes are remembered. Invoking the **Start Reading Input Data** command will re-read the device and overwrite the current settings in the settings panel.

Devices whose settings have changed, but have not been written, are displayed in bold italics in the tree to provide a visual cue. Changed devices that become missing on a subsequent invocation of **Scan Network** turn red in the tree. (Unchanged items that become missing are simply removed from the tree.)

5.5 Settings Panel

The settings panel presents a set of controls that allow you to change the settings of the device currently selected in the device tree.

5.5.1 IOM Settings

The settings panel has the following controls when an IOM is selected in the tree.

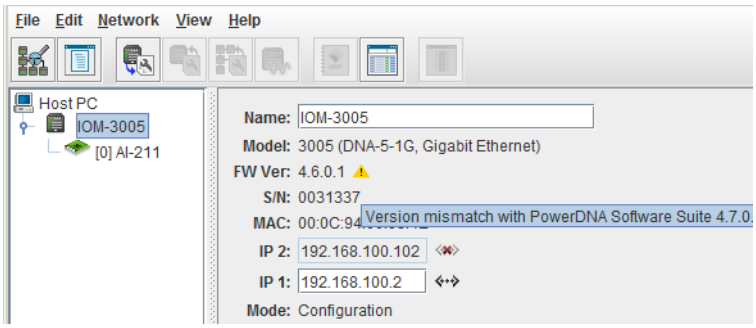


Figure 5-10. Example of IOM Settings Panel

Name shows the IOM name. It can be changed.

Model shows the model number of the IOM.

FW Ver shows the version of the firmware installed on the PowerDNA cube. An orange warning triangle and tooltip will appear if your version is mismatched.

S/N shows the serial number of the IOM.

MAC shows the Ethernet card's fixed MAC address.

IP 2 and 1 fields allow the IP addresses of the IOM to be edited. The icon to the right is superimposed with a red X when there is no network cable in that port.

Mode shows the mode the IOM is in.

5.5.2 I/O Board / Device Settings

Figure 5-11 shows the screen for displaying I/O device settings.

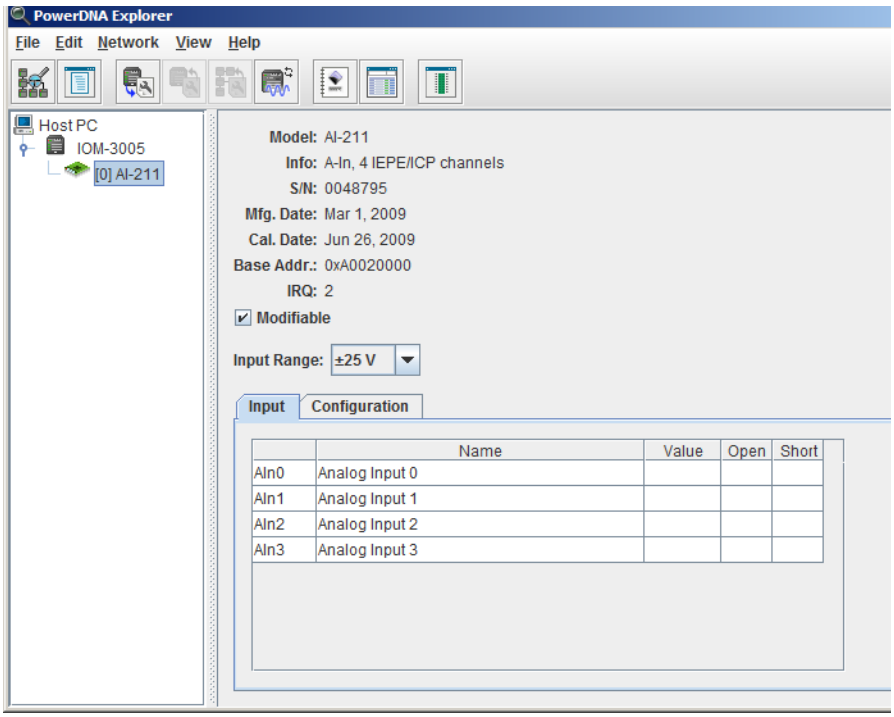


Figure 5-11. Example of I/O Device Settings

Each I/O device has the following settings.

- **Model** shows the model number of the device.
- **Info** shows some key features of the device: A for analog, D for digital, In for input, Out for output, and a number of channels available.
- **S/N** shows the device serial number.
- **Mfg. Date** shows the manufacturing date.
- **Cal. Date** shows the date of the last calibration done.
- **Modifiable** is a checkbox which, when unchecked, excludes the device from configuration. The device is excluded from the **Store All Configs** command, and the **Reload Config** command is disabled. Also, the device appears gray in the tree. All devices are enabled by default.

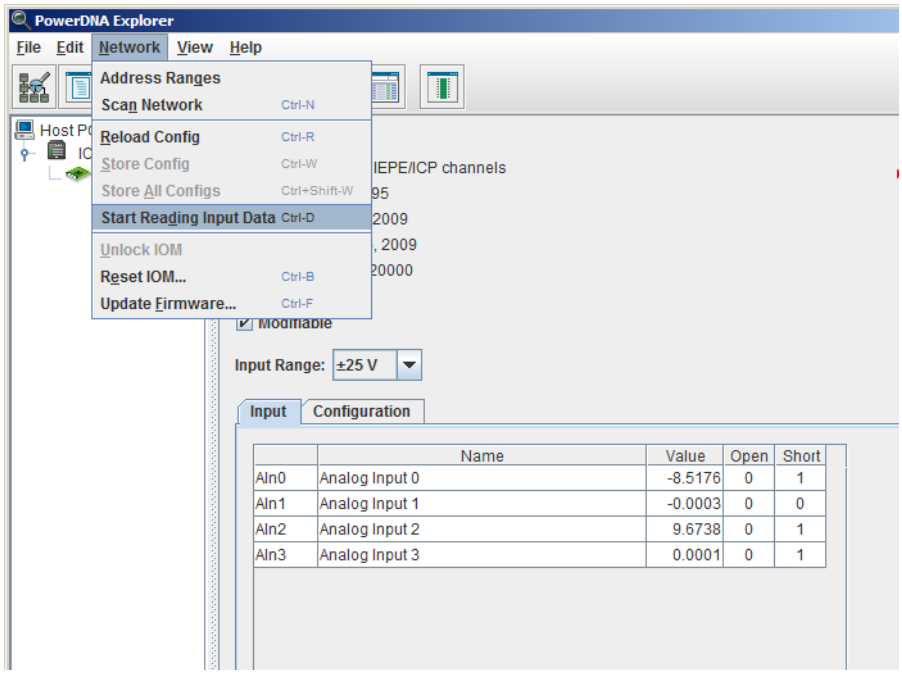


Figure 5-12. Screen from Network >> Start Reading Input Data

5.5.2.1 Interacting with I/O Boards

To read data from an I/O board, select *Network >> Start Reading Input Data***.** The **Value** column for any inputs will update, as shown above in the settings panel.

Also in the settings panel, you can add or edit channel names. After editing names, choose *Network >> Store Config* to save changes to the board. This is true for all boards.

Additionally, if you have changed a configuration value, but have not chosen *Network >> Store Config* to save them, previous values can be re-read from the board, using *Network >> Reload Config*.

5.6 Exploring I/O Boards with PowerDNA Explorer

Settings available through PowerDNA Explorer will be dependent on the settings specific to each board types.

Examples of settings for several types of I/O boards are provided in subsections below:

- Digital Input/Output Board Settings (Section 5.6.1)
- Analog Output Board Settings (Section 5.6.2)
- Analog Input Board Settings (Section 5.6.3)
- Counter/Timer Board Settings (Section 5.6.4)

NOTE: Examples in this section are an introduction to PowerDNA Explorer capabilities; please note PowerDNA Explorer provides a communication link with all types of UEI I/O boards, not just the board-types listed in this section.

5.6.1 Digital Input/ Output Board Settings

The following examples show screens associated with the DIO-405, and then show how the DI-401, DO-402 and DIO-403 are different.

NOTE: Use *Network >> Start Reading Input Data* to see immediate input values in Input tabs. Use *Network >> Store Config* to save values to the module.

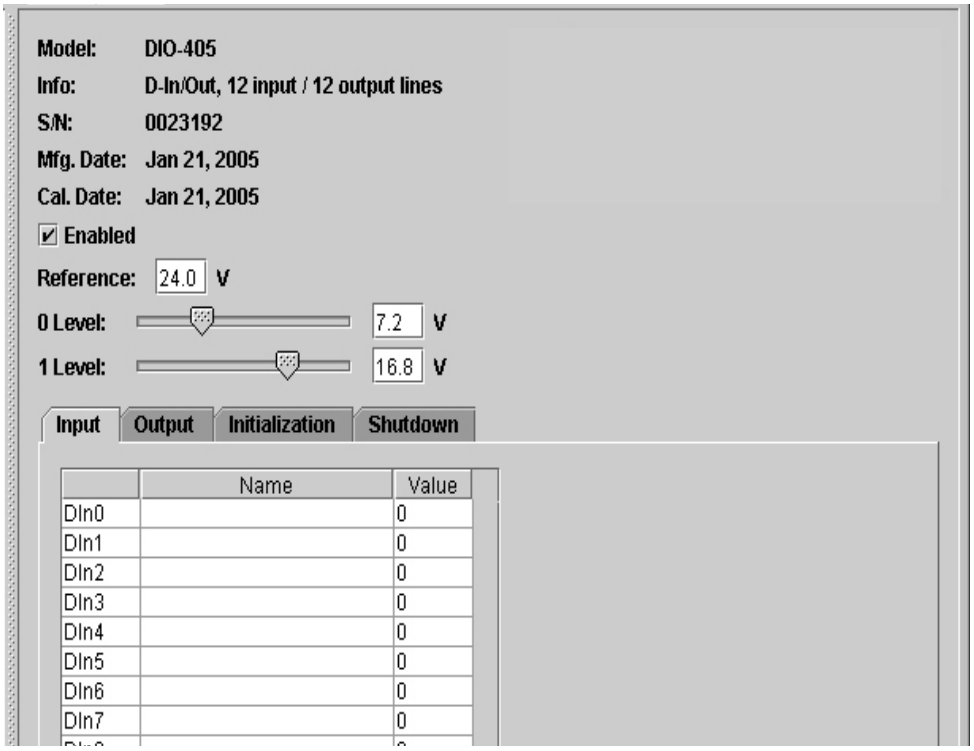


Figure 5-13. Example DIO-405 Input Pane

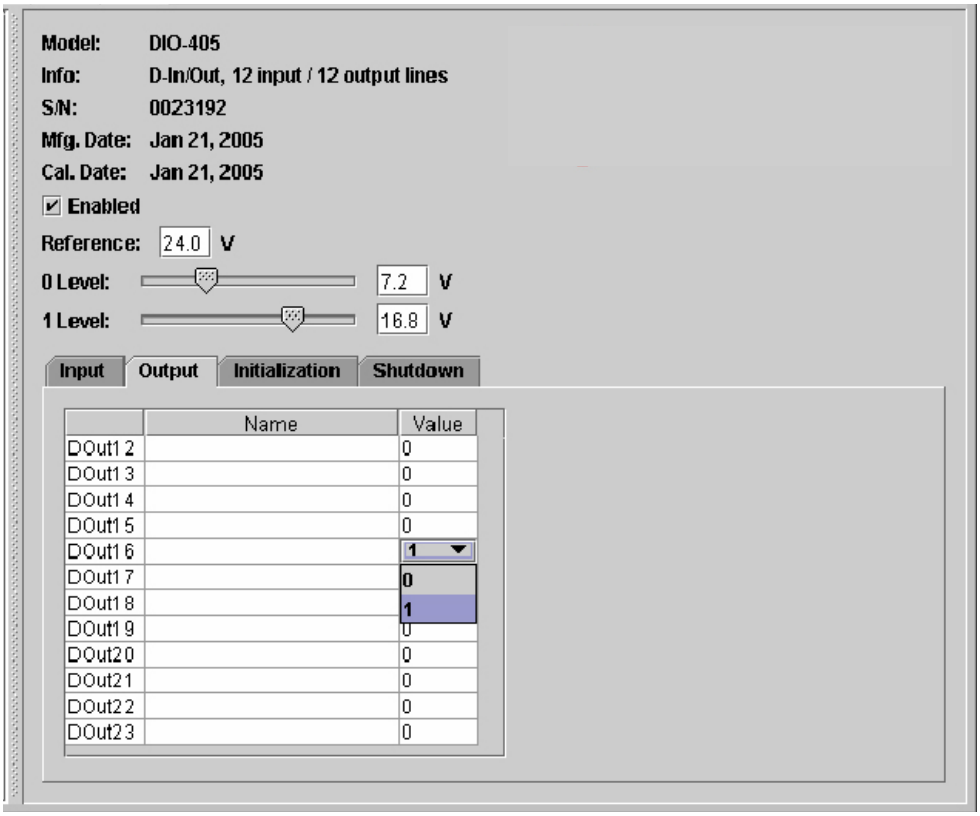


Figure 5-14. Example DIO-405 Output Pane

Reference is a reference voltage.

0 level/1 level are hysteresis values described fully in the DIO-401/2/5 manuals.

Input/Output/Initialization/Shutdown tabs switch between settings for initial and shutdown states, as well as operation mode configuration, and display of current data.

All tabs contain the following columns:

- The first column contains the channel list.
- **Name** is a user-defined string.
- **Value** contains 0 or 1. It is a drop-down menu for output channels allowing you to select 0 or 1.

Note that different board types offer different options in the display, dependent on the features of the board:

- The DI-401 module provides Reference and 0 and 1 Level controls, and Input tab.
- The DO-402 module provides Output, Initialization, and Shutdown tabs; no Reference value or Level sliders.
- The DIO-403 module is different because it groups 8-bits at a time into ports, and three ports into two channels. For the sake of abstraction in PowerDNA Explorer, we'll call all the ports channels.

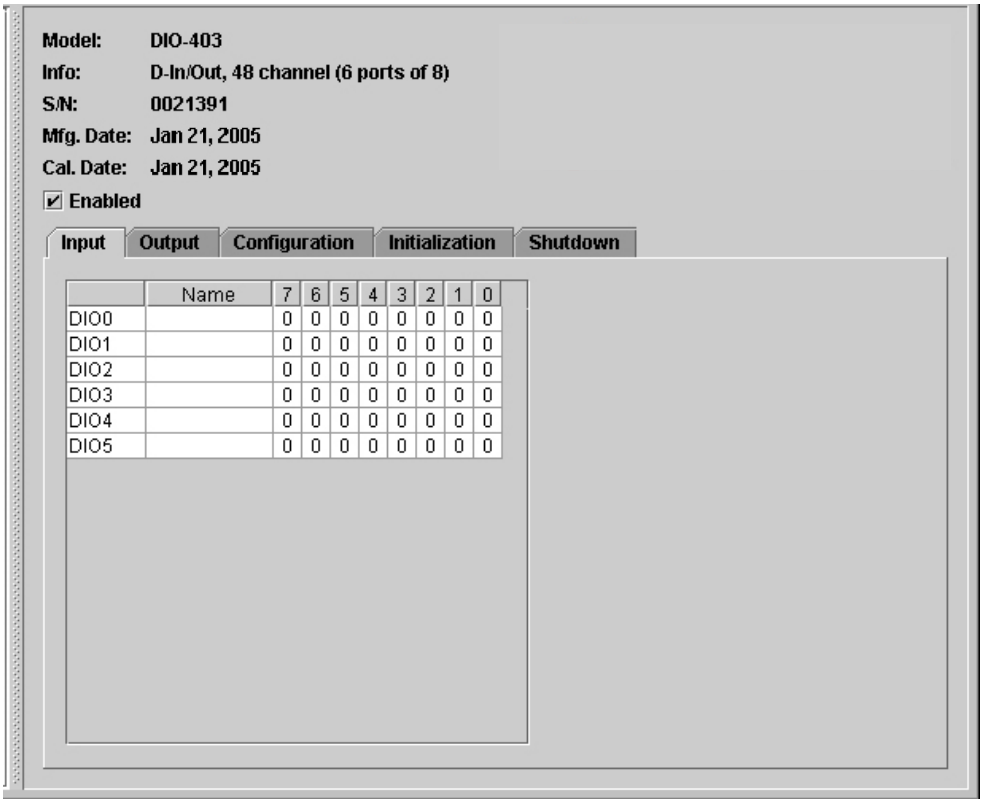


Figure 5-15. Example of DIO-403 Input Pane

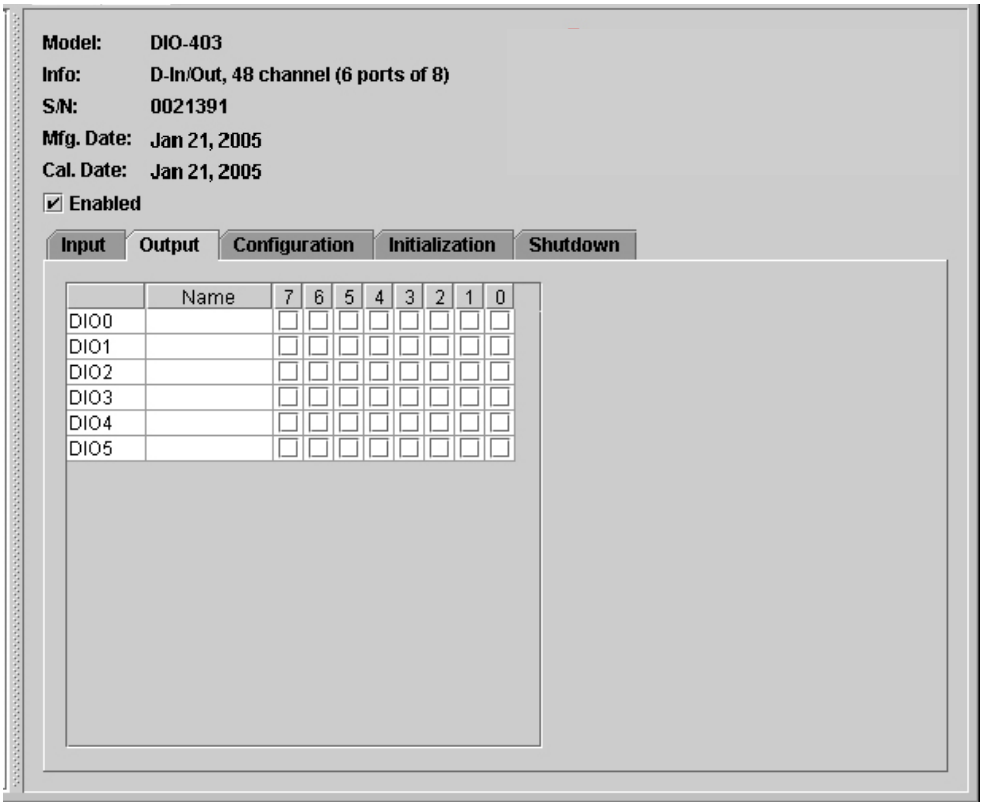


Figure 5-16. Example of DIO-403 Output Pane

Input/Output/Configuration/Initialization/Shutdown tabs switch between settings for initial and shutdown states, as well as operation mode configuration, and display of current data.

Input/Output tabs get/set the current input/output values. They contain the following columns:

- The first column contains the channel list.
- **Name** is a user-defined string.
- **7 through 0** contain the values 0 or 1. For the output tab, they are checkmarks for output channels allowing you to select 0 (unchecked) or 1 (checked).

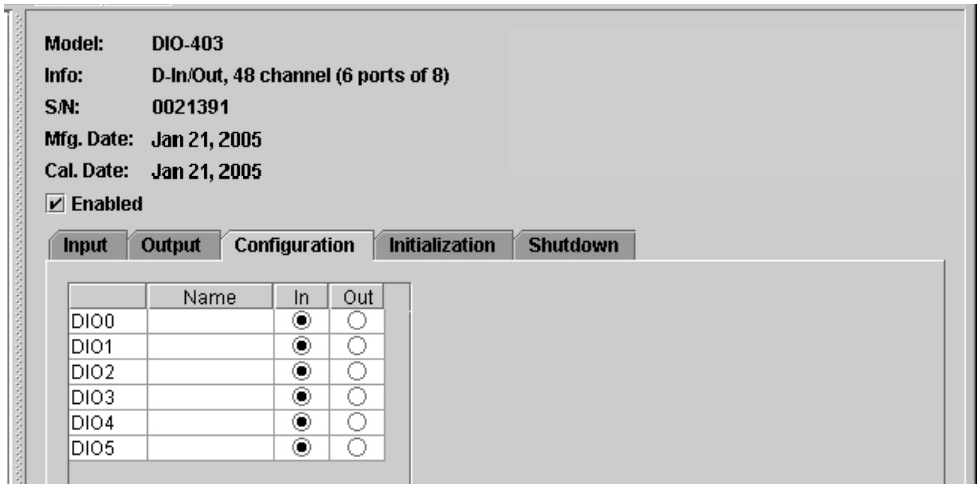


Figure 5-17. Example of DIO-403 Configuration Pane

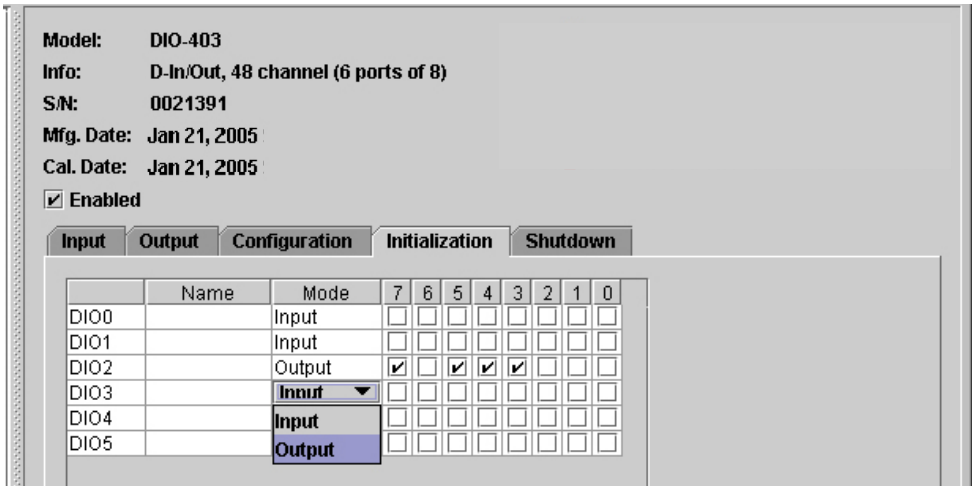


Figure 5-18. Example DIO-403 Startup Value Pane

Configuration tab gets/sets the current input/output directions per port. It contains the following columns:

- The first column contains the channel list
- **Name** is a user-defined string
- **In/Out** contains toggle switches to select whether the channel is to be used for input or for output.

Initialization/Shutdown tabs allow you to set port as input or output, and set output values. They contain the following columns:

- The first column contains the channel list.
- **Name** is a user-defined string.
- **Mode** specifies whether the channel is input or output.
- **7 through 0** contain the values 0 or 1. They are checkmarks for output channels that allow you to select 0 (unchecked) or 1 (checked).

5.6.2 Analog Output Board Settings

The following example shows screens associated with the AO-308.

NOTE: Use *Network >> Start Reading Input Data* to see immediate input values in Input tabs. Use *Network >> Store Config* to save values to the module.

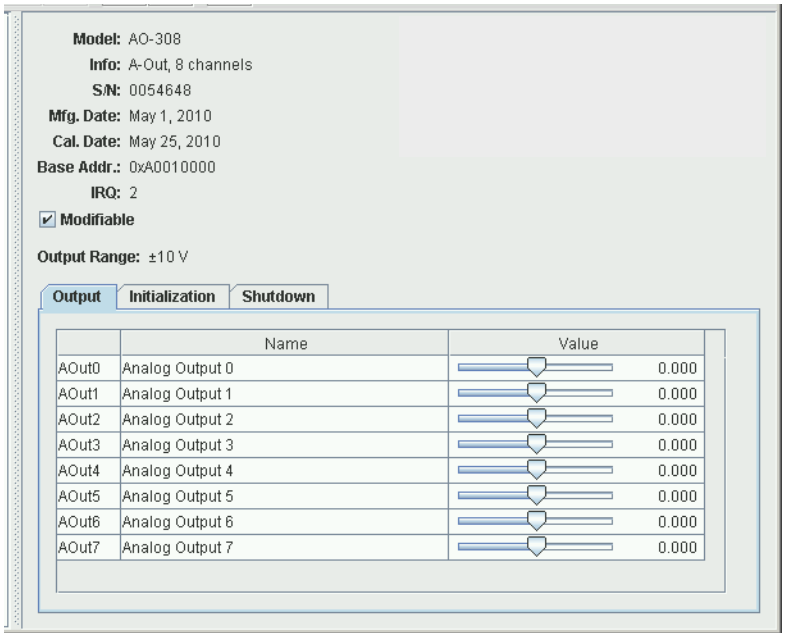


Figure 5-19. Example AO-308 Module

You can change output, initialization, and shutdown values. You can also change Output Range using the combo box, and this only affects values displayed in initialization and shutdown tabs. You can then choose *Network >> Store Config* to apply all changes to the module.

Output/Initialization/Shutdown tabs switch between settings for initial and shutdown states, as well as operation mode configuration.

The **Output, Initialization** and **Shutdown** tabs contain the channel list table, which has the following columns:

- The first column contains the channel list.
- **Name** is a user-defined string.
- **Value** contains a slider to set the voltage to output from the channel and the numerical voltage value, which you can input directly. The actual voltage depends on the selected output range.

5.6.3 Analog Input Board Settings

The following example shows screens associated with the AI-211.

NOTE: Use *Network >> Start Reading Input Data* to see immediate input values in Input tabs. Use *Network >> Store Config* to save values to the module.

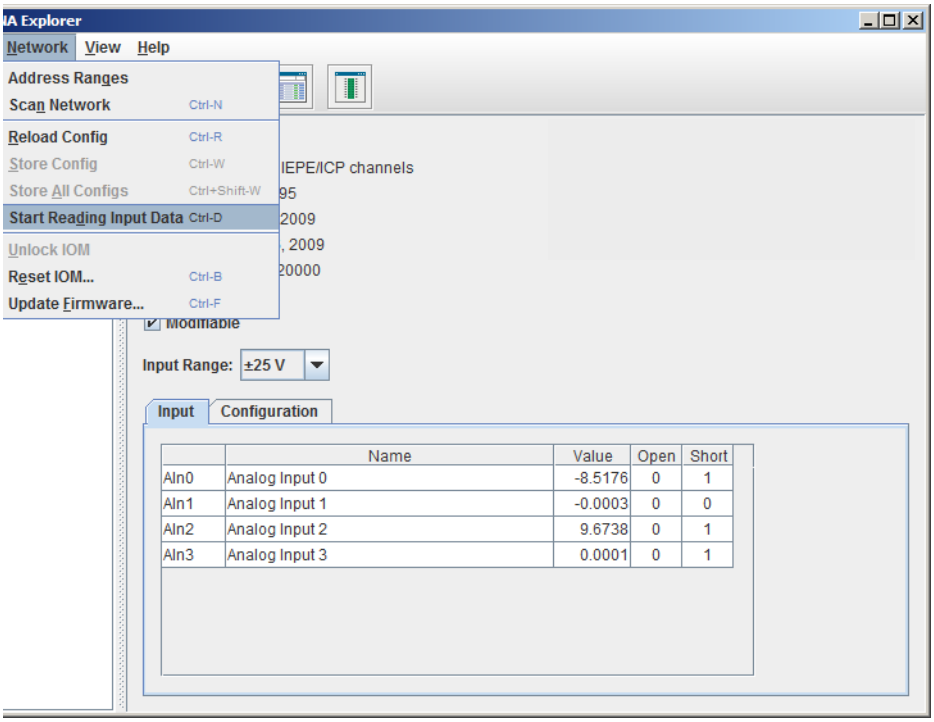


Figure 5-20. Example AI-211 Module

Input Range shows the specified input range. It cannot be changed and is informational only.

The Data table contains the values currently coming into the device. The table is initially blank until you click *Start Reading Input Data*, unless auto-refresh is activated in the preferences dialog. The table shows three columns:

- The first column contains the channel list.
- **Name** is a user-defined string.
- **Value** shows the current value.

5.6.4 Counter/Timer Board Settings

The following example shows screens associated with the CT-601.

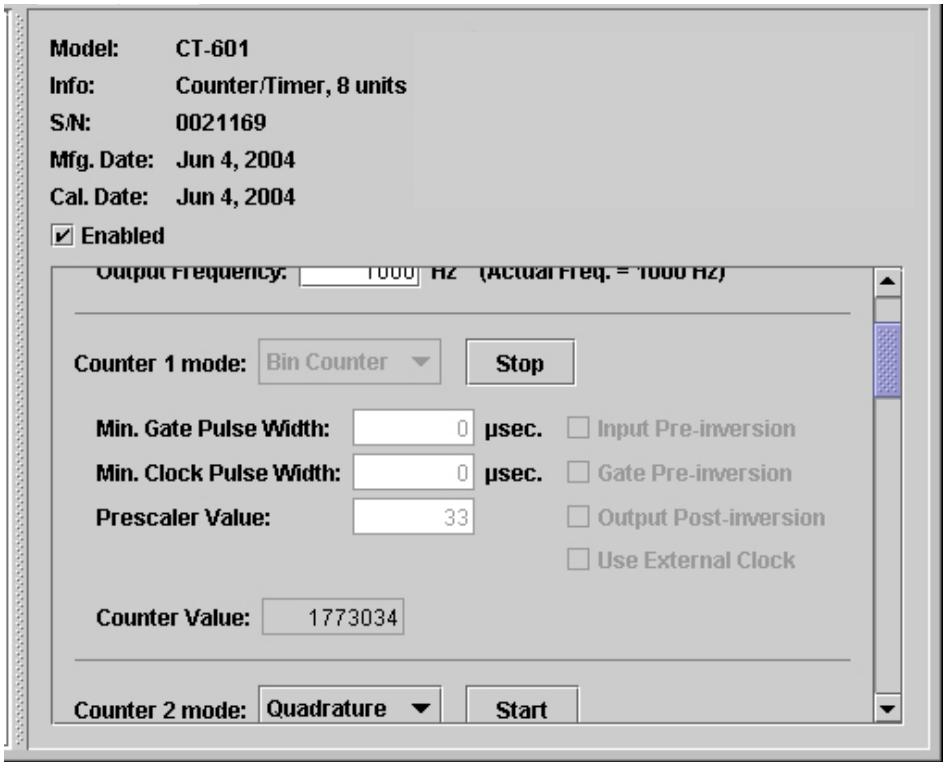


Figure 5-21. Example CT-601 Module Configuration Pane

The CT-601 module has 8 counters. Each counter can be set to one of four different modes: Quadrature, Bin Counter, Pulse Width Modulation (PWM), or Pulse Period. When you change the mode of a counter using the mode combo box, the controls for that counter will change to those appropriate for the mode.

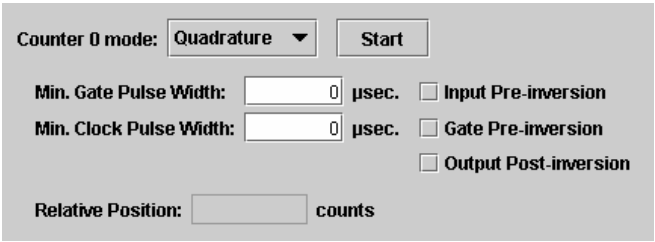


Figure 5-22. Example Quadrature Controls

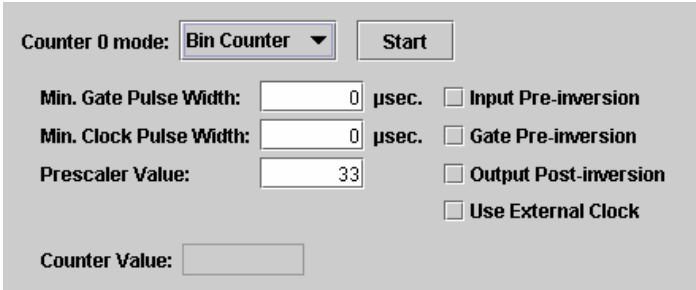
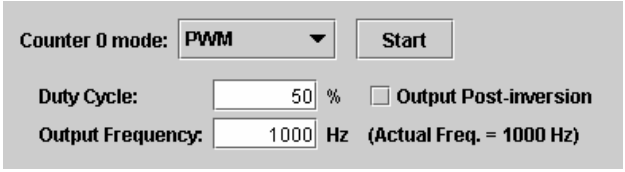


Figure 5-23. Example Bin Counter Controls



Example Pulse Width Modulation (PWM) controls

Figure 5-24. Example Pulse Width Modulation (PWM) Controls

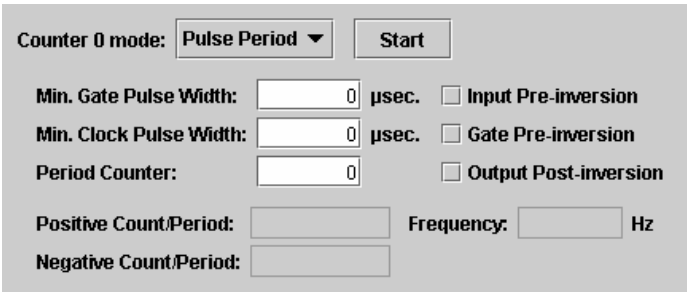


Figure 5-25. Example Pulse Period Controls

After setting the configuration for a counter, you can choose *Network>>Store Config* to store the settings on the device. Clicking **Start** will also write your configuration to the module.

Clicking the **Start** button for a counter will start that counter on the module.

The **Start** button will turn into a **Stop** button, and the other controls for that counter will become disabled until you click **Stop**.

While the module is running, you can choose *Network>>Read Input Data* to retrieve runtime values from the counter, which will display in the read-only text field(s) of the counter control panel.

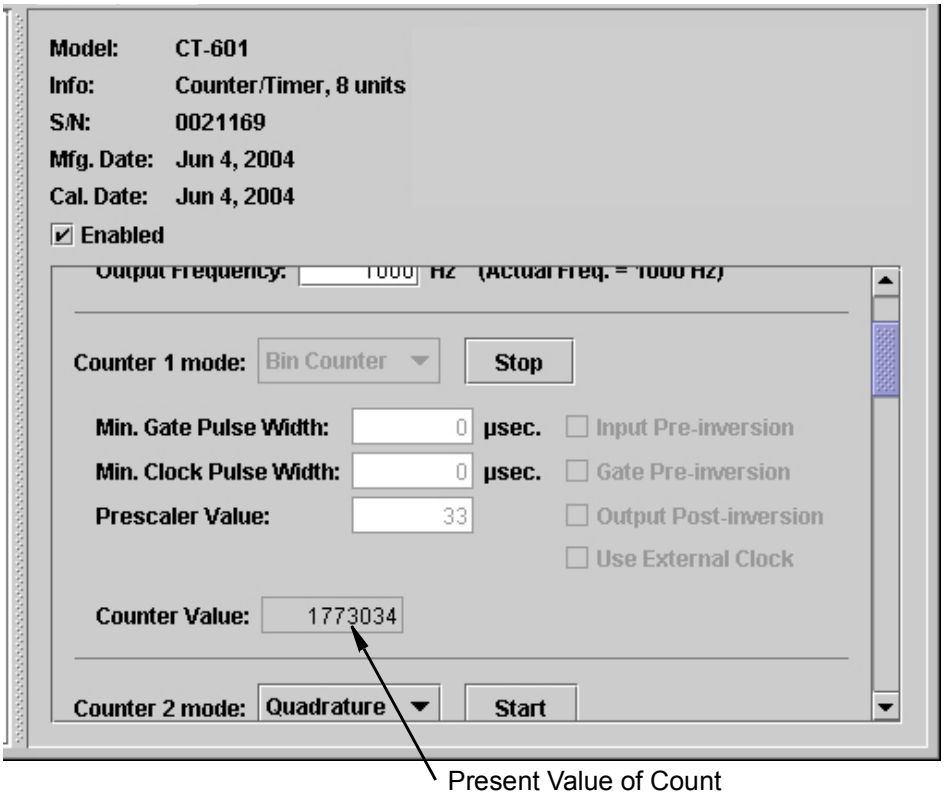


Figure 5-26. Example of Started Counter

Chapter 6 The DNR-MIL-x CPU

This chapter describes the device architecture of the DNR-MIL-x CPU module. This is commonly referred to as the Input Output Module (IOM). Note that I/O boards used for specific types of data acquisition are not described in this chapter.

6.1 DNR-MIL-x CPU/NIC Overview

One slot of a DNR-MIL-x RACKtangle™ enclosure is occupied by the DNR-MIL-x CPU module.

The DNR-MIL CPU is available in a standard, -02, -03, or -11 option. Each option aligns with the respective DNR-MIL-x system option that it is installed in (see Section 1.2 on page 3).

The CPU module includes the selected processor (8347, 8347E, or SoloX), peripheral devices (USB 2.0, RS-232, NIC, etc) for use with a Gigabit Ethernet communication network, and an internal 66 MHz 32-bit common logic interface bus. The NICs are copper (1000BaseT) interfaces. The CPU module has a serial debug port used for configuration and also two USB 2.0 ports (controller and slave) for general purpose use when in UEIPAC mode. LEDs on the front panel of each indicate the current operating status of the device. Refer to **Table 6-1** for a list of CPU board components,

6.2 Device Architecture of CPU/NIC Module

The processor on the CPU module depends on the DNR-MIIL-x system option:

- Standard and -02 systems: NXP-Freescale PowerPC MPC8347 32-bit 400 MHz processor
- -03 systems: MPC8347E 32-bit 400 MHz processor
- -11 systems: NXP i.MX6 SoloX ARM® 32-bit processor composed of the Cortex®-A9 and Cortex-M4 cores. The UEIPAC SoloX's Cortex-A9 core runs at a maximum of 1 GHz while the Cortex-M4 core runs at a maximum of 200 MHz. The more powerful A9 core is available for user programs. The M4 core runs UEI written firmware dedicated to direct access of the various DNx I/O boards.

The processor controls the following components:

Table 6-1 Components in DNR-MIL-x CPU Board (DNR-MIL-x Series)

Item	Description
Primary Network Interface (NIC1)	This interface provides communication between the DNR-MIL-x system and the primary LAN network. For copper 1000BASE-T networks the twisted-pair Cat5/6/7 cable must be shorter than 100 meters (328 feet) between nodes. Please contact Support if these cable lengths pose a challenge.
Diagnostic Network Interface (NIC2)	Identical to NIC1, but this port is set by default to monitor the health of the DNR-MIL-x-x system during operation as a separate diagnostic port. This port may also be assigned as the primary Ethernet port if NIC1 is not available for use; the NIC1/NIC2 ports may be set-up to provide redundant Ethernet connectivity.
RS-232 Serial Interface	This interface provides a serial communication link between the DNR-MIL-x system and a standard RS-232 serial terminal that can be used to debug.
CPU Reset Interface	This interface is disabled by default, but can be software enabled to reset the CPU using an external switch.
USB 2.0 Interface	USB ports A and B are intended for future use and are not software supported at present in all modes.
Flash Memory[1]	• DNR-MIL systems provide 32 MB of flash memory. • DNR-MIL-x-02 systems provide 32 MB of flash memory. • DNR-MIL-x-03 systems provide 128 MB of flash memory. • DNR-MIL-x-11 systems provide 8 GB of flash memory.
SDRAM[1]	• DNR-MIL systems provide 256 MB of SDRAM. • DNR-MIL-x-02 systems provide 256 MB of SDRAM. • DNR-MIL-x-03 systems provide 256 MB of SDRAM. • DNR-MIL-x-11 systems provide 1 GB of SDRAM.
SYNC Port[2]	A high-speed system-to-system synchronization connector permits triggers or clocks to be shared among multiple systems. Two systems may be connected together directly and larger groups may use the SYNC interface to share timing signals among many racks and systems. The trigger and clock inputs will accept signals from standard digital logic that is powered in the range of 3.3V to 5V. The inputs also have internal pull-up resistors to an internal 5V supply, making the inputs also compatible with a low-side drive open-collector output. The Sync and trigger outputs have 5V logic levels. The sync connector's ground and 5V power connections are provided by its own isolated DC-DC converter.
IEEE-1588 Synchronization Support[2]	DNR-MIL-x-02, -03, and -11 systems support IEEE-1588 synchronization in hardware.

Table 6-1 Components in DNR-MIL-x CPU Board (DNR-MIL-x Series)

Item	Description
Solid state hard drive	Optional solid state hard drive (only supported on UEIPAC, UEISIM, UEIModbus, and UEIOPCUA deployments -- 8GB, 16GB, 64GB).
LEDs	The operating conditions indicated by the front panel LEDs are: • Aux2: “heartbeat” blinks if CPU has not halted • Aux1: ON when there is activity on either network interface • Fault: ON when temperature, power, or bus are in the error range • Power Good: ON when the unit is receiving input power
Watchdog Timer With Real-time Clock (Battery Backed)	The DNR-MIL-x system includes a programmable watchdog timer with battery-backed real-time clock.

1.RAM and flash memory are not user-accessible for non-UEIPAC applications (hosted deployments). Portions of RAM and flash are available for UEIPAC-based systems (stand-alone deployment). See UEIPAC documentation for more information
2. 1PPS and IEEE-1588 synchronization support is described in the PowerDNx 1PPS Sync Interface Manual.

Not all components are available for control from the CPU. The CPU can program flash memory, set the LEDs, set up the watchdog timer, set the real-time clock and use 256 bytes of backed-up memory in the watchdog timer chip. All functions are available at the firmware level only (described in iom.c/iom.h).

6.3 DNR-MIL-x CPU/NIC Pinouts

Refer to Section 2.8 on page 14 for DNR-MIL-x pinouts, connectors and cables.

Chapter 7 CPU Programming in PowerDNA Mode

7.1 Overview

This chapter describes information for programming CPU module-specific functions for PowerDNA hosted deployments:

- Memory Map Overview (Section 7.2)
- Startup Sequence (Section 7.3)
- Setting and Reading CPU Core Parameters via Serial Port (Section 7.4)

Example code and application development documentation, (e.g., getting started guides, API reference, synchronization documentation) are provided with the installation.

NOTE: PowerDNA hosted mode is only available for DNR-MIL-x, DNR-MIL-x-02, and DNR-MIL-x-03 systems, which use the 8347/8347E CPU. Therefore, the SoloX CPU (option -11) is not covered in this chapter. For information about programming the CPU modules in stand-alone deployments, please refer to the “UEIPAC SoloX Hardware Manual” and “UEIPAC SoloX Software Manual” for the SoloX CPU or the “UEIPAC Software Manual” for the 8347/8347E CPUs.

7.2 Memory Map Overview

This section describes the memory maps for the DNR-MIL-x CPU modules. DNR-MIL-x CPU board versions align with DNR-MIL-x product versions. For a list of DNR-MIL-x Series product versions, refer to Section 1.2 on page 3.

Table 7-1 Memory Map for DNR-MIL CPU (DNR-CPU-1GBM)

Device	Start Address	End Address	Size	Description
SDRAM	**0x0**	**0xFFFFFFF**	**256MB**	**SDRAM_ADDRESS**
Exception table	0x0	0x3000	12 kB	Processor address map
CPU card address	0xA00E0000	0xA00EFFFC	64 kB	EXT_SRAM_ADDRESS
Processor RAMBAR	0xE0000000			
Module – CS2	0xA0000000	0xA00FFFFC	1 MB	EXT_DEV_ADDRESS2
Module – CS3	0xA0100000	0xA01FFFFC	1 MB	EXT_DEV_ADDRESS3
Flash (Linux kernel)	0xFE000000	0xFF7FFFFF	up to 24 MB	Linux kernel
Flash (firmware)	0xFF800000	0xFFEFFFFF	up to 7 MB	Firmware
Flash (U-Boot)	0xFFF00000	0xFFF5FFFF	approximately 320 kB	U-Boot
Flash (parameters)	0xFFF60000	0xFFFFFFFF	64 kB	Parameters (1 sectors)

Table 7-2 Memory Map for DNR-MIL-x-02 CPU (DNR-CPU-1GBM-02)

Device	Start Address	End Address	Size	Description
SDRAM	**0x0**	**0xFFFFFFF**	**256MB**	**SDRAM_ADDRESS**
Exception table	0x0	0x3000	12 kB	Processor address map
CPU card address	0xA00E0000	0xA00EFFFC	64 kB	EXT_SRAM_ADDRESS
Processor RAMBAR	0xE0000000			
Module – CS2	0xA0000000	0xA00FFFFC	1 MB	EXT_DEV_ADDRESS2
Module – CS3	0xA0100000	0xA01FFFFC	1 MB	EXT_DEV_ADDRESS3
Flash (Linux kernel)	0xFE000000	0xFF7FFFFF	up to 24 MB	Linux kernel
Flash (firmware)	0xFF800000	0xFFEFFFFF	up to 7 MB	Firmware
Flash (U-Boot)	0xFFF00000	0xFFF5FFFF	approximately 320 kB	U-Boot
Flash (parameters)	0xFFF60000	0xFFFFFFFF	64 kB	Parameters (1 sectors)

Table 7-3 Memory Map for DNR-MIL-x-03 CPU (DNR-CPU-1GBM-03)

Device	Start Address	End Address	Size	Description
SDRAM	**0x0**	**0xFFFFFFF**	**256MB**	**SDRAM_ADDRESS**
Exception table	0x0	0x3000	12 kB	Processor address map
CPU card address	0xA00E0000	0xA00EFFFC	64 kB	EXT_SRAM_ADDRESS
Processor RAMBAR	0xE0000000			
Module – CS2	0xA0000000	0xA00FFFFC	1 MB	EXT_DEV_ADDRESS2
Module – CS3	0xA0100000	0xA01FFFFC	1 MB	EXT_DEV_ADDRESS3
Flash (Linux kernel)	0xF8000000	0xFF7FFFFF	up to 120 MB	Linux kernel
Flash (firmware)	0xFF800000	0xFFEFFFFF	up to 7 MB	Firmware
Flash (U-Boot)	0xFFF00000	0xFFF5FFFF	approximately 320 kB	U-Boot
Flash (parameters)	0xFFF60000	0xFFFFFFFF	64 kB	Parameters (1 sectors)

Module Address Space (0xA0000000 – 0xA00FFFFC and 0xA0100000 – 0xA01FFFFC). The first address range is dedicated for devices located on the CS2 line and it accommodates sixteen modules with 64k memory map each. The second address range is designated for fast devices located in the CS3 line and it accommodates fifteen devices with 16MB memory map each.

7.3 Startup Sequence

After reset, the processor reads the boot-up sequence located at the address in Table 6-1. This command sequence is a part of U-Boot code. U-Boot initializes all major subsystems of the CPU core module including DDRAM and Ethernet interface.

After initializing, U-Boot performs a command list stored in its environment sector under the `bootcmd` entry. A standard command to launch DNR-MIL-x firmware is "`go 0xff800100`". U-Boot then gives up control to the firmware code located at 0xFF800100. Firmware self-expands into the DDRAM, initializes the exception table, and starts execution.

7.4 Setting and Reading CPU Core Parameters via Serial Port

CPU Core Module (CM) parameters can be set using the serial interface and entering commands at the `DQ>` prompt, or they can be set using DaqBIOS calls by running an application on the host PC.

To set parameters using the serial interface, first connect your host PC to the DNR-MIL-x by following the procedure in "Initial Boot-up " on page 34, starting at step 2.

Once connected, press ENTER and the DNR-MIL-x should respond with a "`DQ>`" prompt (this is the firmware prompt).

- If you see a Linux shell prompt ("`#`" for root), then you are running a UEIPAC version of the DNR-MIL-x (refer to the UEIPAC manual).
- If you see a "`=>`" prompt, you are still in U-Boot.

Once you see the "`DQ>`" prompt, you can type "`help <Enter>`" to receive the list of all available commands.

NOTE: The following sections provide descriptions of serial parameters applicable to the hosted DNR-MIL-x product versions. For a list of DNR-MIL-x Series product versions, refer to Section 1.2 on page 3.

7.4.1 Help Command

The **`help`** command provides a list of available commands:

```
DQ> help

    help Display this help message      help
     set Set parameter                  set option value
    show Show parameters                show
   store Store parameters (flash)       store
    flrd Re-read flash (flash)          flrd
      mw Write wr <addr> <val> [width,b] mw
      mr Read rd <addr> [width,b] [size] mr
    time Show/Set time                  time [mm/dd/yyyy] [hh:mm:ss]
    pswd Set password                   pswd {user|su}
      ps Show process state #           ps [value]
    test Test something                 test [test number]
   simod System Init/Module Cal         simod [routine]
 default Default parameters             default
   reset Reset system                   reset [all]
  dqping Send DQ_ECHO to <mac addr>     dqping
    mode Set current mode              mode {init|config|oper|shutdown} [ID]
     log Display log content            log [start [end]] -1 = clear
    logf Find entry in the log          logf marker [start [end]]
     ver Show firmware version          ver [all]
  devtbl Show all devices/layers        devtbl [logic|verbose]
 netstat Show network statistics        netstat
     pdj Print device object            pdj <devno> cl
      sd SD Card Commands               sd <command> <arguments>
    stat Display status                 stat [log]
     nif Display nif object             nif
   clear Clear terminal                 clear
```

7.4.2 Show System Parameters Command

The **`show`** command is one of the most frequently used commands. `show` provides a list of DNR-MIL-x system parameters:

```
DQ> show

        name: "IOM-12345 "
       model: 3212
      serial: 0162789
      option: 0001
        fwct: 1.2.0.0
         mac: 00:0C:94:02:7B:E5
         srv: 192.168.100.2
          ip: 192.168.100.100 (1Gbit)
     gateway: 192.168.100.1
     netmask: 255.255.255.0
        mac2: 00:0C:94:F2:7B:E5
        srv2: 192.168.100.102
         ip2: 192.168.100.102 (DOWN)
    gateway2: 192.168.100.1
    netmask2: 255.255.255.0
         udp: 6334
     license: "▒"
    bond prm: bonding mode: FFFFFFFF
    Manufactured 7/27/2016
    Calibrated 7/27/2016
```

To change parameters, use the “`set`” command (type `set` <Enter> for “`set`” command syntax).

7.4.3 Set and Store Commands

The **set** command allows you to change DNR-MIL-x system parameters and the **store** command allows you to save them to system memory (flash).

Typing `set <Enter>` provides a list of parameter names that can be changed.

```
DQ> set
Enter user password > ********

Valid 'set' options:
        name: <Device name>
       model: <Model id>
      serial: <Serial #>
      option: <Option>
        fwct: <autorun.runtype.portnum.umports>
         mac: <ethernet address port 1>
         srv: <Default IP address port 1>
          ip: <IOM IP address port 1>
     gateway: <gateway IP address port 1>
     netmask: <netmask port 1>
        mac2: <ethernet address port 2>
        srv2: <Default IP address port 2>
         ip2: <diagnostic port IP address>
    gateway2: <diagnostic port gateway IP>
    netmask2: <diagnostic port netmask>
         udp: <udp port (dec)>
     license: license string
    bond prm: license string
```

NOTE: The **set** command may require a password. The default password for DNR-MIL-x systems is "`powerdna`".

The following are examples of setting DNR-MIL-x parameters:

- To set a new Primary IP address (NIC1), type:
  `DQ> set ip 192.168.1.10`
- To set a new Secondary Diagnostic Port IP address (NIC2), type:
  `DQ> set ip2 192.168.100.3`

Other parameters can be changed the same way. Refer to Section 7.4.3.1 for more information about each of the **set** parameters.

Once parameters are set, you must store them into non-volatile flash memory:

```
DQ> store
CRC: crc=0xDB097048 flcrc=DB097048
Flash: 1272 bytes of 1272 stored! CRC=0xDB097048
Old=0xC4F8C173
Xflash: 28 bytes CRC=35AA034B
Configuration stored
```

After parameters are stored, reset the firmware.

7.4.3.1 Setting Parameters Via Serial Interface

Refer to **Table 7-4** below for descriptions of DNR-MIL-x system parameters that can be read or modified with the `set` command.

Table 7-4 `Set` Parameters

Set Parameter <Argument>	Description
`name <Device name>`	Sets the device name (up to 32 characters)
`<model>`	Device model (factory programmed, do not change). The valid value is 0x3212.
`<serial>`	DNR-MIL-x serial number (factory programmed, do not change)
`<mac or mac2>`	DNR-MIL-x MAC Ethernet address (factory programmed, do not change)
`fwct <autorun.runtype.portnum.umports>`	Defines the behavior of the U-Boot upon boot-up. The following are valid values for each field. • for "`autorun`": 1 - copy firmware to SDRAM memory location and execute from there • for "`runtype`" for the DNR-MIL-x • for "`portnum`" and "`umports`" should be 0 (zero)
`srv <Host IP address>`	Sets the host IP address. This parameter is ignored when the DNR-MIL-x system is used over the UDP protocol or from the host
`ip <IOM IP address>`	Specifies the IOM primary IP address (NIC1). This is a critical parameter the user must change to allow the DNR-MIL-x system to be visible on the network. The DNR-MIL-x responds to every UDP packet containing a DaqBIOS prolog sent to this address. Since the current release does not support DHCP on hosted deployments, the user should set up the IP address.
`gateway <gateway IP address>`	Specifies where the DNR-MIL-x (NIC1) should send an IP packet if a requested IP packet exists outside of the DNR-MIL-x network (defined by the network mask).
`netmask <network mask>`	Specifies what type of subnet the DNR-MIL-x (NIC1) is connected to. The factory sets netmask to Type C IP network – 254 nodes maximum
`srv2 <Host IP address>`	Sets the host IP address for connection with the IOM diagnostic (secondary) port (NIC2).
`ip2 <IOM IP address>`	Specifies the IOM diagnostic (secondary) IP address (NIC2).
`gateway2 <gateway IP address>`	Specifies the IOM diagnostic (secondary) gateway (NIC2).
`netmask2 <network mask>`	Specifies the IOM diagnostic (secondary) subnet mask (NIC2).

7.4.4 Reset DNR-MIL Command

The **`reset`** command performs a physical reset of the CPU and initiates the full startup sequence on the DNR-MIL-x system:

```
DQ> reset
Stopping DaqBIOS

U-Boot 1.1.3 (PowerDNA 8347 3.2.4) (Mar 24 2014 - 12:31:23) MPC83XX

Clock configuration:
```

<...many U-Boot messages deleted...>

```
Net:   Freescale TSEC0:- PHY is Realtek RTL8212 (1cc912)
PHY is Freescale TSEC0
W:9140 rg:0 Gig-E controller found
W:1140 rg:0 EthController Freescale TSEC0
Hit any key to stop autoboot:  0
## Starting application at 0xFF800100 ...
Welcome to PowerDNA!
PowerDNA (C) UEI, 2001-2017. Running PowerDNA Firmware on MPC8347A
Built on 13:05:16 Aug 23 2017
RAM size:128MB Flash size:32MB
Initialize uC/OS-II (Real-Time Kernel v.280)
CM-4 PPC8347 detected
6 devices detected

 Address   Irq  Model Option  Phy/Virt  S/N    Pri DevN
-------------------------------------------------------
0xA0000000   2    207    1    phys   0165992     10   0
0xA0010000   2    650    1    phys   0154839     20   1
0xA0020000   0    364    1    phys   0170276     30   2
0xA0030000   2    217    1    phys   0153841     40   3
0xA00C0000   2     20    1    phys   0162268     50   4
0xA00D0000   3     40    1    phys   0162861     60   5
0xA00E0000   3      5    1     cpu   0162789      0  14
-------------------------------------------------------
Current time: 10:19:54 08/30/2017
Starting filesystem...  (H)
SD card is not present.
Power DNA version 4.10.0 release build 3
Built on 13:05:16 Aug 23 2017
396MHz MPC8347 DCache:32k uC/OS v.280 is running

Enter 'help' for help.

DQ>
```

7.4.5 Password Command

Some commands (such as `mr, mw, set,` and `store`) require entering a user password. Once the password is entered, these commands become enabled until firmware reset.

There are two levels of password protection available. The first is user level and the second is super-user level. Super-user level is currently used only for updating firmware over the Ethernet link.

- `DQ> pswd user` sets up a user level password. First, you'll be asked about your old password and then (if it matches) to enter the new password twice.
- `DQ> pswd su` sets up super-user level password. First, you'll be asked about old super-user password and then (if it matches) to enter the new super-user password twice.

DNR-MIL-x systems come with both default passwords set to "`powerdna`".

Some DaqBIOS commands require clearing up user or super-user password. Use **DqCmdSetPassword()** before calling these functions. The PowerDNA API Reference Manual notes which functions are password-protected.

7.4.6 Display Table of Installed Boards & Logic Version Command

The **`devtbl`** command is another of the more frequently used commands. This command displays all I/O boards found and initialized by firmware along with assigned device numbers.

```
DQ> devtbl
```

The **`devtbl`** command with the **`logic`** option displays the CPU logic version on each installed I/O board:

```
DQ> devtbl logic
```

The **`devtbl`** command with the **`verbose`** option displays detailed information about each installed I/O board:

```
DQ> devtbl verbose
```

7.4.7 Display Power Diagnostics Command

Typing **`simod 5`** at the serial prompt displays diagnostic information about the DNR-MIL-x CPU boards. This diagnostic information includes actual voltage readings on each of the 2.5V, 24V, 1.2V, 3.3V, and 1.5V supplies, as well as actual temperature and current measurements.

```
DQ> simod 5
```

7.4.8 Memory Test/ Memory Clear Command

Typing **`simod 7`** performs a memory test on the UEI CPU address space.

The test writes standard memory test bit patterns to each memory location and then reads each location back and verifies. At the end, it reports any bit mismatches.

Note that this memory test writes over any content in that memory space; therefore, it can be used to clear memory, as needed.

```
DQ> simod 7
Memory test/clear
Clear memory and reboot? y/[n]>n
CPU layer memory test
Start addr=0x00200000  End addr=0x07FFFFFC (125MB)
Total errors: 0
DQ>
```

Typing "`y`" after "`Clear memory and reboot? y/[n]>`" causes the chassis to automatically reboot.

```
DQ> simod 7
Memory test/clear
Clear memory and reboot? y/[n]>y
CPU layer memory test
Start addr=0x00200000  End addr=0x07FFFFFC (125MB)
ADDR: 0x04C00000 (76MB) errors=0
```

<...memory test completes and then system reboots...>

7.4.9 Monitor CPU and Pbuf Usage Command

Entering **`simod 15`** at the serial command prompt causes the CPU and packet buffer load to continuously print to the serial console.

`simod 15` can be used to monitor the DNR-MIL-x serial port while your application is sending and receiving control words and data over Ethernet.

```
DQ> simod 15
Printing statistics
+cpu:1 pbuf:avail:576 used:20 max:20 err:0
+cpu:12 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
+cpu:8 pbuf:avail:576 used:20 max:20 err:0
```

7.4.10 Clock Command

The **`time`** command shows and sets up the date and time on the DNR-MIL-x system:

```
DQ> time
Current time: 14:56:17 09/01/2017
```

To set up time of the time of day, enter:

```
DQ> time 17:40:00
```

To set up date, enter:

```
DQ> time 11/03/2017
```

Date and time are stored in the battery-backed real-time clock chip.

Appendix A

A.1 Configuring a Second Ethernet Card Under Windows 7

To configure an Ethernet card for your system, use the following procedure:

A. Set Up Your Ethernet Network Interface Card (NIC).
If you already have an Ethernet card installed, skip ahead to the next section, “Configure TCP/IPv4”.

If you have just added an Ethernet card, to install it, do the following:

STEP 1: From the *Start* menu, and select *Control Panel*.

STEP 2: Under *Printers and Other Hardware*, click *Add a device* and follow the on-screen instructions.

NOTE: We recommend that you allow Windows to search for and install your Ethernet card automatically. If Windows does not find your Ethernet card, you will need to install it manually by following the manufacturer's instructions.

Once your Ethernet card has been installed, continue to the next section.

B. Configure TCP/IPv4.

STEP 1: From the *Start* menu, select *Control Panel*.

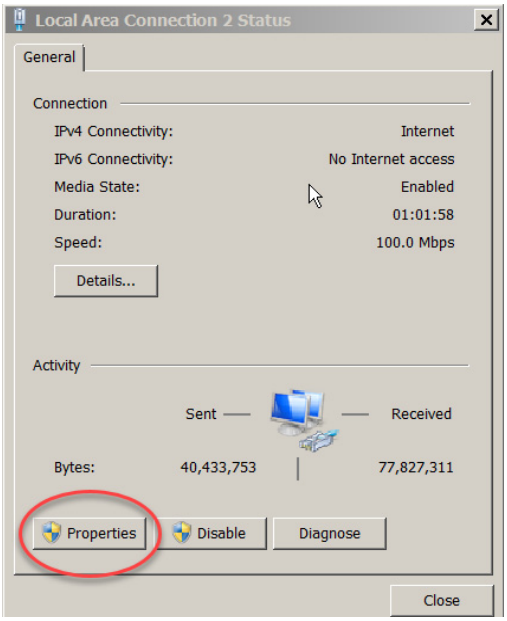
STEP 2: In the Control Panel window, click *Network and Internet*.

STEP 3: In the Network and Internet window, click *Network and Sharing Center*.

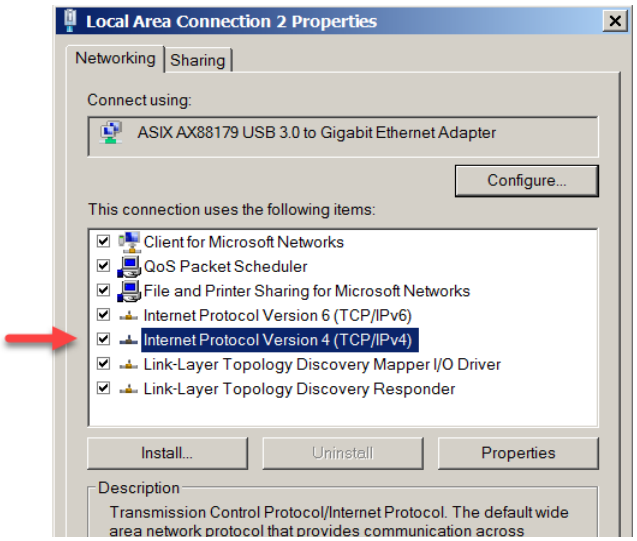
STEP 4: In the left sidebar of the Network and Sharing Center window, click *Change adapter settings*.

STEP 5: Double-click the icon for the network interface you are connecting as your second NIC. This is typically under a *Local Area Connection* heading.

STEP 6: In the Local Area Connection Status window, click **Properties**:

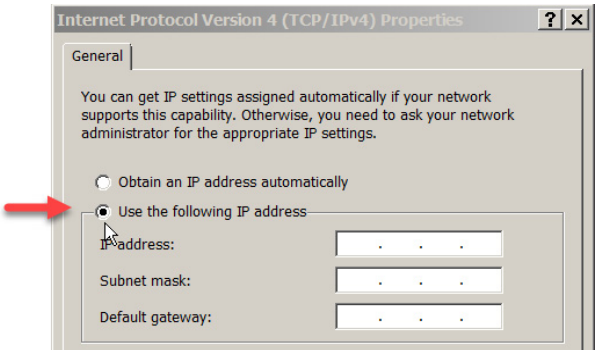


STEP 7: In the Local Area Connection Properties window, verify the Networking tab is selected, and double-click *Internet Protocol Version 4 (TCP/IPv4)*.



STEP 8: If Internet Protocol (TCP/IPv4) is not listed, click **Install** and follow directions on the screen.

STEP 9: Click the *Use the following IP address* button (see Figure below). Note any addresses listed in the *IP Address*, *Subnet Mask*, *Default Gateway*, *Preferred DNS Server* or *Alternate DNS Server* fields. You may want to re-enter them later to reconfigure your PC, if needed.



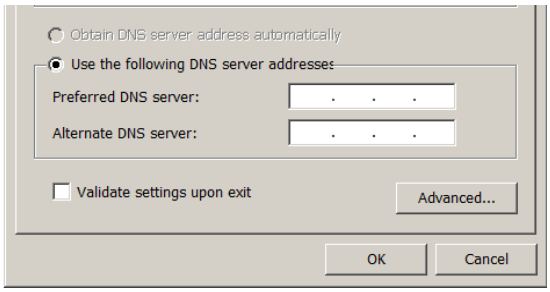
In the *IP address* field, type the IP address for the host PC NIC port (e.g., `192.168.100.1)`.

In the *Subnet mask* field, type `255.255.255.0`.

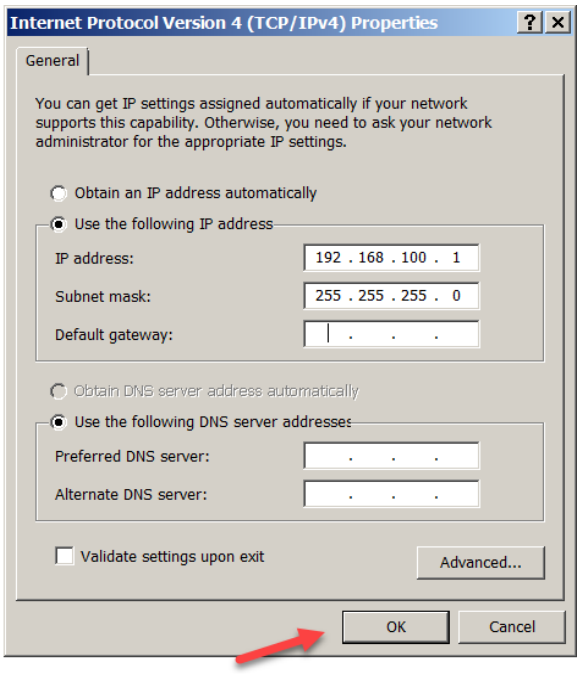
Leave the *Default Gateway* field blank.

NOTE: In the above example, setting the host PC NIC address to 192.168.100.1 with a subnet mask of 255.255.255.0 allows the host PC to communicate with components having IP addresses from 192.168.100.2 through 192.168.100.254 via that NIC port. All UEI cubes and racks on this network will need to have IP addresses unique and in that range. (The default IP address of the UEI RACKtangle / HalfRACK is 192.168.100.2.)

STEP 10: Select *Use the following DNS server addresses* and verify the *Preferred DNS server* fields and the *Alternate DNS server* fields are blank.



STEP 11: Click **OK** in the *TCP/IPv4 Properties* window (see figure below).



STEP 12: Click **OK** in the *Local Area Connection 2 Properties* window, and click **Close** in the *Local Area Status* window.

STEP 13: **Close** the *Control Panel* window.

For instructions on setting the IP address, subnet mask, and default gateway on a UEI chassis, refer to "IP Address Overview & Update Procedures" on page 35.