United Electronic Industries

The High-Performance Alternative

DNx-AI-212

—

User Manual

12-Channel, 24-bit, Simultaneously Sampling, Differential Analog Input Board for Thermocouples with Cold-Junction Compensation for the PowerDNA Cube and PowerDNR RACKtangle

October 2015

PN Man-DNx-AI-212-1015

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Chapter 1 Introduction

This document outlines the feature set and use of the DNx-AI-212 board. The AI-212 is a 12-channel analog input module for the PowerDNA I/O Cube (DNA-AI-212) and the DNR-1G HalfRACK and RACKtangle chassis (DNR-AI-212).

1.1 Organization of Manual

This AI-212 User Manual is organized as follows:

- **Introduction**
  This chapter provides an overview of DNx-AI-212 Analog Input Board features, device architecture, connectivity, and logic.
- **Programming with the High-Level API**
  This chapter provides an overview of the how to create a session, configure the session, and interpret results with the Framework API.
- **Programming with the Low-Level API**
  This chapter is an overview of low-level API commands for configuring and using the AI-212 series layer.
- **Appendix A - Accessories**
  This appendix provides a list of accessories available for use with the DNx-AI-212 board.
- **Index**
  This is an alphabetical listing of the topics covered in this manual.

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Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:

Tips are designed to highlight quick ways to get the job done or to reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.

CAUTION! *Caution advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

Text formatted in **bold** typeface generally represents text that should be entered verbatim. For instance, it can represent a command, as in the following example: “You can instruct users how to run setup using a command such as **setup.exe**.”

Text formatted in `fixed` typeface generally represents source code or other text that should be entered verbadim into the source code, initialization, or other file.

Examples of Manual Conventions

Before plugging any I/O connector into the Cube or RACKtangle, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

Usage of Terms

Throughout this manual, the term “Cube” refers to either a PowerDNA Cube product or to a PowerDNR RACKtangle™ rack mounted system, whichever is applicable. The term DNR is a specific reference to the RACKtangle, DNA to the PowerDNA I/O Cube, and DNx to refer to both.

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1.2 The AI-212 Interface Board

The DNA-AI-212 and DNR-AI-212 are 12-channel, channel-to-channel and channel-to-chassis isolated, simultaneously sampling A/D boards compatible with UEI's popular Cube and RACKtangle chassis respectively. The DNA/DNR versions are electronically identical. The DNx-AI-212 features a ±2.048 V input range and 24-bit converters providing an input resolution of 0.24 µV.

One A/D per channel configuration allows simultaneous sampling at rates up to 2000 S/s each (24,000 S/s aggregate). The A/D per-channel configuration virtually eliminates input cross talk and channel settling time issues.

The DNx-AI-212 is an ideal, high accuracy thermocouple measurement device, offering offset and gain errors of less than 0.1°C on all standard thermocouples (including J, K, T, S, E, R). This accuracy combined with the channel-to-channel isolation makes the board a perfect solution for industrial temperature measurement, even when using non-isolated thermocouples.

Additionally, the DNx-AI-212 is designed to take advantage of the extremely accurate ADT 7420 digital temperature sensor which provides a dedicated CJC measurement. The CJC sensor is mounted externally on the DNA-STP-212 screw terminal panel. The software included will perform all required TC linearization and CJC compensation and return data in °C, °K, °F or °R when desired. An open thermocouple detection circuit has also been implemented.

Software included with the DNx-AI-212 provides a comprehensive yet easy to use API that supports all popular Windows programming languages as well as supporting programmers using Linux and most real-time operating systems including QNX, RTX, VXworks and more. Finally, the UEIDAQ Framework supplies complete support for those creating applications in data acquisition software packages such as LabVIEW, MATLAB/Simulink, DASYLab or any application which supports ActiveX or OPC servers.

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1.3 Features

The AI-212 layer has the following features:

- 12 fully differential analog input channels
- Simultaneous sampling (one A/D converter per channel)
- 24-bit resolution and ±2.048V input range for every analog input
- Built-in anti-aliasing filters
- Built-in 50, 60Hz rejection at <20S/s and 400 Hz at <160S/s
- Built-in CJC circuitry for thermocouple monitoring
- Channel-to-channel and channel-to-chassis isolation
- “Open” input wiring detection (detects unwired or burnt thermocouples)
- Protection against ESD, overvoltage, and overcurrent
- Weight of 120 g or 4.24 oz for DNA-AI-212; 630 g or 22.2 oz with PPC5

1.4 Specification

The technical specification for the DNx-AI-212 board are listed in **Table 1-1**. The measurements are provided at 20 samples per second unless otherwise noted.

Table 1-1. DNx-AI-212 Technical Specifications

Number of channels:	12 fully differential plus CJC
ADC resolution	24 bits
Sampling rate	up to 1800 samples/sec per channel 21,600 S/S board aggregate.
TC Measurement accuracy	See Table
Input bias current	< 100 pA typical (open TC source off)
Input offset	< 1 uV @ 25°C, (<3 µV -40°C to +85°C)
Gain error	±0.005 % (typical)
Input INL error	6 ppm typical, 15 ppm max
Input impedance	>5000 MΩ
Input range	±2.048 Volt (gain = 1)
Gains	1, 2, 4, 8, 16, 32, 64 (adjusted to optimise range for TC type selected)
Anti-Aliasing filtering	@47.6% of sample rate, ~100 dB/decade
50/60/400 Hz notch filtering	>70 dB at sample rate = 20 Hz or less
Common mode rejection	G=1: 90 dB, G=32: 125 dB (typical)
Chan to Chan crosstalk	< 0.5 µVrms
CJC Sensor type	ADT 7420, mounted on STP panel
Isolation	350 Vrms, chan-to-chan & chan-to-chassis
Power consumption	4 W max
Operating temp. (tested)	-40°C to +85°C
Operating humidity	95%, non-condensing
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500Hz, broadband random
Shock *IEC 60068-2-27*	50 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations

Thermocouple Type	**Max Error** (CJC 25°C), °C	**Max Error** (CJC -40 to 85°C), °C
B	±0.5	±0.8
C	±0.3	±0.6
E	±0.2	±0.5
J	±0.1	±0.4
K	±0.3	±0.6
N	±0.5	±0.8
R	±0.8	±1.1
S	±0.8	±1.1
T	±0.3	±0.6

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1.5 Comparison between AI-212 and AI-207 Layers

The following table is a side-by-side comparison of specification items for the AI-207 and the AI-212 analog input layers,

Table 1-2. AI-207 vs. AI-212

Item	AI-207	AI-212
No. and Type of Channels	16 differential analog voltage plus 1 CJC	12 differential analog voltage plus 6 CJC
A/D Converters	One	12 (one per channel)
Simultaneous Sampling	No	Yes
Sampling Rate	16 kHz aggregate max (1 kHz for 16 channels, 2 kHz for 8 channels, or 16 kHz for one channel)	2000 samples/second per channel, (24 kS/s aggregate)
CJC Selection	Channel 33, (adjustable gain)	Channel 24-30 (digital)
Available Gains	1, 2, 4, 8, 10, 20, 40, 80, 100, 200, 400, 800	1, 2, 4, 8, 16, 32, 64
Input Range	±10V (at gain 1), ..., ±12.5mV (at gain 800)	±2.048V (at gain 1), ..., ±32mV (at gain 64)
Resolution	18-bit	24-bit
Source Impedance Compatibility	Best with low impedance sources	Performs well with either low or high impedance sources
Isolation	350Vrms between inputs and chassis. Common ground for input channels.	350Vrms between input channel and chassis, and also between channels.
Pinout	37-pin	62-pin
Noise Filtering	Averaging engine that averages multiple samples to improve resolution	One FIR filter per channel. Data rates lower than 20S/s have 50/60/400Hz rejection.
Channel List	Specifies the channels that are to be read and the order in which to read them. Thus, the returned data is in the order that the channel list shows. If a channel needs to be sampled more often than other channels, the AI-207 allows the channel to be entered more than once in the channel list.	Specifies the channels that are to be read, but because they are simultaneously sampled, the sequential order concept does not apply. The AI-212 always returns data with the channels in numerical order regardless of what order they were in the channel list. A channel may only appear once in the channel list.

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1.6 Device Architecture

Figure 1-1 is a block diagram of the architecture of the AI-212 layer.

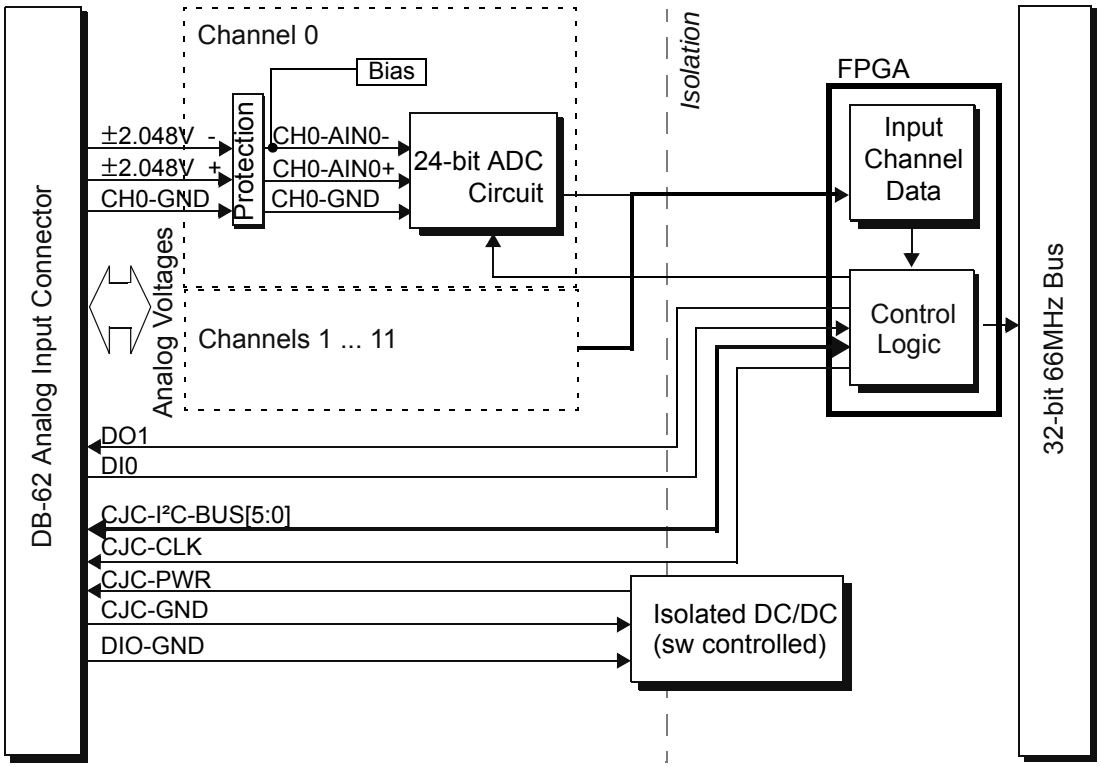

Figure 1-1. Block Diagram of the AI-212 Layer

Each AI-212 has twelve differential input channels designed for high-resolution analog voltage signal measurement. Each channel has 24-bit sampling resolution and maximum sampling rate of 1800 samples per second (one sample every 10msec), up to 21600 max samples per second per board. Each channel is individually isolated and uses dedicated components to avoid crosstalk/noise between channels and also ensures that one channel's failure (e.g. due to accidental over-voltage) does not affect other channels or the board.

Each channel's input consists of two analog and one ground line. The two analog lines carry your input voltages to be compared differentially against one other before being sampled digitally. Design was intended for thermocouples, but any voltage in the input range of +2.048V to -2.048V may also be used. The grounding line is provided to conveniently bias any input to channel ground. The analog input lines (AIN+/- in **Figure 1-1**) enter through the DB-62 connector pins into a SP724 protection circuit designed to redirect ESD / transients to the channel's isolated power supply before entering the A/D converter.

There is one 24-bit A/D converter per differential input channel. The converter is a highly-integrated, precision delta-sigma (ΔΣ) ADC with a range of ±2.048V and 24-bit resolution. It has a low-noise programmable-gain-amplifier (PGA) with selectable gains of 1 to 64. The ADC has hardware support for sensor burnout detect, a digital filter that settles in one cycle, and voltage bias for thermocouples (ON by default at AIN-; do not connect GND to AIN- when bias is on to avoid overloading bias circuit). Dedicating one single ADC for each input channel virtually eliminates input cross talk and channel settling time issues even when connected to high impedance signal sources.

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The converter control & data lines are wired (through an isolation barrier) to the board's main controller. The 350V isolation barrier ensures that disturbances or damage to one channel does not affect other channels, allowing the AI-212 to be an ideal solution for precise temperature measurement that must happen over long periods of time.

The main controller, in addition to containing the standard logic to provide DNx functionality, also contains AI-212 specific logic blocks with the role to send commands to all 12 channels, provide clocking & synchronization, receive & process data from channels, and provide sampled data and configuration access to the Cube & RACKtangle applications.

To perform data acquisition, the main controller sends a command to sample up to all 12 analog inputs simultaneously, receive 24-bit values from the conversion chip and provide them in output buffer. The output buffer is made accessible to standard DNx function calls and is read using software calls in either the UEIDAQ Framework (see Chapter 2) or the low-level API (see Chapter 3).

In addition to each channel's analog inputs *AIn+* and *AIn-*, described above, each layer also has a digital input, digital output line, and digital ground line. The digital lines are wired through a protection circuit directly into the main controller.

The DNA-AI-212 has hardware support for up to six ADT7420 temperature sensors for cold-junction-compensation (CJC). This sensor has 16-bit ±0.25°C accuracy and can provide data over the I²C bus protocol on any of the six CJC I²C lines to the main controller through the isolation barrier. Two sensors are built-in to the DNA-STP-AI-212 accessory terminal panel and are read every 250ms. This terminal panel offers a direct connection for thermocouples. External analog CJC sensors may be supported at a later time on this unit, contact UEI for details.

1.7 Indicators

A photo of the DNx-AI-212 unit is illustrated below.

The front panel has two LED indicators:

- RDY: indicates that the layer is receiving power and operational.
- STS: can be set by the user using the low-level framework.

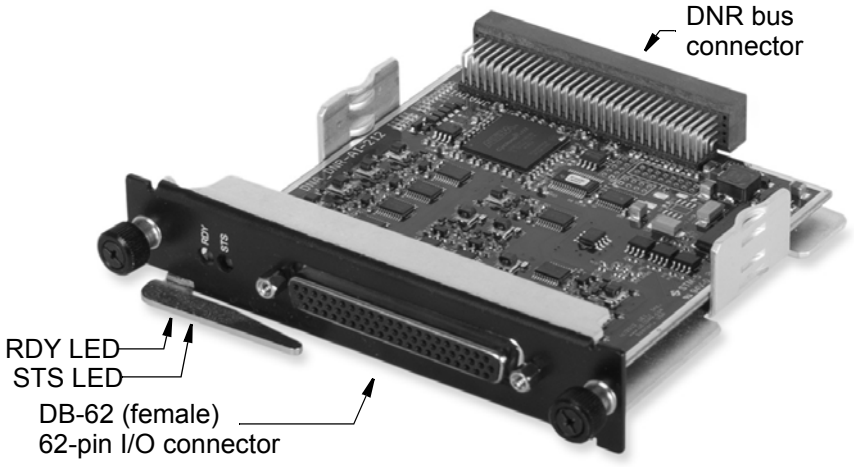
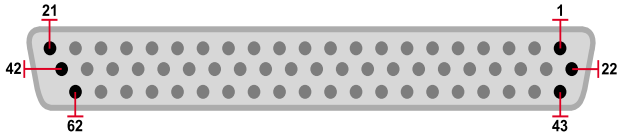


Figure 1-2. The DNR-AI-212 Analog-Input Layer

1.8 Layer Connectors and Wiring

Figure 1-3 below illustrates the pinout of the AI-212. The AI-212 layer uses a B-size 62-pin D-sub connector. The following signals are located at the connector:

- CH N+ — input channel N, differential mode.
  Use CH N- as TC return or analog input signal returns.
  Use CH N GND as ground for analog inputs requiring them (optional).
- +5V 50mA — provides power for CJC circuitry.
- CJC I²C 0 to 5 — digital I²C bus line for CJC inputs.
- DIO — digital I/O lines:
  - DI0: digital input line.
  - DO1: digital output line.
  - DGND: digital ground line (wired to channel's isolated ground).



Pin	*Signal*	*Pin*	*Signal*	*Pin*	*Signal*
1	CJC I²C 3	22	CJC I²C 4	43	CJC I²C 2
2	CJC I²C 0	23	CJC I²C 1	44	CJC I²C CLK
3	5 VDC (50 mA Max)	24	CJC Gnd	45	CJC Gnd
4	Rsvd for CJC Ain	25	CJC I²C 5	46	CH 11 Gnd
5	CH 11-	26	Rsvd	47	CH 11+
6	Rsvd	27	CH 10 Gnd	48	CH 10-
7	CH 9 Gnd	28	CH 10+	49	Rsvd
8	CH 9+	29	CH 9-	50	CH 8 Gnd
9	CH 8-	30	Rsvd	51	CH 8+
10	Rsvd	31	CH 7 Gnd	52	CH 7-
11	CH 6 Gnd	32	CH 7+	53	Rsvd
12	CH 6+	33	CH 6-	54	CH 5 Gnd
13	CH 5-	34	Rsvd	55	CH 5+
14	Rsvd	35	CH 4 Gnd	56	CH 4-
15	CH 3 Gnd	36	CH 4+	57	Rsvd
16	CH 3+	37	CH 3-	58	CH 2 Gnd
17	CH 2-	38	Rsvd	59	CH 2+
18	Rsvd	39	CH 1 Gnd	60	CH 1-
19	CH 0 Gnd	40	CH 1+	61	Rsvd
20	CH 0+	41	CH 0-	62	DIO 1
21	DIO 0	42	DIO Gnd		

Figure 1-3. Pinout Diagram of the AI-212 Layer

NOTE: If you are using a accessory panel with the AI-212, please refer to the Appendix for a description of the panel.

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1.8.1 Wiring guideline

You may wire analog signals within the ±2.048V range directly between the CH+ and CH- differential inputs. You must also connect either CH+ or CH- to GND over a resistor R. **Figure 1-4** shows a wiring diagram where CH- is used. Connecting CH+ or CH- to GND ensures that your input signal uses the same ground reference voltage as the ADC circuitry, rather than a “floating” ground. The resistor R reduces noise coming from GND and must have an impedence that is higher than that of the circuit to be measured (e.g. 10kΩ to 50kΩ). Not including a resistor (using only a shunt) between ground and an input is the equivalent of measuring in single-ended (rather than differential) mode. The Vbias source must be disabled (see page 13) when using this wiring scheme.

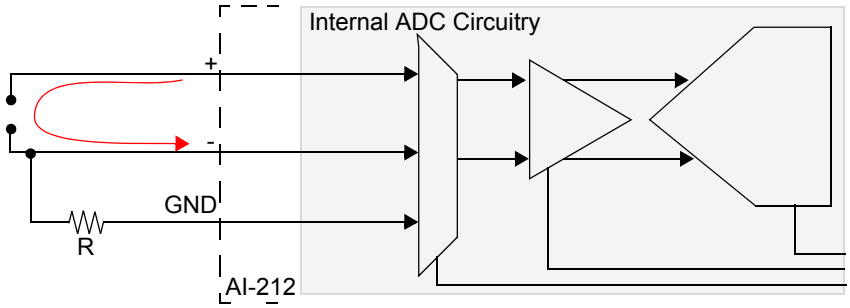

Figure 1-4. Wiring for differential signal or grounded thermocouple

Thermocouples should be wired directly to the CH+ and CH- inputs with GND unconnected and the fixed bias voltage source enabled as shown in **Figure 1-5**. You may add an RC analog input filter across the CH+ and CH- inputs as well. The bias voltage in **Figure 1-5** above is used to bring the voltage potential of the thermocouple outputs within the common-mode range of the AI-212 channel. Do not wire either CH+ or CH- input to GND either directrly or thorugh a resistor; any thermocouple input is floating regardless of whether it is grounded or not because each channel on the AI-212 is isolated from all other inputs. The bias voltage source can be enabled in software as shown in “Bias Flag” on page 13. The bias voltage output is internally set to half-way between the supply rails (1.5V minus half of the positive power supply voltage).

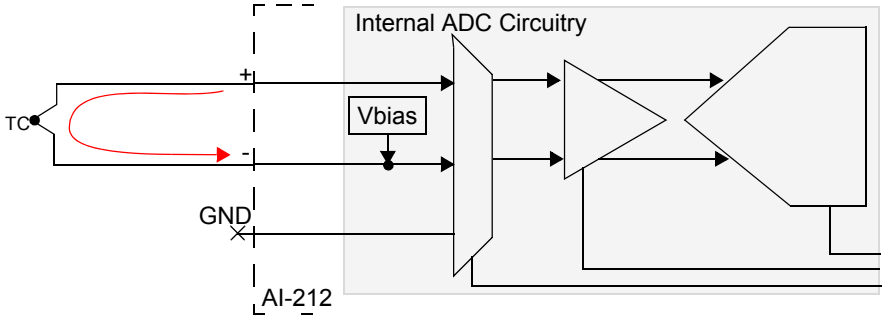

Figure 1-5. Wiring for isolated thermocouples on the AI-212

***NOTE: Improper wiring and failure to enable/disable the Vbias source are a common problem that results in incorrect measurement values**. Ensure that your wiring scheme is correct and that you have enabled or disabled Vbias.*

Chapter 2 Programming with the High Level API

This section describes how to control the DNx-AI-212 using the UeiDaq Framework High Level API.

UeiDaq Framework is object oriented and its objects can be manipulated in the same manner from different development environments such as Visual C++, Visual Basic or LabVIEW.

The following section focuses on the C++ API, but the concept is the same no matter what programming language you use.

Please refer to the “UeiDaq Framework User Manual” for more information on use of other programming languages.

2.1 Creating a Session

The Session object controls all operations on your PowerDNx device. Therefore, the first task is to create a session object:

```
// create a session object for input
CUeiSession aiSession;
```

2.2 Configuring the Resource String

UeiDaq Framework uses resource strings to select which device, subsystem and channels to use within a session. The resource string syntax is similar to a web URL:

```
<device class>://<IP address>/<Device Id>/<Subsystem><Channel list>
```

For PowerDNA and RACKtangle, the device class is **pdna**.

For example, the following resource string selects analog input lines 0,1,2,3 on device 1 at IP address 192.168.100.2: “pdna://192.168.100.2/Dev1/Ai0:3” as a range, or as a list “pdna://192.168.100.2/Dev1/Ai0,1,2,3”.

2.3 Configuring the Input

This section will show you how to configure your input for voltage measurement or thermocouple measurement.

2.3.1 Voltage Measurement

The gain applied on each channel is specified by using low and high input limits.

For example, the AI-212 available gains are 1, 2, 4, 8, 16, 32, 64 and the maximum input range is [-2.048V, +2.048V (gain = 1)].

To select the gain of 1, you need to specify input limits of [-2.048V, +2.048V]:

```
// Configure channels 0,1 to use a gain of 1 in differential mode
aiSession.CreateAIChannel(“pdna://192.168.100.2/Dev0/Ai0,1”,
                          -2.048, 2.048,
                          UeiAIChannelInputModeDifferential);
```

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2.3.2 Thermocouple Measurement

For thermocouples, use the object method `CreateTCChannel` which automatically handles temperature calculations, as follows:

```
// Configure channel 0 to 2, scaling for thermocouples;
// thermocouple Type K, degrees F°, using CJC built-in
// compensation from the STP-AI-212 board, in differential mode.

mySs.CreateTCChannel("pdna://192.168.100.2/Dev0/Ai0:2",
                     -2.048, 2.048,
                     ThermocoupleType.TypeK,
                     TemperatureScale.Fahrenheit,
                     ColdJunctionCompensationType.BuiltIn,
                     0, "",
                     AIChannelInputMode.Differential);
```

2.3.3 Additional channel parameter

You can configure an additional parameter using the channel object methods (or a property node under LabVIEW):

- **Bias**

The AI-212 features a programmable Bias feature that connects a mid-supply voltage to the Ain- terminal when enabled. This is useful when measuring floating (ungrounded) thermocouples.

The DNA-STP-AI-212 terminal panel provides a 100K resistance to ground, which negates the need for the bias feature.

You can enable or disable Bias on a channel as follows:

```
// Get channel 0 object

CUeiAIChannel* pChan =
               dynamic_cast<CUeiAIChannel*>(aiSession.GetChannel(0));

// Enable bias on channel

 pChan-> EnableBias (true);
```

Enabling the bias unnecessarily will not overload or damage the AI-212; but it will produce bad readings such as -800 degrees at room temperature.

2.4 Configuring the Timing

You can configure the AI-212 to run in simple mode (point by point) or high-throughput buffered mode (ACB mode), or high-responsiveness (DMAP) mode. In simple mode, the delay between samples is determined by software on the host computer. In buffered mode, the delay between samples is determined by the AI-212 on-board clock and data is transferred in blocks between PowerDNA and the host PC.

The following sample shows how to configure the simple mode. Please refer to the “UeiDaq Framework User’s Manual” to learn how to use other timing modes.

```
// configure timing of input for point-by-point (simple mode)

aiSession.ConfigureTimingForSimpleIO();
```

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2.5 Read Data

Reading data is done using *reader* object(s). There is a reader object to read raw data coming straight from the A/D converter. There is also a reader object to read data already scaled to volts or temperature unit.

The following sample code shows how to create a scaled reader object and read samples.

```
// create a reader and link it to the analog-input session's stream
CUeiAnalogScaledReader aiReader(aiSession.GetDataStream());
// the buffer must be big enough to contain one value per channel
double data[2];
// read one scan, where the buffer will contain one value per channel
aiReader.ReadSingleScan(data);
```

2.6 Cleaning-up the Session

The session object will clean itself up when it goes out of scope or when it is destroyed. To reuse the object with a different set of channels or parameters, you can manually clean up the session as follows:

```
// clean up the session
aiSession.CleanUp();
```

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Chapter 3 Programming with the Low-level API

The PowerDNA cube and PowerDNR RACKtangle and HalfRACK can be programmed using the low-level API. The low-level API offers direct access to PowerDNA DAQBios protocol and also allows you to access device registers directly.

However, we recommend that, when possible, you use the UeiDaq Framework High-Level API (see **Chapter 2**), because it is easier to use. You should need to use the low-level API only if you are using an operating system other than Windows.

For additional information about low-level programming of the AI-212, please refer to the PowerDNA API Reference Manual document under:

Start » Programs » UEI » PowerDNA » Documentation

Refer to the PowerDNA API Reference Manual on how to use low-level functions of AI-212, as well as others related to cube operation.

3.1 Bias Flag

A biasing circuit is available on the channel's AIN- pin and can be enabled or disabled. The circuit should be enabled for isolated thermocouple applications, or disabled for general purpose analog input or grounded thermocouple.

NOTE: *Failing to enable or disable the voltage bias source (Vbias) is a common problem that causes incorrect measurements.*

To enable the voltage bias circuit, logical-or (|) DQ_AI212_BIAS_ON_FLAG to the channel list entry for the channel you wish to disable as shown in sample code. Not adding this flag ensures that the voltage vias circuit will be disabled.

To get the status of the flag, use DQ_AI212_GET_BIAS_FLAG([channel list entry]).

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Appendix A

A. Accessories

The following cables and STP boards are available for the AI-212 layer.

DNA-CBL-62

This is a 62-conductor round shielded cable with 62-pin male D-sub connectors on both ends. It is made with round, heavy-shielded cable; 2.5 ft (75 cm) long, weight of 9.49 ounces or 269 grams; up to 10ft (305cm) and 20ft (610cm).

DNA-STP-62

The STP-62 is a Screw Terminal Panel with three 20-position terminal blocks (JT1, JT2, and JT3) plus one 3-position terminal block (J2). The dimensions of the STP-62 board are 4w x 3.8d x1.2h inch or 10.2 x 9.7 x 3 cm (with standoffs). The weight of the STP-62 board is 3.89 ounces or 110 grams.

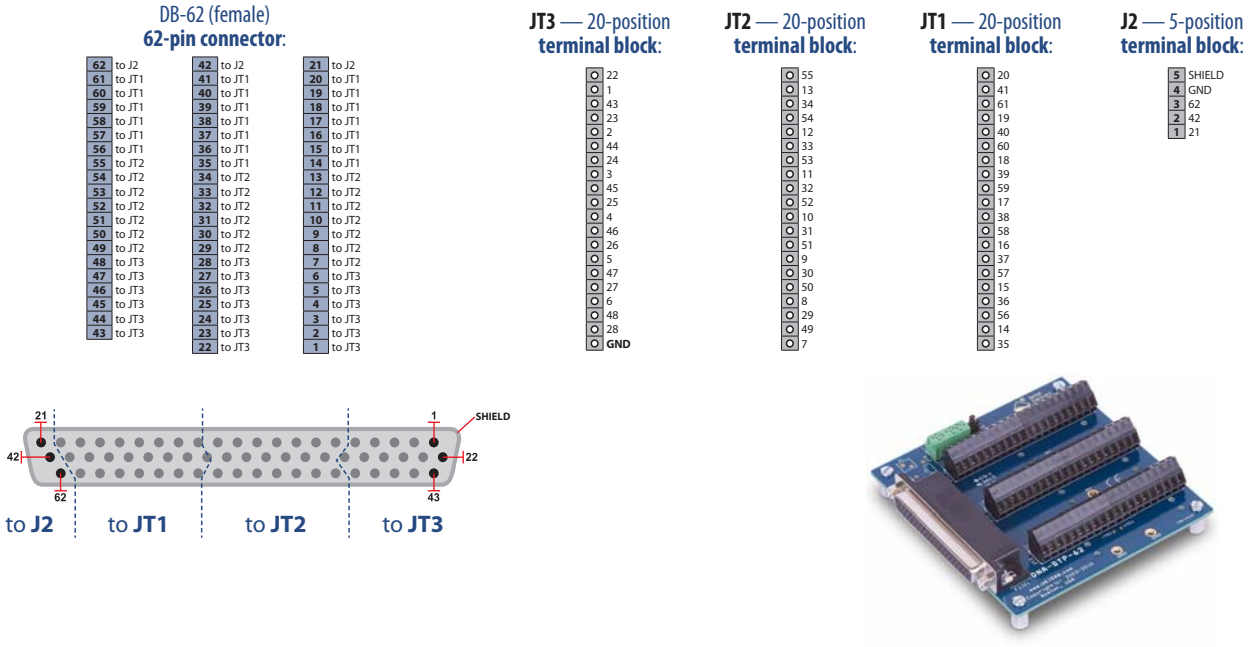

Figure A-1. Pinout and photo of DNA-STP-62 screw terminal panel

DNA-STP-212D

The DNA-STP-212D is a Screw Terminal Panel with built-in CJC temp sensors. It is suitable for direct connection to the DNx-AI-212 board or may be mounted remotely.

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