DNx-AI-217

User Manual

16-Channel, 24-bit, Simultaneously Sampling, Differential
Analog Input Board
for the PowerDNA Cube and RACK Series Chassis

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PN Man-DNx-AI-217

CE

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Chapter 1 Introduction

This document outlines the feature set and use of the AI-217, a 16-channel analog input board.

The following product versions are described in this manual:

- AI-217-1: decimating 120 kS/s/channel with 128-tap-FIR-filter
- AI-217-803: non-decimating 30 kS/s/channel with 512-tap-FIR-filter

The following sections are provided in this chapter:

- Organization of this Manual (Section 1.1)
- Manual Conventions (Section 1.2)
- Naming Conventions (Section 1.3)
- Related Resources (Section 1.4)
- Before You Begin (Section 1.5)
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1.1 Organization of this Manual

This AI-217 User Manual is organized as follows:

- **Introduction**
  Chapter 1 summarizes the features and specifications of the AI-217.
- **Device Overview**
  Chapter 2 describes the device architecture, logic, and connectivity of the AI-217.
- **Programming with the High-Level API**
  Chapter 3 provides an overview of the how to create a session, configure the session, and interpret results with the Framework API.
- **Programming with the Low-Level API**
  Chapter 4 is an overview of low-level API commands for configuring and using the AI-217 board.
- **Appendix A - Accessories**
  This appendix provides a list of accessories available for use with the AI-217 board.

1.2 Manual Conventions

The following conventions are used throughout this manual:

Tips are designed to highlight quick ways to get the job done or to reveal good ideas you might not discover on your own.

CAUTION! advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.

NOTE: Notes alert you to important information.

Typeface	Description	Example
bold	field or button names	Click **Scan Network**
»	hierarchy to get to a specific menu item	**File » New**
`fixed`	source code to be entered verbatim	`session.CleanUp()`
<brackets>	placeholder for user-defined text	`pdna://<IP address>`
italics	path to a file or directory	*C:/Program Files*

1.3 Naming Conventions

The DNA-AI-217, DNR-AI-217, and DNF-AI-217 board versions are compatible with the UEI Cube, RACKtangle, and FLATRACK chassis respectively. These boards are electronically identical and differ only in mounting hardware. The DNA version stacks in a Cube chassis, while the DNR and DNF versions plug into the backplane of a Rack chassis. Throughout this manual, the term DNx-AI-217 refers to both Cube and Rack products.

1.4 Related Resources

This manual only covers functionality specific to the AI-217. To get started with the UEI IOM, please see the documentation included with the software installation. On Windows, these resources can be found from the desktop by clicking **Start » All Programs » UEI**

UEI's website includes other user resources such as application notes, FAQs, tutorials, and videos. In particular, the glossary of terms may be helpful when reading through this manual: https://www.ueidaq.com/glossary

Additional questions? Please email UEI Support at uei.support@ametek.com or call 508-921-4600.

1.5 Before You Begin

No Hot Swapping!

Before plugging any I/O connector into the Cube or RACKtangle, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

Check Your Firmware

Ensure that the firmware installed on the Cube or Rack CPU matches the UEI software version installed on your PC. The IOM is shipped with pre-installed firmware and a matching software installation. If you upgrade your software installation, you must also update the firmware on your Cube or RACK CPU. See “FirmwareUpdatingProcedures” for instructions on checking and updating the firmware. These instructions are located in the following directories:

- On Linux: *<PowerDNA-x.y.z>/docs*
- On Windows: **Start » All Programs » UEI » PowerDNA » Documentation**

1.6 AI-217 Features

The DNx-AI-217 is a 16-channel simultaneously sampling A/D board that features 24-bit resolution with 7 software selectable input gain ranges. The DNx-AI-217 is pin compatible with UEI's DNx-AI-207 board and offers an easy upgrade path for those looking for more resolution, higher sample rates or simultaneously sampling inputs.

Features of the DNx-AI-217 board include:

- 16 differential analog input channels
- Simultaneous sampling (one A/D converter per channel)
- Maximum sampling rate:
  - 120 kHz per channel for the AI-217-1
  - 30 kHz per channel for the AI-217-803
  - 480 kHz max aggregate per board for both versions
- 24-bit resolution
- ±10V input range
- Programmable gains: 1, 2, 4, 8, 16, 32 and 64
- Built-in Guardian diagnostics: open input detection and input over-range detection per channel
- Pin compatible with DNx-AI-207
- Low-pass FIR filtering
- Weight of 120 g or 4.24 oz for DNA-AI-217; 630 g or 22.2 oz with PPC5 chassis
- Tested to withstand 5g vibration, 50g shock, -40 to +85°C temperature

1.6.1 ADC Input Configuration

Each AI-217 channel has a dedicated A/D converter. This configuration allows channels to be sampled simultaneously at rates up to 120 kSample/s each for AI-217-1 or 30 kSample/s each for AI-217-803 (up to 480 kS/s max aggregate rate per board for either board version). Using the configuration of a single A/D per channel virtually eliminates input cross talk and channel settling time issues even when connected to high impedance signal sources.

The DNx-AI-217 is fully isolated from the Cube/RACK chassis and is overvoltage protected up to ±40 V (power on or off). The inputs go into a high impedance mode when power is removed making the AI-217 ideal for use in redundant measurement/control applications.

1.6.2 Guardian Diagnostic Support

The DNx-AI-217 is a member of UEI's Guardian series, a series of products with build-in user diagnostic features. The AI-217 board provides both open input detection functionality, as well as the ability to detect input overvoltage conditions.

1.6.3 Environmental Conditions

As with all UEI PowerDNA boards, the DNx-AI-217 can be operated in harsh environments and has been tested at 5*g* vibration, 50*g* shock, -40 to +85°C temperature. Each board provides 350 V_{rms} isolation between the board and its enclosure, or any other installed boards.

1.6.4 Software Support

Software included with the DNx-AI-217 provides a comprehensive yet easy to use API that supports all popular operating systems including Windows, Linux, real-time operating systems such as QNX, RTX, VXworks and more. The UEIDAQ framework comes with bindings for various programming languages such as C, C++, C#, VB.NET and scientific software packages such as LabVIEW and Matlab, as well as supporting OPC servers.

1.7 Specification

Table 1-1 lists the technical specifications for the AI-217-1 and AI-217-803. All specifications are for a temperature of 25°C unless otherwise stated.

Table 1-1 Technical Specifications

	AI-217-1	AI-217-803
Number of Channels	16 fully differential	
ADC resolution/type	24 bits / SAR. (AD7766)	
Sampling rate	120 kS/s per channel (max); 1600 kS/s max aggregate for entire board	30 kS/s per channel (max); 480 kS/s max aggregate for entire board
FIFO depth	2048 samples	
Input bias current	<2 nA typical	
Input offset	At 25°C: < 4 µV; G=1, < 2 µV; G=2, <1 µV; G>2 At -40°C to +85°C: 2.5 times the 25°C offset	
Gain and INL error	< 0.004% (40 ppm) max	
Input impedance	100 MΩ (min)	
Input range	±10V (gain = 1)	
Input resolution	1.19 µV (gain = 1), 18.6 nV (gain = 64)	
Gains	1, 2, 4, 8, 16, 32, 64	
Common mode rejection	110 dB typical	
Chan to Chan crosstalk	< 1 µVrms	
Open input detection current	100 µA	
Isolation	350 Vrms	
Overvoltage protection	-40V to +40V (power on or off)	
Power off leakage current	< 10 µA (-40V to +40V)	
Power consumption	2.2W max	
Operating temperature range	Tested -40 to +85°C	
Operating humidity	95%, non-condensing	
Vibration IEC 60068-2-6 IEC 60068-2-64	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500 Hz, broadband random	
Shock IEC 60068-2-27	100 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations	
Altitude	120,000 ft	
MTBF	275,000 hours	

1.8 Comparison between AI-217 and AI-207 Boards

The following table is a side-by-side comparison of specifications for the AI-207 and the AI-217 analog input boards:

Table 1-2 AI-207 vs. AI-217

Item	AI-207	AI-217
Channels	16 differential analog voltage plus 1 CJC	16 differential analog voltage
Input Range	±10 V	±10 V
Num. of A/D Converters	1	16 (one per input channel)
Simultaneous Sampling	No	Yes
Sample Delivery Rate	16 kHz aggregate max (1 kHz for 16 channels, 2 kHz for 8 channels, or 16 kHz for one channel)	1 Hz - 120 kHz per channel for 217-1, 480 kHz aggregate max. (30 kHz/channel max for 217-803)
CJC Channel	Channel 33 (adjustable gain)	not recommended for use with AI-217
Available Gains	1, 2, 4, 8, 10, 20, 40, 80, 100, 200, 400, 800	1, 2, 4, 8, 16, 32, 64
Source Impedance Compatibility	Best with low impedance sources	Performs well with either low or high impedance sources
Resolution	18-bit	24-bit
Isolation	350 V_{rms} between inputs and chassis. Common ground for input channels.	350 V_{rms} between inputs and chassis. Common ground for input channels.
Pinout	Same for both models	
Noise Filtering	Averaging engine that averages multiple samples to improve resolution	AI-217 has a simple analog low-pass RC filter on the front-end for anti-aliasing designed for 60k-120kS/s. Digital FIR filter for all channels with user-configurable coefficients on back-end. AI-217-1 has 128-tap FIR AI-217-803 has 512-tap FIR
Channel List	Specifies the channels that are to be read and the order in which to read them. Thus, the returned data is in the order that the channel list shows. If a channel needs to be sampled more often than other channels, the AI-207 allows the channel to be entered more than once in the channel list.	Specifies the channels that are to be read, but because they are simultaneously sampled, the sequential order concept does not apply. The AI-217 always returns data with the channels in numerical order regardless of what order they were in the channel list. A channel may only appear once in the channel list.

For an 8-channel analog input board with per-channel isolation, see the AI-218 documentation.

Chapter 2 Device Overview

This chapter describes the device architecture, logic, and connectivity for the DNx-AI-217 Analog Input Board. The following sections are provided:

- Device Architecture (Section 2.1)
- A/D Conversion (Section 2.2)
- FIR Filter (Section 2.3)
- Diagnostics (Section 2.4)
- Indicators (Section 2.5)
- Pinout (Section 2.6)
- Wiring Guidelines (Section 2.7)
- Data Representation (Section 2.8)

2.1 Device Architecture

Figure 2-1 is a block diagram of the architecture of the AI-217 board.

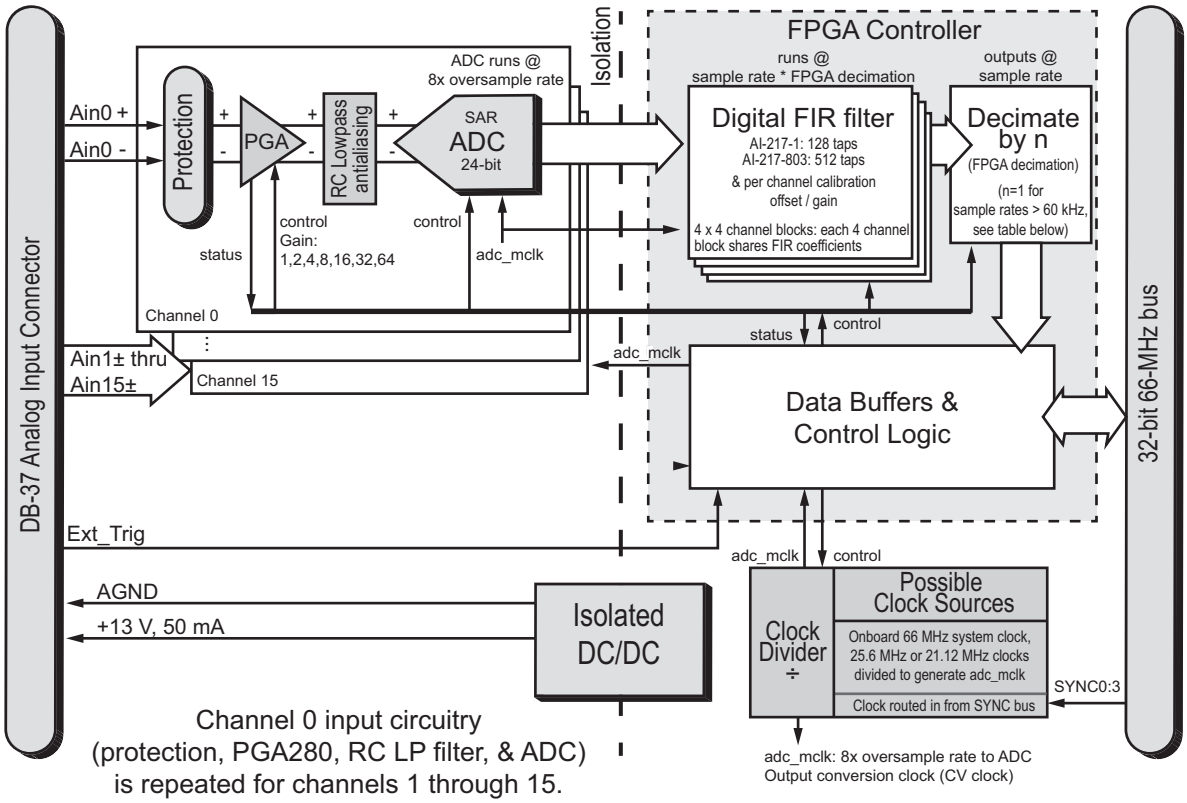


Figure 2-1 Block Diagram of the AI-217 Board

Each AI-217 has sixteen differential input channels designed for high-speed, high-resolution analog voltage signal measurement.

Each channel provides 24-bit sampling resolution over a ±10 V input range and maximum sampling rate of 120,000 samples per second (one sample every 8.333 µsec) for the AI-217-1 or 30,000 samples per second (one sample every 33.333 µsec) for the AI-217-803.

Each AI-217 analog input board is capable of up to 480,000 samples per second maximum aggregate sample rate per board.

Additionally, the DNx-AI-217 board is fully isolated from the Cube or RACK chassis.

2.1.1 Input Lines & Overvoltage Protection

Each channel's input consists of a pair of analog input pins that carry a differential voltage to be sampled. Overvoltage protection is engaged when power is removed and/or when input voltages exceed the AI-217 ±10 V input range specification (at approximately a ±12 V input voltage). When protection is activated, the inputs go into a high impedance mode and inputs are protected up to ±40 V, powered or unpowered.

The analog input lines (Ain+ and Ain- in **Figure 2-1**) enter through the DB-37 connector pins into the ±40 V overvoltage protection and then into the programmable gain amplifier (PGA280).

2.1.2 PGA & Diagnostics

The PGA provides user-programmable 1, 2, 4, 8, 16, 32, and 64x gains, as well as Guardian diagnostic features including open input detection and input overrange detection. Gains and Guardian diagnostics are user-programmable.

The output of the PGA is filtered by an onboard RC low-pass filter before A/D conversion.

2.1.3 Controller Logic

The structure of the on-chip logical modules for the AI-217 controller is illustrated in **Figure 2-2**.

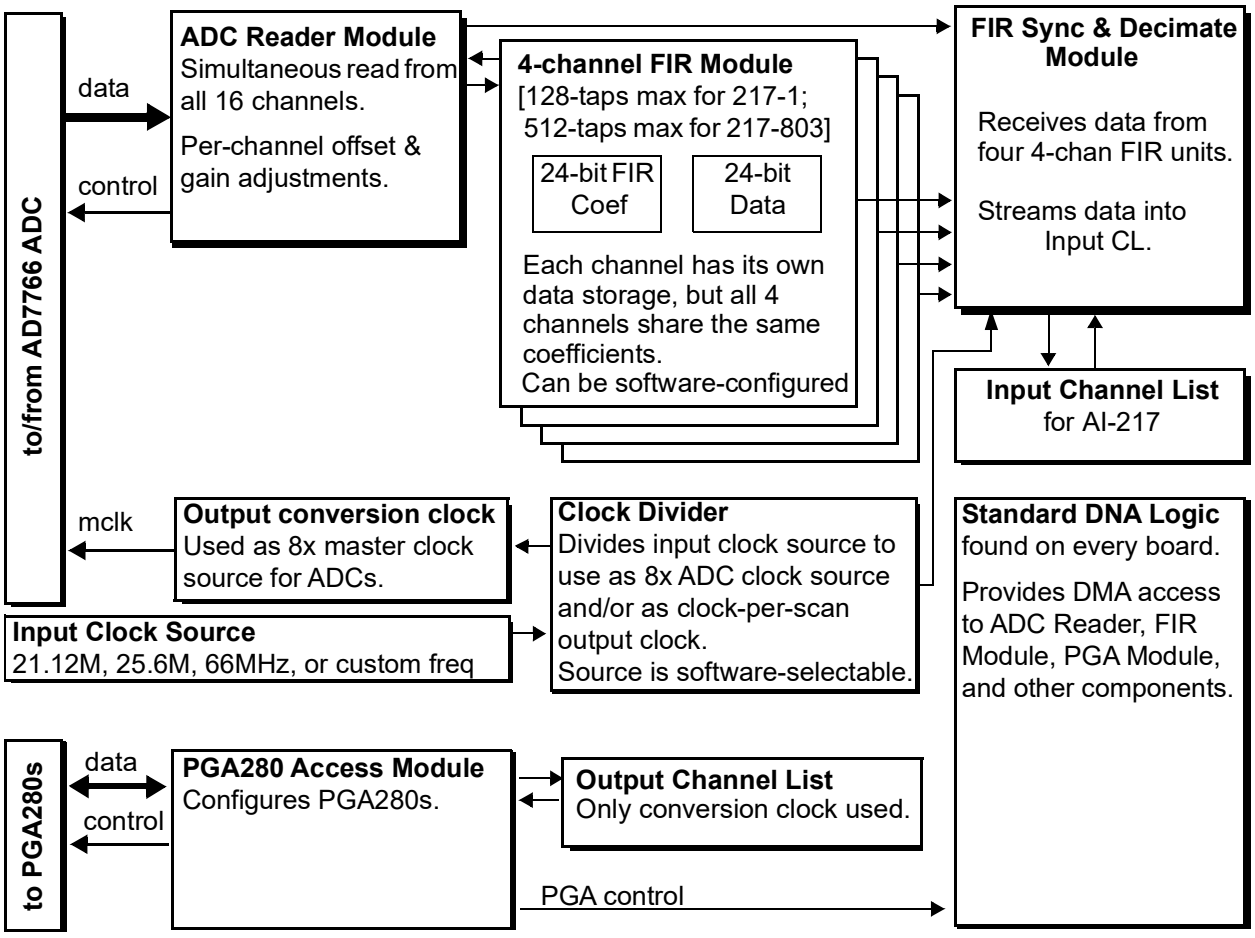


Figure 2-2 Logical Modules of the DNx-AI-217 Controller

2.1.3.1 ADC Conversion

ADC conversion is provided by a 24-bit oversampled successive approximation (SAR) A/D converter per input channel. Using a single ADC for each input channel virtually eliminates input crosstalk and channel settling time issues even when connected to high impedance signal sources. All sixteen analog inputs are first sampled by each ADC simultaneously and then calibration gain/offset adjustments are applied. The samples from ADCs are isolated from the AI-217's controller via an opto-isolatation barrier.

The AI-217 provides a special clock divider that can use 66 MHz as well as fixed 21.12 MHz or 25.6 MHz clocks to create different frequencies used to run the ADC; the AI-217[1] incorporates a programmable PLL that allows the generation of the base frequency with 0.1% or better accuracy.

More information about A/D conversion is provided in Section 2.2 on page 11.

1. This feature is supported on logic revision 02.10.D3 (2013). UEI Technical Support can provide you with a field programmable update package if your logic is older. Use PowerDNA Explorer's Hardware Report to show logic versions for your AI-217.

2.1.3.2 FIR Modules

Samples from the A/D are passed to *FIR Modules*, which provide both finite-input-response (FIR) filtering and decimation.

The module streams data into a Channel List output buffer that holds the digitized samples acquired from analog input sampling. Data held in the Channel List buffer is then retrieved by your computer application when using the high-level framework data acquisition calls (see **Chapter 3**) or low-level function calls (see **Chapter 4**).

Each data sample is stored sequentially in the output buffer in order by channel numbers.

More information about AI-217 digital FIR filtering is provided in Section 2.3 on page 19.

2.2 A/D Conversion

The AI-217 implements A/D converters (AD7766) that use an oversampled SAR architecture and require a clock source (`mclk`) that is 8x the output data rate of the ADC. AI-217 incorporates one ADC for each of the 16 analog input channels, and one for the CJC input.

A/D conversion sample rates and other details of using internal or external clocks are provided in the following sections:

- AI-217-1 A/D Conversion (Section 2.2.1 on page 11)
- AI-217-803 A/D Conversion (Section 2.2.2 on page 16)

2.2.1 AI-217-1 A/D Conversion

The maximum output data rate for an AI-217-1 channel is 120 kHz.

The master clock (`mclk`) that drives the A/D converter can be generated by an onboard clock source (set by firmware) or an external clock (programmed by users). Refer to **Figure 2-3** below and the following AI-217-1 clock configuration summaries in **Table 2-1**.

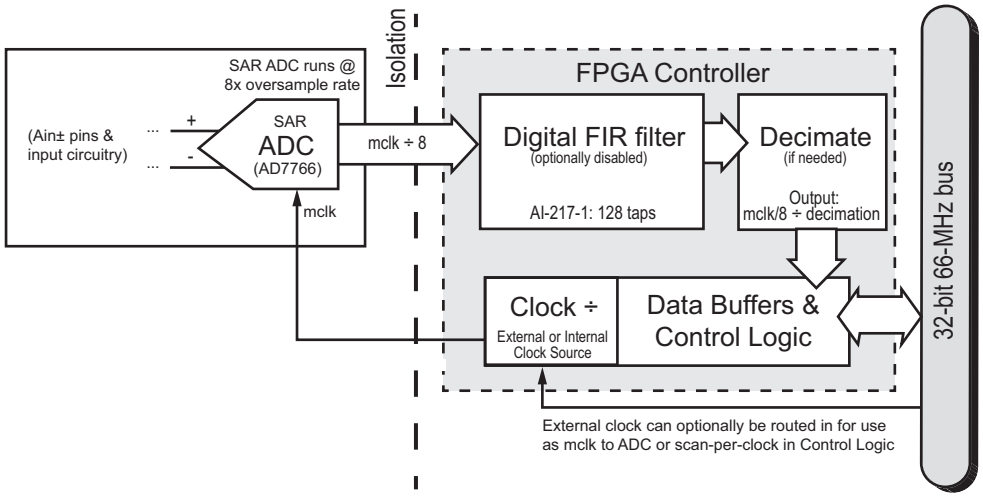


Figure 2-3 Simplified Block Diagram of AI-217-1 A/D Conversion Path

Table 2-1 AI-217-1 Clocking Configurations

Clocking Configuration	Summary	Detailed Description
Using an Onboard Master Clock Source	Firmware sets ADC clocking (`mclk`, which drives output sample rate) using an onboard clock source and a sample rate based on the user-programmed output sample rate	Section 2.2.1.1
Using an External Master Clock Source	The user sets up an external clock to drive the A/D converter. The external clock is used as the `mclk` master clock for the ADC and must be programmed at 8x the desired output sample rate	Section 2.2.1.2
Using Scan-per-clock Mode	The user sets up an external clock to produce the 1x desired output sample rate and sets a `DQ_SYNCLCLK_CLOCK_PER_SCAN` configuration flag to allow that external clock to pace output samples directly	Section 2.2.1.3

2.2.1.1 Using an Onboard Master Clock for AI-217-1

The AI-217-1 uses an onboard master clock source unless programmed to use an external source.

AI-217-1 A/D conversion using an onboard master clock source is set as follows:

- the user can set the desired sample rate via API
- the firmware calculates the required master clock (`mclk`) and engages the appropriate digital FIR filter and decimation ratio to achieve an output data rate as close as possible to the user-programmed rate
- the user has the option of reading back the actual sample rate that is calculated and set by the firmware
- the user also has the option of setting or resetting parameters for the digital FIR and decimation via API

2.2.1.1.1 Calculating `mclk` Rate for AI-217-1 Onboard Clocking

The following section provides detailed information about the onboard clocking mechanism for the AI-217-1 A/D conversions. (See Section 2.2.1.2 for external clocking).

NOTE: Please note that the master clock rate, FIR filter characteristics, and decimation ratio are automatically calculated and set by the firmware when using onboard clocking, based on the user-programmed sample rate. The only time the following could be needed by the user is if you want to optimize or change FIR filter characteristics. FIR descriptions are provided in Section 2.3 on page 19.

The master clock (`mclk`) rate used for AI-217-1 onboard ADC clocking is constrained by two factors:

- the `mclk` rate must be between 480 kHz to 960 kHz (the 480 kHz minimum is unique to using onboard clock sources on the AI-217-1)
- the `mclk` rate must be evenly divisible by one of the three onboard clock sources (66 MHz, 21.12 MHz or 25.6 MHz) (See *NOTE below)

Using the user-programmed data output rate as a seed, the firmware calculates the closest sample rate available that will satisfy system constraints and then sets the AI-217-1 to use that sample rate.

Because the output sample rate is dependent on `mclk`, the AI-217-1 data output rate must comply with the following formula:

```
delivered data rate = (clock_source / whole#) / (n * 8)
```

where:

- `clock_source` is one the three onboard clock sources (66 MHz, 21.12 MHz or 25.6 MHz) (See *NOTE)
- `whole#` must be an integer, not fractional
- `8` is the oversample rate of the ADC
- `n` is the n:1 decimation value (power of 2). Refer to **Table 2-2**.

NOTE: *AI-217 board versions after logic revision 02.10.D3 (2013) incorporate a programmable PLL that allows the generation of the base frequency with 0.1% or better accuracy when sample rates aren't evenly divisible by onboard clock sources. UEI Technical Support can provide a field programmable update package if your board's logic is older. You can use PowerDNA Explorer's Hardware Report to show logic versions of your AI-217 boards.

Table 2-2 Decimation Ratios At Delivered Data Rates for the AI-217-1

Delivered Data Rate	Decimation Ratio	ADC Output Rate	Master Clock (`mclk`) Rate
60.01 kHz to 120 kHz	1:1	60.01 kHz to 120 kHz	480 kHz to 960 kHz
30.01 kHz to 60 kHz	2:1	60.01 kHz to 120 kHz	480 kHz to 960 kHz
15.01 kHz to 30 kHz	4:1	60.01 kHz to 120 kHz	480 kHz to 960 kHz
7.501 kHz to 15 kHz	8:1	60.01 kHz to 120 kHz	480 kHz to 960 kHz
3751 Hz to 7.501 kHz	16:1	60.01 kHz to 120 kHz	480 kHz to 960 kHz
1876 Hz to 3750 Hz	32:1	60.01 kHz to 120 kHz	480 kHz to 960 kHz
937.6 Hz to 1875 Hz	64:1	60.01 kHz to 120 kHz	480 kHz to 960 kHz
469 Hz to 937.5 Hz	128:1	60.01 kHz to 120 kHz	480 kHz to 960 kHz
235 Hz to 468.75 kHz	256:1	60.01 kHz to 120 kHz	480 kHz to 960 kHz
1 Hz to 234.375 Hz	>= 512:1	60.01 kHz to 120 kHz	480 kHz to 960 kHz

To get output data rates less than 60 kHz, the decimation module in the FPGA is used. The decimation module will only keep 1 in n samples, where n is the decimation factor. The following pseudocode shows how to calculate the master clock frequency and the decimation ratio for the AI-217-1:

```
// calculate decimation factor and sample rate

decratio = 1;
while (mclkrate <= (480000/8)){ // start at 60000Hz
        mclkrate *= 2;
        decratio *= 2;
}
```

2.2.1.2 Using an External Master Clock for AI-217-1

An externally generated ADC master clock (`mclk`) for the AI-217-1 board can be routed in over a chassis-wide bus.

External clock sources can be routed in from a PLL or Event Module on the chassis CPU board, from a different board installed in the chassis (e.g. IRIG-650), or from a clock source external to the chassis routed in through the external sync connector.

When supplying an external clock (and when the AI-217-1 is not in the scan-per-clock mode), the user provides the ADC master clock, which must meet the following system requirements:

- the `mclk` rate must be less than or equal to 960 kHz
- the `mclk` rate must be 8x the desired ADC data delivery rate (output sample rate if decimation is not used)
- the user is responsible for enabling or disabling the digital FIR filter / decimation module and setting options accordingly

When supplying `mclk` externally, the external master clock should constantly run even when conversion results are not used. This primes a long FIR filter that should stay settled (see AD7766 datasheet for details about the ADC). Samples are always produced but are not stored in the output buffer until a start command or start trigger is issued.

Note that the A/D converter oversamples at an 8x rate: in the configuration described in this section, the ADC uses an `mclk` provided externally and produces samples at an `mclk`/8 rate (see **Figure 2-3** on page 11). If no additional decimation is programmed, this will be the output data rate of the channel.

When programming the digital FIR, users can also program a decimation rate. If the decimation hardware in the FPGA is used, the user must program `mclk` accordingly, otherwise `mclk` is just the output data rate * 8.

As an example:

- If decimation is set to 2 and you want samples available at a 30 kHz delivery rate, the output of the A/D converter would need to be at 2 * 30 kHz, or 60 kHz.
- To get the A/D converter to produce samples at a 60 kHz rate, it will need a 60 kHz * 8 (or 480 kHz) `mclk` source. That will be the rate you program the external clock.

2.2.1.2.1 Synchronizing Multiple Boards with an AI-217-1 External Clock

When multiple boards require synchronization, a master clock generated externally can be routed to the chassis-wide SYNC bus (e.g. SYNC1 line), and used as the clock for all of the AI-217-1 slave boards (CVCKSRC1).

Keeping all AI-217-1 boards synchronized using an 8x ADC clock and hardware trigger would provide fully synchronous operation of multiple boards; however, if other boards in the system require synchronization at a 1x rate, then the following options are available:

- a master clock synchronized to a 1PPS pulse[1] can be generated on the CPU board, distributed throughout the chassis, and divided down locally on I/O boards, as needed.

- a master 8x clock can be divided by eight clock cycles using a counter board (e.g., CT-601) and distributed across the system. This may require an extra board if the CT-601 isn't installed.
- a scan-per-clock mode can be used, where each individual board is configured to run the ADC at the maximum rate of 120 kHz and the scan clock (CLCKSRC1) is used as a gate that grabs one last scan received from the converters at the 1x data output rate. See the next section for more information.

2.2.1.3 Using Scan-per-clock Mode (AI-217-1)

Scan-per-clock mode is a simplified programming mode for the AI-217-1. It allows users to program an external clock at the desired 1x sample rate, without concern for A/D converter oversample constraints. To use scan-per-clock mode, a `DQ_SYNCLCLK_CLOCK_PER_SCAN` configuration flag is set using a low-level function call. See **Chapter 4** for more information about low-level programming.

In this mode, onboard control logic provides a 960 kHz clock to the A/D converter, which results in a 120 kHz rate out of the A/D converter. The digital FIR can be enabled or disabled based on customer configuration.

The Decimate module after the FIR is not used; instead the pacing of samples is accomplished in the control logic. In this mode, the digital FIR block produces a sample every 120 kHz, regardless of whether the FIR is enabled or not (if it's not enabled then the incoming samples pass straight through and are not digitally filtered). The output samples from the digital FIR are continually overwritten in a single register in the control logic, and stored in the Channel List output buffer on a rising edge of the incoming clock, synchronized to the desired sample rate.

When using scan-per-clock mode, be aware of the following:

- There could be ±1 conversion cycle ($8.\overline{3}$ µsec) jitter when synchronizing multiple I/O boards to the same clock source.
- If the digital FIR filter is not enabled, the only filtering is by the low-pass analog RC filter and FIRs in the A/D converter (AD7766), which have a typical -3 dB cutoff frequency at 0.49 * the A/D output rate (for scan-per-clock mode, f_c = ~60 kHz). This means that any noise or harmonics less than 60 kHz could fold back into your band of interest after the control logic decimates samples.
- If the digital FIR filter is enabled and used, note it will run at 120 kHz. (For more information about the AI-217 digital FIR, please see Section 2.3.)

1. This feature is supported on logic revision 02.12.36 (2017). UEI Technical Support can provide you with a field programmable update package if your logic is older. Use PowerDNA Explorer's Hardware Report to show logic versions for your AI-217.

2.2.2 AI-217-803 A/D Conversion

The AI-217-803 differs from the AI-217-1 in the following ways:

- the maximum output data rate per channel is 30 kHz
- the maximum master clock rate (`mclk`) that drives the A/D converter is 240 kHz (30 kHz* 8)
- there is no decimation after the digital FIR filter
- the digital FIR filter increases from a maximum of 128 taps to 512 taps

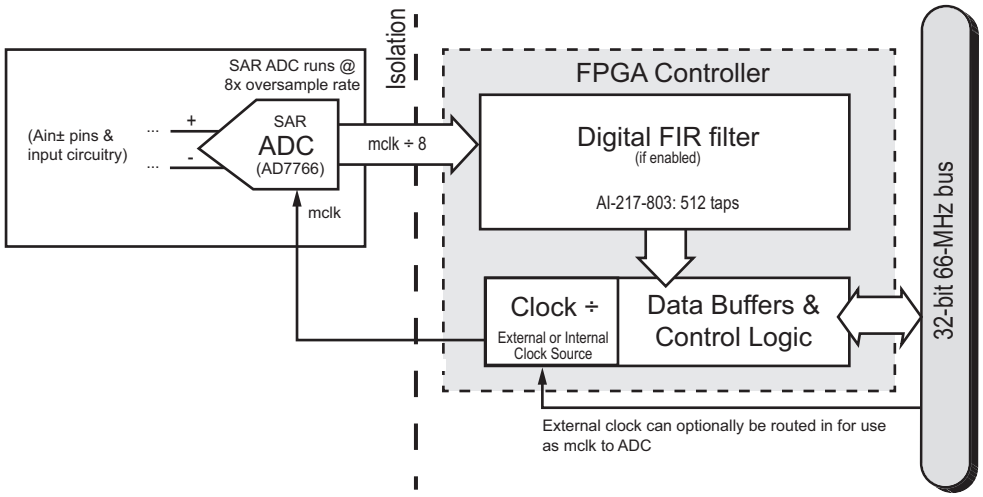


Figure 2-4 Simplified Block Diagram of AI-217-803 A/D Conversion Path

Similar to the AI-217-1, the master clock that drives the A/D converter can be generated by an onboard clock source (set by firmware) or an external clock (programmed by users). Refer to **Figure 2-4** above and AI-217-803 master clock configuration summaries below:

Table 2-3 AI-217-803 Clocking Configurations

Clocking Configuration	Summary	Detailed Description
Using an Onboard Master Clock Source	Firmware sets ADC clocking (`mclk`, which drives output sample rate) using an onboard clock source, based on the user-programmed output sample rate	Section 2.2.2.1
Using an External Master Clock Source	The user sets up an external clock to drive the A/D converter. The external clock is used as the master clock for the ADC and must be programmed at 8x the desired output sample rate	Section 2.2.2.2

NOTE: With the AI-217-803 the user may need to supply an appropriate input anti-aliasing (low-pass) filter on the front-end, similar to the analog RC low-pass filter of the AI-217-1, if aliasing below 56 kHz is a concern.

2.2.2.1 Using the Onboard Master Clock for AI-217-803

The following section provides detailed information about the onboard clocking mechanism for the AI-217-803 A/D conversions. (See Section 2.2.2.2 for external clocking).

AI-217-803 A/D conversion is set as follows when using an onboard master clock source:

- the user can set the desired sample rate via API
- the firmware calculates the required master clock (`mclk`) to achieve an output data rate as close as possible to the user-programmed rate
- the user has the option of reading back the actual sample rate calculated and set by the firmware
- the user also has the option of setting or resetting parameters for the digital FIR via API

NOTE: Please note that the master clock rate and FIR filter characteristics are automatically calculated and set by the firmware when using onboard clocking, based on the user-programmed sample rate. The only time the following could be needed by the user is if you want to optimize or change FIR filter characteristics. FIR descriptions are provided in Section 2.3 on page 19.

In this onboard clock configuration for the AI-217-803, the master clock rate must be less than 240 kHz and must be evenly divisible by one of the three onboard clock sources (66 MHz, 21.12 MHz or 25.6 MHz). (See *NOTE below.)

Using the user-programmed data output rate as a seed, the firmware calculates the closest sample rate available that is evenly divisible by one of the onboard clock sources and then sets the AI-217-803 to use that sample rate.

```
delivered data rate = (clock_source / whole#) / (8)
```

where (8) accounts for the 8x oversample rate of the A/D converter.

NOTE: *AI-217 board versions after logic revision 02.10.D3 (2013) incorporate a programmable PLL that allows the generation of the base frequency with 0.1% or better accuracy when sample rates aren't evenly divisible by onboard clock sources. UEI Technical Support can provide a field programmable update package if your board's logic is older. You can use PowerDNA Explorer's Hardware Report to show logic versions of your AI-217 boards.

2.2.2.2 Using an External Master Clock for AI-217-803

An externally generated ADC master clock (`mclk`) for the AI-217-803 board can be routed in over a chassis-wide bus.

External clock sources can route in from a PLL or Event Module on the chassis CPU board, from a different board installed in the chassis (e.g. IRIG-650), or from a clock source external to the chassis routed in through the external sync connector.

When routing in an external clock, the user is supplying `mclk`, which means the user is responsible for providing an `mclk` that meets system requirements:

- the `mclk` rate must be less than or equal to 240 kHz
- the `mclk` rate must be 8x the desired data delivery rate (output sample rate)
- the user is responsible for enabling or disabling the digital FIR filter and setting options accordingly

The external master clock should be constantly running even when conversion results are not used. This primes a long FIR filter and helps with settle times (see AD7766 datasheet for details about the ADC). Samples are always produced but are not stored in the output buffer until a start command or start trigger is issued.

Note that the A/D converter has its own FIR filters with a typical -3 dB cutoff frequency at 0.49 times the A/D output rate. If additional filtering is needed, the AI-217-803 provides the option of using a digital FIR module in the FPGA.

Refer to Section 2.3 for more information about the digital FIR module.

2.3 FIR Filter

This section discusses the configuration of the digital FIR filter found in the *FIR module* logical block. This should not be confused with FIR filters built into the A/D converter (described in the AD7766 datasheet) or the RC low-pass anti-aliasing filter at the output of the PGA, discussed in Section 2.1.

The *FIR module* implements an integer-based finite-input-response filter with the following characteristics:

- 128-taps on the AI-217-1, for a faster response and lower group delay
- 512-taps on the AI-217-803, which provides a sharper filter with less ripple

The AI-217 *FIR module* provides four 4-channel digital FIR filters, which can be optionally enabled or disabled. Each 4-channel digital FIR filter corresponds to the following channel groupings: channels 0 to 3, 4 to 7, 8 to 11, and 12 to 15.

Each channel uses its own storage for the 24-bit sample data and each four channels share the same 24-bit coefficients. By default, all channels are set to the same coefficients by the software function call for simplicity, and thus have the same output data rate.

The default filter is configured to suppress harmonics greater than one half of the ADC output data rate; however, you can generate/use your own filter coefficients.

The filter operates as per standard digital FIR filter theory:

1. The newest input sample from the ADC is put into the delay line register.
2. Each sample in the delay line is multiplied by the corresponding coefficient. All multiplied values are accumulated to provide the result to the output line.
3. Shift the delay line by one sample to make room for the next input sample.

Caveats of using the digital FIR filter are that rippling may occur in response to sharp edges, and using the digital FIR adds additional group delay.

2.3.1 FIR Group Delay

The total group delay for the AI-217 is calculated as follows:

- 128/2=64 sample delay for the AI-217-1 or 512/2=256 sample delay for the AI-217-803
- 37 sample delay for the FIR filters inside of the A/D converter (AD7766)
- an additional 1 sample delay is required by the channel architecture

This yields a maximum total group delay of 102 samples for the AI-217-1 and 294 samples for the AI-217-803 when the digital FIR filters are enabled.

2.3.2 Using the Digital FIR Filter

The following options for the AI-217 digital FIR filter can be set or reset by the user:

- enable or disable the FIR filter
- override the automatic selection of coefficients, and select one of the already existing sets of coefficients
- import your own set of coefficients, and optionally set a new number of taps (128 or less for the AI-217-1, and 512 or less for the AI-217-803)
- set or reset the decimation rate (AI-217-1 only): the *FIR module's* decimation ratio can also be user-configured to 0 (keep all samples) or higher

2.3.2.1 FIR Filter Sample Rate

The digital FIR filter on the AI-217 always runs at the output rate of the A/D converter.

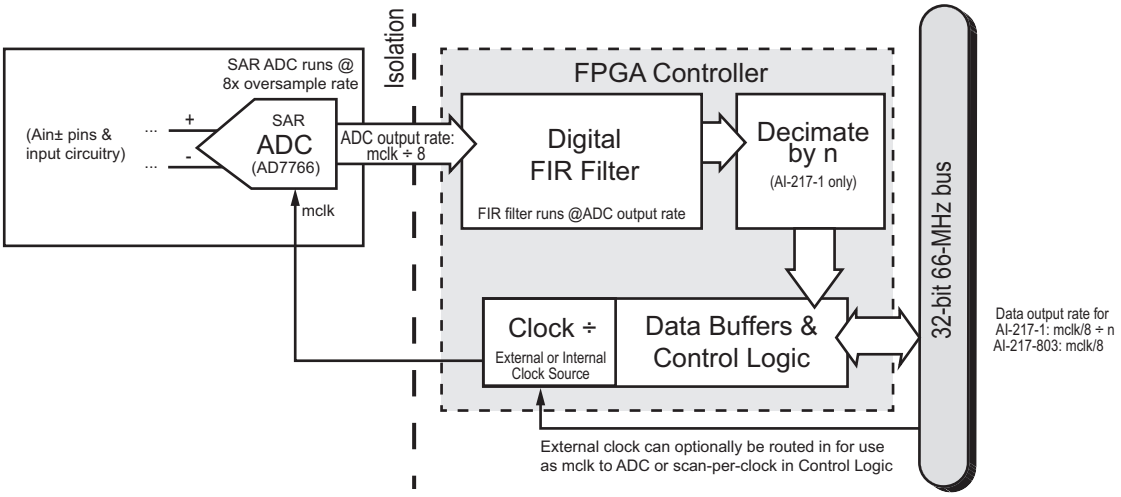


Figure 2-5 Simplified Block Diagram of AI-217

The following table can be used to calculate at what rate the FIR filter will be running on each board version and for the different clocking configurations. For more information about clock configurations for the A/D converter, refer to Section 2.2.

Table 2-4 AI-217 FIR Filter Sample Rates

Board Version	Clock Configuration	FIR Sample Rate (=ADC Output Rate)
AI-217-1	Onboard master clock mode (internally generated `mclk`)	decimation ratio * output data rate See **Table 2-5** for a mapping of decimation ratios to output data rates
AI-217-1	External master clock mode	output data rate
AI-217-1	Clock-per-scan mode (external clock)	120 kHz
AI-217-803	Onboard master clock mode (internally generated `mclk`)	output data rate
AI-217-803	External master clock mode	output data rate

The following table can be used to map the decimation ratio to the output data rate for the AI-217-1 when using onboard clock sources. Knowing the output data rate and the decimation ration will allow you to calculate at what rate the FIR filter is running (FIR filter rate = data output rate * decimation rate).

Table 2-5 AI-217-1 FIR Filter Sampling Rates for Internally Generated Master Clocks

Output Data Rate	Decimation Ratio	FIR Sampling Rate	ADC Output Rate
60.01 kHz to 120 kHz	1:1	1 * delivered data rate	Note that the ADC output rate (and by design, the FIR sampling rate) will stay constrained between 60.01 kHz to 120 kHz when using master clocks generated by AI-217-1 onboard/ internal clock sources. Decimation is used to achieve output sample rates less than 60 kHz.
30.01 kHz to 60 kHz	2:1	2 * delivered data rate	
15.01 kHz to 30 kHz	4:1	4 * delivered data rate	
7.501 kHz to 15 kHz	8:1	8 * delivered data rate	
3751 Hz to 7.501 kHz	16:1	16 * delivered data rate	
1876 Hz to 3750 Hz	32:1	32 * delivered data rate	
937.6 Hz to 1875 Hz	64:1	64 * delivered data rate	
469 Hz to 937.5 Hz	128:1	128 * delivered data rate	
235 Hz to 468.75 Hz	256:1	256 * delivered data rate	
1 Hz to 234.375 Hz	>= 512:1	>= 512 * delivered data rate	

2.3.2.2 FIR Filter Coefficients

The AI-217 has a set of 10 pre-established digital FIR filters to choose from.

The FIR filters are designed with the -3 dB cutoffs as shown in **Table 2-6**.

At sample rates below 234 Hz (filter index 9), the filter is a moving average.

Users can select one of the onboard digital FIR filters by setting the index parameter in the digital FIR setup API.

Refer to the following table for characteristics of each of the ten AI-217 digital FIR filters, and refer to **Table 2-4** on page 20 for FIR sample rates.

.

Table 2-6 Default AI-217 FIR Filters

Index for Default FIR Filters	-3 dB Cutoff
0	~ 0.5 * FIR sample rate
1	~ 0.5 * FIR sample rate * 1/2
2	~ 0.5 * FIR sample rate * 1/4
3	~ 0.5 * FIR sample rate * 1/8
4	~ 0.5 * FIR sample rate * 1/16
5	~ 0.5 * FIR sample rate * 1/32
6	~ 0.5 * FIR sample rate * 1/64
7	~ 0.5 * FIR sample rate * 1/128
8	~ 0.5 * FIR sample rate * 1/256
9	~ 0.5 * FIR sample rate * 1/256

When using onboard clock sources, the firmware automatically selects the appropriate filter index that corresponds with the user-selected sample rate. Keep in mind, when using onboard clock sources on the AI-217-1 the ADC sample rate (and FIR filter sample rate) is restricted to between 60.01 kHz to 120 kHz; output sample rates below 60 kHz are achieved by decimation.

When inputting a master clock from an external source, the user must program the FIR module and select which coefficients to use. You can select from one of the filters listed above, or if you do not want to use the digital FIR filter, you can disable it.

2.3.2.3 Programming Custom FIR Filter Coefficients

Users have the option of designing their own digital filter and uploading those coefficients for use by the AI-217 input channels.

Please carefully review the A/D converter requirements found in Section 2.2 starting on page 11 and FIR filter descriptions found in this section before attempting to design your own filter.

2.4 Diagnostics

The DNx-AI-217 is a member of UEI's Guardian series, a series of products with build-in user diagnostic features. The AI-217 board provides both open input detection functionality, as well as the ability to detect input overvoltage conditions.

Diagnostic features can be accessed when programming using the high level Framework with the `EnableOpenCircuitDetection()` and `IsCircuitOpen()` methods. Refer to **Chapter 3** for more information.

Diagnostic information can be retrieved when programming with the low level API with the `DqAdv217GetPgaStatus()` API. Refer to **Chapter 4** for an overview of the function, to the PowerDNA API Reference Manual for a detailed description of how the function works, and to the sample code on how to use it.

2.5 Indicators

The DNx-AI-217-1 and DNx-AI-217-803 indicators are described in **Table 2-7** and illustrated in **Figure 2-6**.

Table 2-7 AI-217 Indicators

LED Name	Description
RDY	Indicates board is powered up and operational
STS	Indicates which mode the board is running in: • **OFF**: Configuration mode, (e.g., configuring channels, running in point-by-point mode) • **ON**: Operation mode, (e.g., running in VMap or ACB mode)

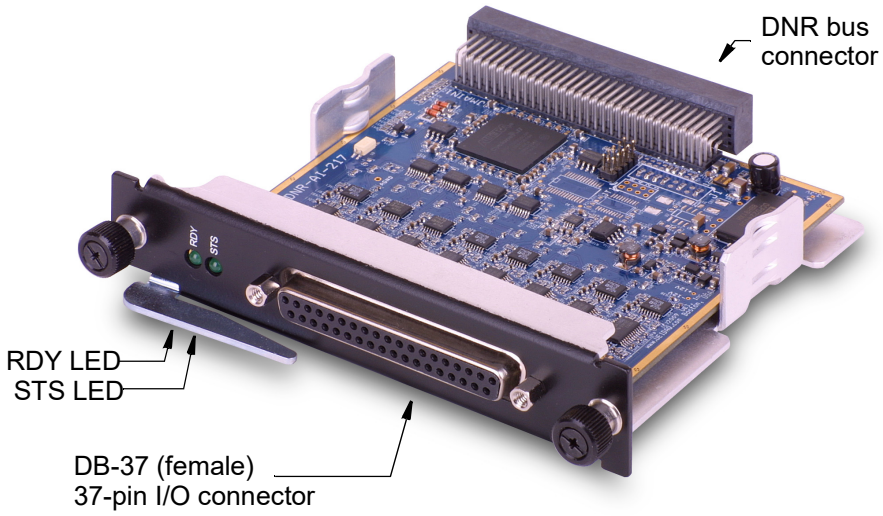


Figure 2-6 Photo of DNR-AI-217 Analog Input Board

2.6 Pinout

Figure 2-7 below illustrates the pinout of the AI-217. The AI-217 board uses a 37-pin D-sub connector. The following signals are located at the connector:

- AIN0+ to AIN15+ — input channel, differential mode. Use AIN0- to AIN15- as signal returns.
- +13V, 50mA — optional power source for external circuitry
- AGND — board analog ground, isolated from system ground.
- EXT_TRIG — accepts an external trigger signal to the board.

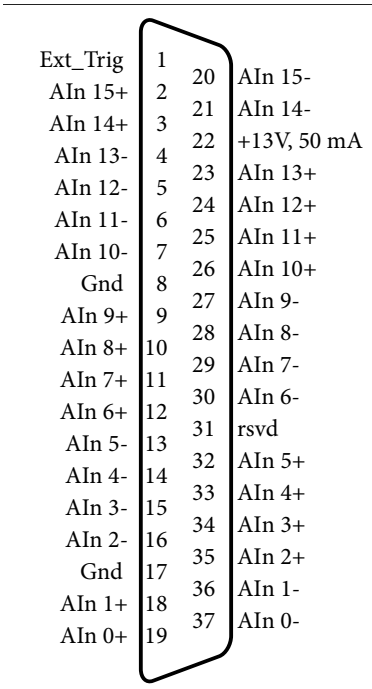


Figure 2-7 Pinout Diagram of the AI-217 Board

NOTE: If you are using a accessory panel with the AI-217, please refer to **Appendix A** for a description of the panel.

2.7 Wiring Guidelines

The recommended analog input wiring method depends on if the signal source is grounded or floating. Grounded signals are connected to the earth, such as an RTD bridge circuit powered by a desktop power supply. Floating signals are isolated from the earth; examples include thermocouples, batteries, or instruments with isolated outputs.

2.7.1 Grounded Signals

As shown in **Figure 2-8**, grounded signals should have the signal source ground wired directly to Gnd on the AI-217. Both AIn+ and AIn- inputs are referenced to Gnd and then subtracted to remove voltages common to both inputs.

It is possible to wire a differential channel for single-ended mode, but the AI-217 will still read the input differentially. Since single-ended mode is more susceptible to noise and does not increase the channel count on the AI-217, we recommend making differential measurements whenever possible.

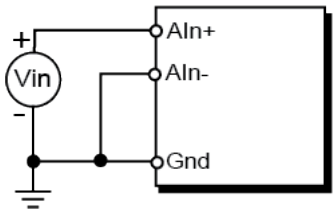
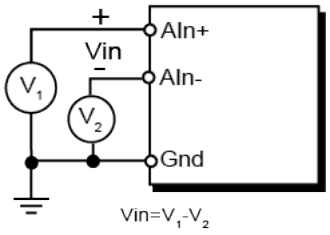
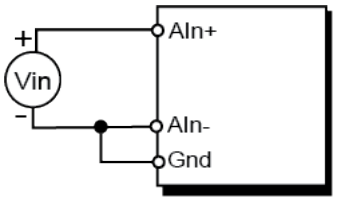
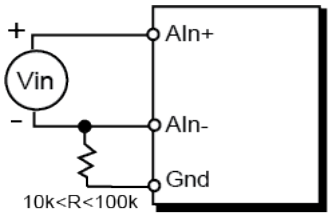
Signal Type	Single-Ended Mode	Differential Mode
Grounded		
Floating		

Figure 2-8 Analog Input Wiring on the AI-217

2.7.2 Floating Signals

Generally speaking, floating differential inputs should have AIn- wired to Gnd via a resistor. If there is no connection to Gnd, input bias currents from the source can cause input voltages to exceed the amplifier's common mode range.

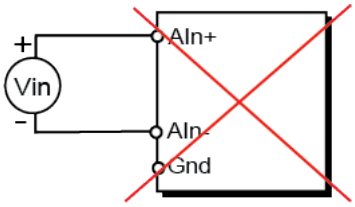


Figure 2-9 Improper Wiring for Floating Inputs

A resistor between 10 kΩ < R < 100 kΩ is small enough to provide a path to ground for input bias current, while large enough to allow AIn- to float relative to the voltage reference.

If a wire is used to connect AIn- and Gnd, the measurement will be referenced to AIn- and noise signals common to both leads will no longer be subtracted away. We recommend measuring floating input differentially by adding a resistor between AIn- and Gnd as shown in **Figure 2-8**.

Unused Pins

Unused pins on the AI-217 may be left disconnected. Disconnected pins will not reliably go to 0V, but this does not affect the operation of the other pins. If you want unused inputs to read 0V, you can short AIn+ and AIn- with a wire and connect a resistor between AIn- and Gnd.

2.8 Data Representation

The AI-217 is designed with 24-bit A/D converters. The AI-217 channels can return 24-bit straight binary in 32-bit words.

To convert data into floating point, use the following formula (when channel is programmed at a gain of 1):

$$\text{Volts} = (\text{Raw} \;\&\; 0\text{xFFFFFF}) \times \frac{20\text{V}}{(2^{24} - 1)} - 10\text{V}$$

Chapter 3 Programming with the High-Level API

This chapter provides the following information about using the UeiDaq high-level Framework API to program the DNx-AI-217:

- About the High-level Framework (Section 3.1)
- Creating a Session (Section 3.2)
- Configuring the Resource String (Section 3.3)
- Configuring the Input (Section 3.4)
- Configuring the Timing (Section 3.5)
- Detecting Open Circuits (Section 3.6)
- Reading Data (Section 3.7)
- Cleaning-up the Session (Section 3.8)

3.1 About the High-level Framework

UeiDaq Framework is object oriented and its objects can be manipulated in the same manner from different development environments, such as Visual C++, Visual Basic, or LabVIEW.

UeiDaq Framework is bundled with examples for supported programming languages. Examples are located under the UEI programs group in:

- *Start » Programs » UEI » Framework » Examples*

The following sections focus on the C++ API, but the concept is the same no matter which programming language you use.

Please refer to the “UeiDaq Framework User Manual” for more information on use of other programming languages.

3.2 Creating a Session

The Session object controls all operations on your PowerDNx device. Therefore, the first task is to create a session object:

```
// create a session object for input
                    CUeiSession aiSession;
```

3.3 Configuring the Resource String

UeiDaq Framework uses resource strings to select which device, subsystem, and channels to use within a session. The resource string syntax is similar to a web URL:

```
<device class>://<IP address>/<Device Id>/<Subsystem><Channel list>
```

For PowerDNA Cubes and RACKs, the device class is **pdna**.

For example, the following resource string selects analog input lines 0,1,2,3 on device 1 at IP address 192.168.100.2: “pdna://192.168.100.2/Dev1/Ai0:3” as a range, or as a list “pdna://192.168.100.2/Dev1/Ai0,1,2,3”.

3.4 Configuring the Input

This section describes how to configure an input for voltage measurement, thermocouple measurement, or RTD measurement.

3.4.1 Voltage Measurement

The gain applied on each channel is specified by using low and high input limits.

For example, the AI-217 available gains are 1, 2, 4, 8, 16, 32, 64 and the maximum input range is [-10V, +10V (gain = 1)].

To select the gain of 1, you need to specify input limits of [-10V, +10V]:

```
// Configure channels 0,1 to use a gain of 1 in differential mode

aiSession.CreateAIChannel("pdna://192.168.100.2/Dev0/Ai0,1",
                                    -10.0, 10.0,
                                  UeiAIChannelInputModeDifferential);
```

3.4.2 RTD Measurement

RTD measurements are configured using the Session object method `CreateRTDChannel`.

RTD sensors are resistive sensors whose resistance varies with temperature. Knowing the resistance of an RTD, we can calculate the temperature using the “Callendar Van-Dusen” equations.

RTD sensors are specified using the "alpha" (α) constant. It is also known as the temperature coefficient of resistance, which defines the resistance change factor per degree of temperature change. The RTD type is used to select the proper coefficients A, B and C for the Callendar Van-Dusen equation, which is used to convert resistance measurements to temperature.

To measure the RTD resistance, we need to know the amount of current flowing through it. We can then calculate the resistance by dividing the measured voltage by the known excitation current.

To measure the excitation current, we measure the voltage from a high precision reference resistor whose resistance is known.

The reference resistor is built-into the terminal block if you are using a DNA-STP-AI-U, but you can provide your own external reference resistor, if preferred.

In addition, you must configure the RTD type and its nominal resistance at 0° Celsius, as shown in the following example:

```
// Add 4 channels (0 to 3) to the channel list and configure them to
// measure a temperature between 0.0 and 200.0 deg. C.
// The RTD sensor is connected to the DAQ device using two wires, the
// excitation voltage is 5V, and the reference resistor is the 20kOhm
// resistor built-into the DNA-STP-AI-U.
// The RTD alpha coefficient is 0.00385, the nominal resistance at 0° C
// is 100 Ohms, and the measured temperature will be returned in °C.

MySession.CreateRTDChannel("pdna://192.168.100.2/dev0/Ai0:3",
                           0, 1000.0, UeiTwoWires, 5.0,
                            UeiRefResistorBuiltIn, 20000.0,
                            UeiRTDType3850, 100.0,
                            UeiTemperatureScaleCelsius,
                            UeiAIChannelInputModeDifferential);
```

3.5 Configuring the Timing

You can configure the AI-217 to run in simple mode (point by point) or high-throughput buffered mode (ACB mode), or high-responsiveness (DMAP) mode.

In simple mode, the delay between samples is determined by software on the host computer. In buffered mode, the delay between samples is determined by the AI-217 on-board clock and data is transferred in blocks between PowerDNA and the host PC.

The following sample shows how to configure the simple mode. Please refer to the “UeiDaq Framework User’s Manual” to learn how to use other timing modes.

```
// configure timing of input for point-by-point (simple mode)
aiSession.ConfigureTimingForSimpleIO();
```

3.6 Detecting Open Circuits

The AI-217 can source a 100µA current through each input channel to detect whether the circuit is closed or open. This can be enabled on a per channel basis. Use the AI channel object method `EnableOpenCircuitDetection` to turn on the feature on any input channel (0 to 15).

The example below shows how to turn on open circuit detection on all channels:

```
// turn on open circuit detection on all channels
for(int ch=0; ch<session.GetNumberOfChannels(); ch++) {
    CUeiAIChannel* pChan =
       dynamic_cast<CUeiAIChannel*>(session.GetChannel(ch));
    pChan->EnableOpenCircuitTest(true);
}
```

Once the session is started, you can retrieve the result of the open circuit detection with the channel object method `IsCircuitOpen`:

```
// return if circuit is open
for(int ch=0; ch<session.GetNumberOfChannels(); ch++) {
    CUeiAIChannel* pChan =
        dynamic_cast<CUeiAIChannel*>(session.GetChannel(ch));
    if(pChan->IsCircuitOpen())
    {
        std::cout << "Open circuit detected on channel " <<
                     pChan->GetIndex() << std::endl;
    }
}
```

3.7 Reading Data

Reading data is done using *reader* object(s). There is a reader object to read raw data coming straight from the A/D converter. There is also a reader object to read data already scaled to volts or mV/V.

The following sample code shows how to create a scaled reader object and read samples.

```
// create a reader and link it to the analog-input session's stream
CUeiAnalogScaledReader aiReader(aiSession.GetDataStream());
// the buffer must be big enough to contain one value per channel
double data[2];
// read one scan, where the buffer will contain one value per channel
aiReader.ReadSingleScan(data);
```

3.8 Cleaning-up the Session

The session object will clean itself up when it goes out of scope or when it is destroyed. To reuse the object with a different set of channels or parameters, you can manually clean up the session as follows:

```
// clean up the session
aiSession.CleanUp();
```

Chapter 4 Programming with the Low-Level API

This chapter provides the following information about programming the AI-217 using the low-level API:

- About the Low-level API (Section 4.1)
- Low-level Functions (Section 4.2)
- Low-level Programming Techniques (Section 4.3)

4.1 About the Low-level API

The low-level API provides direct access to the DAQBIOS protocol structure and registers in C. The low-level API is intended for speed-optimization, when programming unconventional functionality, or when programming under Linux or real-time operating systems.

When programming in Windows OS, however, we recommend that you use the UeiDaq high-level Framework API (see **Chapter 3**). The Framework extends the low-level API with additional functionality that makes programming easier, faster, and less error-prone.

For additional information regarding low-level programming, refer to the "PowerDNA API Reference Manual" located in the following directories:

- On Linux: *<PowerDNA-x.y.z>/docs*
- On Windows: **Start » All Programs » UEI » PowerDNA » Documentation**

4.2 Low-level Functions

Table 4-1 provides a summary of AI-217-specific functions. All low-level functions are described in detail in the PowerDNA API Reference Manual.

Table 4-1 Summary of Low-level API Functions for DNx-AI-217

Function	Description
`DqAdv217Read`	Returns continuously sampled data from input channel
`DqAdv217GetPgaStatus`	Returns the PGA status of the AI-217, which includes error detection flags
`DqAdv217SetCfgLayer`	Sets advanced board configuration parameters for the AI-217
`DqAdv217SetFIR`	Convenience function to configure the FIR and decimation factor
`DqAdv217SetPll`	Configures custom sampling rates using phase lock loop (PLL) on CPU board

4.3 Low-level Programming Techniques

Application developers are encouraged to explore the existing source code examples when first programming the AI-217. Sample code provided with the installation is self-documented and serves as a good starting point.

Code examples are located in the following directories:

- On Linux: *<PowerDNA-x.y.z>/src/DAQLib_Samples*
- On Windows: **Start » All Programs » UEI » PowerDNA » Examples**

Appendix A

Accessories

A.1 Cables

The following cables are available for the DNx-AI-217 board:

DNA-CBL-37

This is a 37-conductor flat ribbon cable with 37-pin male D-sub connectors on both ends. The length is 3ft and the weight is 3.4 ounces or 98 grams.

DNA-CBL-37S

This is a 37-conductor round shielded cable with 37-pin male D-sub connectors on both ends. It is made with round, heavy-shielded cable; 3 ft (90 cm) long, weight of 10 ounces or 282 grams; also available in 10ft and 20ft lengths.

A.2 STP Boards

The following screw terminal panels are available for use with the DNx-AI-217 board:

DNA-STP-37

The DNA-STP-37 provides easy screw terminal connections for all DNA and DNR series I/O boards which utilize the 37-pin connector scheme. The DNA-STP-37 is connected to the I/O board via either DNA-CBL-37 or DNA-CBL-37S series cables. The dimensions of the STP-37 board are 4.2w x 2.8d x1.0h inch or 10.6 x 7.1 x 7.6 cm (with standoffs). The weight of the STP-37 board is 2.4 ounces or 69 grams.

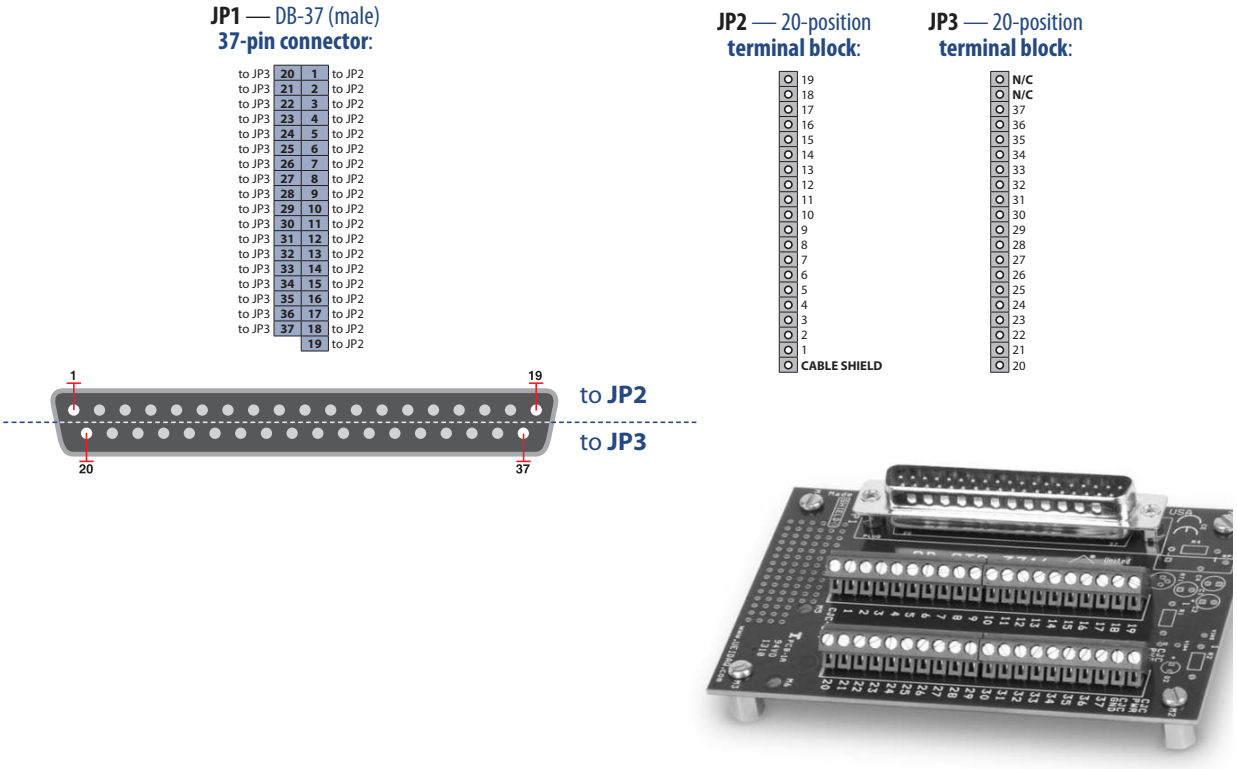


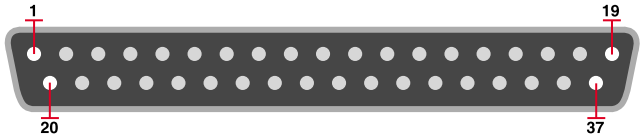
Figure A-1 Pinout and Photo of DNA-STP-37 Screw Terminal Panel

DNA-STP-AI-U

Universal screw-terminal panel designed for PowerDNA analog input boards. The panel offers a precision 5.000V reference with calibration, jumper-enabled RC filter on every channel, and voltage-excited RTD support.

J207/208 — DB-37 (male)
37-pin connector:

AIN-N15	20	1	DIO1/TRIG
AIN-N14	21	2	AIN-P15
+VA13/AGND	22	3	AIN-P14
AIN-P13	23	4	AIN-N13
AIN-P12	24	5	AIN-N12
AIN-P11	25	6	AIN-N11
AIN-P10	26	7	AIN-N10
AIN-N9	27	8	AGND
AIN-N8	28	9	AIN-P9
AIN-N7	29	10	AIN-P8
AIN-N6	30	11	AIN-P7
AIN-P24/AGND	31	12	AIN-P6
AIN-P5	32	13	AIN-N5
AIN-P4	33	14	AIN-N4
AIN-P3	34	15	AIN-N3
AIN-P2	35	16	AIN-N2
AIN-N1	36	17	AGND
AIN-N0	37	18	AIN-P1
		19	AIN-P0



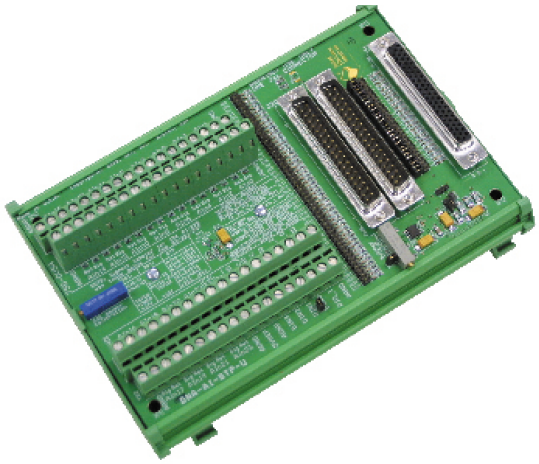


Figure A-2 Pinout and Photo of DNA-STP-AI-U Screw Terminal Panel