United Electronic Industries

The High-Performance Alternative

DNx-AI-254

—

User Manual

4-Channel LVDT/RVDT Interface Board for the PowerDNA Cube and RACK series chassis

November 2018

PN Man-DNx-AI-254

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Contacting United Electronic Industries

Mailing Address:

27 Renmar Avenue
Walpole, MA 02081
U.S.A.

For a list of our distributors and partners in the US and around the world, please contact a member of our support team:

Support:

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Fax: (508) 668-2350

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Chapter 1 Introduction

This document outlines the feature set and use of the DNx-AI-254 boards.

AI-254 boards are 4-channel LVDT/RVDT interface boards for the PowerDNA Cube and RACK chassis. The AI-254 provides 16-bit resolution and 4-, 5-, and 6-wire device support.

This chapter contains the following sections:

- Organization of Manual (Section 1.1)
- AI-254 Board Overview (Section 1.2)
- Features (Section 1.3)
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1.1 Organization of Manual

The AI-254 User Manual is organized as follows:

- **Introduction**
  This section provides an overview of the features, device architecture, connectivity, and logic of the AI-254 PowerDNx boards.
- **Programming with the High-Level API**
  This chapter provides an overview of the how to create a session, configure the session, and format relevant data using the Framework API.
- **Programming with the Low-Level API**
  This chapter provides an overview of low-level API commands for configuring and using the AI-254, including examples of each of the supported LVDT/RVDT operating modes.
- **Appendix A - Accessories**
  This appendix provides a list of accessories available for use with the AI-254 boards, including board adapters for voltage step-up transformer signal conditioning.
- **Index**
  This is an alphabetical listing of the topics covered in this manual.

NOTE: A glossary of terms used with the PowerDNA Cube/RACK and I/O boards can be viewed or downloaded from www.ueidaq.com.

Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:

Tips are designed to highlight quick ways to get the job done or to reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.

CAUTION! *Caution advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

Text formatted in **bold** typeface generally represents text that should be entered verbatim. For instance, it can represent a command, as in the following example: “You can instruct users how to run setup using a command such as **setup.exe**.”

Bold typeface will also represent field or button names, as in “Click **Scan Network**.”

Text formatted in `fixed` typeface generally represents source code or other text that should be entered verbatim into the source code, initialization, or other file.

Examples of Manual Conventions

Before plugging any I/O connector into the Cube or RACK chassis, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

No HOT SWAP

Always turn POWER OFF before performing maintenance on a UEI system. Failure to observe this warning may result in damage to the equipment and possible injury to personnel.

Usage of Terms

Throughout this manual, the term “Cube” refers to either a PowerDNA Cube product or to a PowerDNR RACKtangle™ rack mounted system, whichever is applicable. The term DNR is a specific reference to the RACKtangle, DNA to the PowerDNA I/O Cube, and DNx to refer to both.

1.2 AI-254 Board Overview

The DNx-AI-254 boards are 4-channel LVDT/RVDT analog inputs or simulated LVDT/RVDT outputs. The boards support a wide variety of linear and rotational motion and/or position measurements in industrial and military applications.

The DNA-AI-254, DNR-AI-254, and DNF-AI-254 boards are compatible with the UEI Cube, RACKtangle, and FLATRACK chassis respectively. All board versions are functionally identical except for the mounting hardware. The DNA version is designed to stack in a Cube chassis. The DNR/F versions are designed to plug into the backplane of a RACK chassis.

1.2.1 Channel Configuration

Each of the four channels on the AI-254 may be configured either as an LVDT/RVDT input interface with either internal or external excitation or as an LVDT/RVDT simulator output with external excitation. When programmed as in LVDT/RVDT simulator mode, the simulated outputs may be used as a software-controlled input stimulus for an avionics test system or flight simulator.

The wiring connections for the various modes of operation are described in detail in “Operating Modes” on page 11.

1.2.2 Input Channels

Each input channel has two programmable gain amplifiers and two 16-bit successive approximation ADCs (total of eight per board) that enable the channel to be used as two single-ended inputs or as one differential input pair.

1.2.3 Output Channels

Each output channel has two independent 16-bit DACs (total of eight per board) that permit the channel to be used for outputting two single-ended voltages or one differential voltage output pair. Each output channel may be configured to output a programmable excitation voltage to the primary of an LVDT/RVDT device or alternatively as the simulated output voltage from the secondary of an LVDT/RVDT. When used in simulator mode, the board uses a user-programmable value as the position input for a simulated LVDT/RVDT device.

The AI-254 is ideal for many applications. Where higher current and voltage are necessary, for 4-wire output requiring V_{rms} > 6.7V, or for 5-wire simulated output mode requiring V_{rms} > 3.4V, use the DNx-AI-256.

1.2.4 Displacement Calculations

The AI-254 calculates the LVDT/RVDT device position automatically at a rate equal to twice the frequency of the excitation voltage. The calculated values may be retrieved at any time or stored in a 256-sample FIFO. Each analog output can also generate pre-loaded voltage waveforms with programmable phase shift.

1.2.5 Isolation & Over-voltage Protection

Each board provides 350 V_{rms} isolation between channels and between the board and the chassis or any other installed boards. Boards also provide electro-shock-discharge (ESD) isolation. As with all UEI PowerDNA boards, the AI-254 is tested at 5*g* vibration, 50*g* shock, -40 to +85°C temperature, and altitudes up to 70,000 feet.

1.2.6 Software Support

Software for the AI-254 is provided as part of the UEI Framework. Framework provides a comprehensive, yet easy-to-use, API that is compatible with all popular Windows programming languages and that also supports programmers using Linux and most realtime operating systems such as QNX, RTX, or RT Linux. Also, UEI Framework can be used for creating applications in LabVIEW, MATLAB/Simulink, or any application that supports ActiveX or OPC servers.

1.3 Features

The common features of the AI-254 are listed below:

- Four channels individually configurable either as LVDT/RVDT inputs with internal or external excitation or as simulated outputs with external excitation
- Inputs and outputs configurable as 8 single-ended or 4 differential pair voltages
- $28V_{rms}$ input range (other ranges available)
- 1/2/5/10 programmable gain amplifiers on every input
- 16-bit resolution
- May be used with 4-, 5-, and 6-wire LVDT/RVDT devices
- Reference (excitation voltage) output for each channel
- 2 to 6.7 V_{rms} user-programmable excitation voltage for each channel
- User-programmable excitation frequency range of 100 Hz to 5 kHz for each channel
- Up to 50 mA excitation current without external buffering
- Isolation up to 350 V_{rms} between channel and between I/Os and GND
- Tested to withstand 5g vibration, 50g shock, -40 to +85°C temperature, and altitude up to 70,000 ft or 21,000 meters
- Weight of 136 g or 4.79 oz for DNA-AI-254; 817 g or 28.8 oz with PPC5
- UEI Framework Software API may be used with all popular Windows programming languages, RT Linux, RTX, or QNX, LabVIEW, MATLAB, and any application supporting ActiveX or OPC

1.4 Indicators

The AI-254 indicators are described in **Table 1-1** and illustrated in **Figure 1-1**.

Table 1-1 AI-254 Indicators

LED Name	Description
RDY	Indicates board is powered up and operational
STS	Indicates which mode the board is running in: • **OFF**: Configuration mode (e.g., configuring channels, running in point-by-point mode) • **ON**: Operation mode (e.g., running in DMap mode)

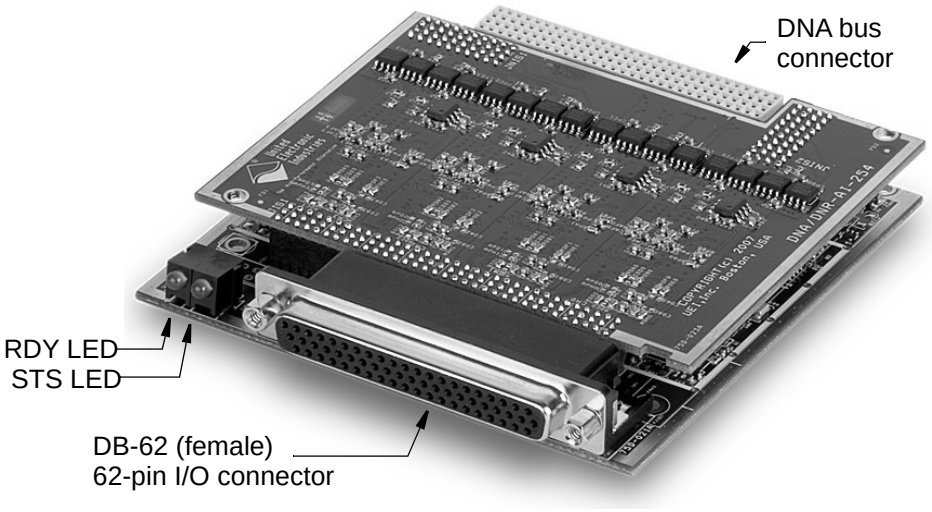


Figure 1-1 Photo of DNA-AI-254 Board

1.5 Specification

Technical specifications for the DNx-AI-254 board are listed in **Table 1-2**:

Table 1-2 . DNx-AI-254 Technical Specification

Inputs	
Number of channels	4
Configuration	Supports all common input/excitation configurations (e.g. 4, 5 and 6-wire)
Resolution	16-bit
Accuracy	0.1%
Input Impedance	100 kOhm
Maximum input voltage	28 Vrms (requires external excitation above 6.7 Vrms)
Excitation Frequency	100 Hz to 5.0 kHz, programmable with 1 Hz resolution, ±0.1 % overall accuracy
Excitation Voltage	2-6.7 Vrms, programmable with 0.05 Vrms resolution, ±0.1% overall accuracy
Excitation Drive	50 mA at 6.7 Vrms
Primary Impedance	130 Ohm min at 6 Vrms
Update rate	Up to 1 times the excitation frequency. The default rate is 1/10 the excitation frequency
Simulation Outputs	
Number of channels	4
Configuration	2-, 3- or 4-wire
Resolution	16-bit
Output Accuracy	0.1%
Output Voltage	2 to 6.7 Vrms (3-wire simulated outputs requiring greater than 3.35 VRMS will require an external transformer coupler. For larger outputs please see the DNx-AI-256)
Output Drive Current	50 mA max

1.6 Device Architecture

A block diagram of the AI-254 board is shown in **Figure 1-2**. The AI-254 board provides four channels that can be independently configured as either an LVDT/RVDT input interface with either internal or external excitation or as an LVDT/RVDT simulator output with external excitation.

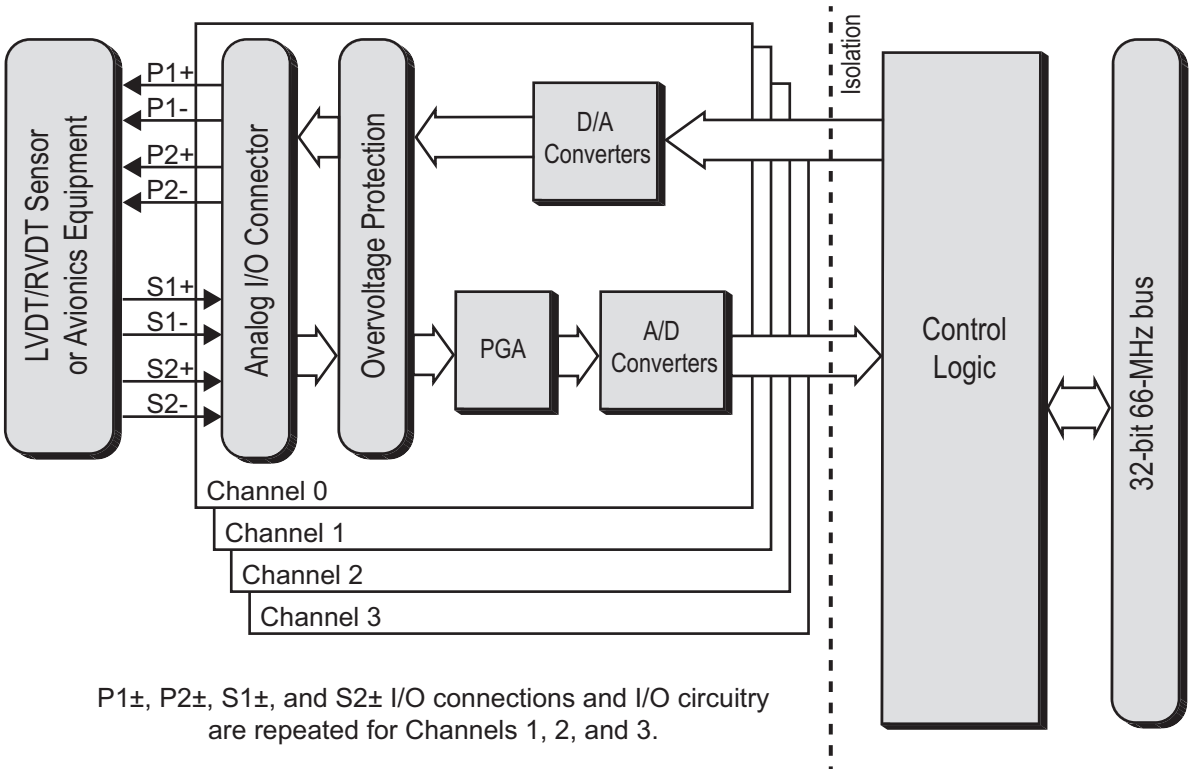


Figure 1-2 Block Diagram of a Channel on the AI-254 I/O Board

The board logic is divided into isolated and non-isolated sections. The non-isolated side converts between the LVDT/RVDT analog signal(s) and digital samples across an optoelectronic isolation barrier to the control logic, which includes a sample buffer and bus transfer that uses the UEI Common Logic Interface standard.

The DNx-AI-254 is physically a two-board module composed of a base board plus an AI-254-specific daughter board (refer to **Figure 1-1** on page 5). The DNA- and DNR- versions of the base board are functionally the same except for the bus connectors used. AI-254 LVDT/RVDT simulation output functionality is similar to the 2-channel, higher-current, higher-frequency, higher-voltage AI-256 board.

1.6.1 Functional Description

As shown in Figure 1-2, each of the four channels is designed to operate as an independent multi-function data acquisition system.

Each channel can be configured as either a 4-, 5-, or 6-wire LVDT/RVDT analog input channel that connects to an LVDT/RVDT sensor or as an output/simulator, which can be used to drive simulator inputs or to test LVDT/RVDT measurement products.

When a channel is configured as an LVDT/RVDT analog input channel, the channel is designed to supply a user-programmable AC excitation to the primary winding of a single LVDT or RVDT sensor while accepting AC analog voltage input signals from the two secondary windings of the sensor.

As an alternative, the channel can be configured to operate with excitation supplied from an external source instead of generated internally to the AI-254. In such cases, the excitation voltage is read as an input to the AI-254 channel and used as a reference for computation of the sensor core position.

A summary of the AI-254 modes of operation is provided in **Table 1-3**:

Table 1-3 AI-254 Modes of Operation

Mode	Analog Input or Simulated Output	Sensor Wire Configuration	Internal or External Excitation	Section Reference
Mode 0 DQ_AI254_MODE_INT_5	Analog Input Mode	5- or 6-wire	Internal Excitation	Section 1.8.1.2
Mode 1 DQ_AI254_MODE_INT_4	Analog Input Mode	4-wire	Internal Excitation	Section 1.8.1.1
Mode 2 DQ_AI254_MODE_EXT_5	Analog Input Mode	5- or 6-wire	External Excitation	Section 1.8.2.2
Mode 3 DQ_AI254_MODE_EXT_4	Analog Input Mode	4-wire	External Excitation	Section 1.8.2.1
Mode 4 DQ_AI254_MODE_SIM_5	Simulated Output	5- or 6-wire*	External Excitation	Section 1.8.3.2
Mode 5 DQ_AI254_MODE_SIM_4	Simulated Output	4-wire	External Excitation	Section 1.8.3.1

NOTE: *When simulating a 5-wire LVDT/RVDT sensor, the AI-254 P1 and P2 outputs provide a maximum output voltage of 3.4 V_{rms} instead of the differential 6.7 V_{rms}.

Functional descriptions of analog input mode and simulator out mode are provided in the following sections. Examples of each mode of operation and required AI-254 pin connectivity are described in detail in Section 1.8.1.1 thru Section 1.8.3.2.

1.6.1.1 Analog Input Mode

When a channel is configured as an LVDT/RVDT analog input device, the voltages on the secondary windings of the sensor are connected as single-ended AC analog inputs to the AI-254 through S1± and S2±. These input signals are fed to two amplifiers with a user-programmable gains of 1, 2, 5, or 10. The single-ended signals are then converted to differential pairs for input to successive approximation A/D converters running in parallel at up to 330 kHz each. The output of the ADC is represented as a 16-bit digital word.

The analog voltage inputs from the two secondary windings are converted by the ADCs and continuously integrated/divided to compute the moving averages of both inputs.These average values are called Sa and Sb, one for each secondary winding. The readings of the excitation voltage applied to the primary winding are also averaged to compute the averaged excitation value, Se.

Either the Sa and Sb input, or the input with the highest amplitude, is monitored for a desired direction of zero crossing. When a zero crossing is detected, Sa, Sb, and Se are latched and the values are further processed to compute the 24-bit values (Sa-Sb)/(Sa+Sb) and/or (Sa-Sb)/Se. Results are then adjusted as needed with a 24-bit gain and offset. These values are also used to compute the physical position of the magnetic core within the LVDT/RVDT sensor. The computed results are then passed to the averaging/decimation engine, the output of which is stored in the FIFO for the channel.

The following values are also stored in the FIFO:

- Timestamp
- Raw value
- Calibrated value
- Averaged position
- Sa and/or Sb
- ADC raw values of the last conversion
- Watermark
- Data
- Count

1.6.1.2 Simulator Output Mode

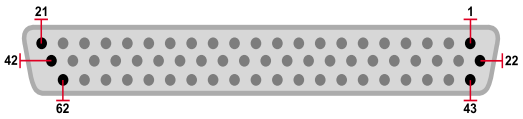
When a channel is configured as a simulator output device, the channel simulates the operation of the secondary windings of an LVDT/RVDT sensor. In this mode, the DAC generates analog voltages on P1± and P2± to represent the output voltages of LVDT/RVDT secondary windings. Refer to **Figure 1-8** on page 16 and **Figure 1-9** on page 17 for diagrams of using an AI-254 as a simulated 4-wire device and a simulated 5-/6-wire device.

The channel outputs can also be configured to generate a user-defined custom analog waveform output signal on the P1± and P2± terminals, normally used for LVDT/RVDT excitation voltage. (Refer “Use of Custom Waveform Output for Excitation” on page 18.)

Timing of the analog waveform output is controlled by detecting zero crossings of the analog input on the channel.

1.7 Connectors and Wiring (Pinout)

Figure 1-3 shows the pinout of the 62-pin female connector for the AI-254:



	Pin	Signal	Pin	Signal	Pin	Signal
Chan 0	1	Rsvd	22	Gnd	43	P1-
	2	P2+	23	P2-	44	P1+
	3	Rsvd	24	n/c	45	Gnd
	4	S1+	25	S1-	46	Rsvd
	5	S2+	26	S2-	47	n/c
Chan 1	6	Gnd	27	Rsvd	48	Rsvd
	7	P1+	28	P1-	49	Rsvd
	8	P2+	29	P2-	50	Rsvd
	9	S1+	30	S1-	51	Gnd
	10	S2+	31	S2-	52	Rsvd
Chan 2	11	Rsvd	32	n/c	53	P1-
	12	P2+	33	P2-	54	P1+
	13	Rsvd	34	Gnd	55	Gnd
	14	S1+	35	S1-	56	Rsvd
	15	S2+	36	S2-	57	n/c
Chan 3	16	Gnd	37	Rsvd	58	Rsvd
	17	P1+	38	P1-	59	n/c
	18	P2+	39	P2-	60	Rsvd
	19	Rsvd	40	Gnd	61	S1-
	20	S2+	41	S2-	62	S1+
	21	Rsvd	42	n/c		

Figure 1-3 DNx-AI-254 LVDT/RVDT Pinout Diagram

NOTE:

1. Use S1+ and S1- for S1 secondary analog differential input connections. When the AI-254 is configured in simulator output mode, S1+ and S1- are used to measure the excitation reference voltage.
2. Use S2+ and S2- for S2 secondary analog differential input connections.
3. P1+ and P1- represent the output of two independent DACs. They may be used as two single-ended voltage outputs or together as a single differential output voltage at twice the DAC output. When the AI-254 is configured for internal excitation, they are normally used to provide the excitation voltage for an LVDT/RVDT device. When the AI-254 is configured in simulator output mode, P1+ and P1- are used to provide one of the two simulated measurement outputs (S1 secondary winding).
4. P2+ and P2- represent the output of two independent DACs. They may be used as two single-ended voltage outputs or together as a single differential output voltage at twice the DAC output voltage. When the AI-254 is configured for internal excitation, they are normally not used or connected. When the AI-254 is configured in simulation mode, P2+ and P2- are used to provide the second of the two simulated measurement outputs (S2 secondary winding).

The following table is provided as a convenient reference for connecting sensors to the various I/O pins.

Table 1-4 DNx-AI-254 Pin Connections by Channel Number

Signal	Ch 0	Ch 1	Ch2	Ch 3
P1+	44	7	54	17
P1-	43	28	53	38
P2+	2	8	12	18
P2-	23	29	33	39
S1+	4	9	14	62
S1-	25	30	35	61
S2+	5	10	15	20
S2-	26	31	36	41
Rsvd	1, 3, 27, 46	48, 49, 50, 52	11, 13, 37, 56	19, 21, 58, 60
NC	24, 27, 47	32	57	42, 59
Gnd	22, 45	6, 51	34, 55	16,40

1.8 Operating Modes

The AI-254 can be used in any of six operating modes, as follows:

- (Mode 0) Analog input mode with internal excitation connecting to a 5/6-wire LVDT/RVDT sensor
- (Mode 1) Analog input mode with internal excitation connecting to a 4-wire LVDT/RVDT sensor
- (Mode 2) Analog input mode with external excitation connecting to a 5/6-wire LVDT/RVDT sensor
- (Mode 3) Analog input mode with external excitation connecting to a 4-wire LVDT/RVDT sensor
- (Mode 4) Simulation of the outputs of a 5/6-wire LVDT/RVDT with external excitation
- (Mode 5) Simulation of the outputs of a 4-wire LVDT/RVDT with external excitation

The AI-254 can be used to self-test inputs and outputs by connecting a simulation channel directly to a separate input channel, (e.g., 4-wire analog input mode with internal excitation on channel 0 wired to 4-wire simulator output mode on channel 1). For more information, refer “Simulator Output to LVDT/ RVDT Input Mode” on page 19.

1.8.1 Analog Input Mode with Internal Excitation (Mode 0 and Mode 1)

When an AI-254 channel is configured as an analog input board with internally supplied excitation, the channel can generate an independent user-programmable excitation voltage from 2 to 6.7 V_{rms} at a frequency that may be set between 100 and 5000 Hz. Each excitation source can drive up to 50 mA without external buffering and can drive primary impedances as low as 130 ohms at excitation voltages up to 6.7 V_{rms}.

1.8.1.1 4-wire configuration (Mode 1)

The output signals from the secondaries of the LVDT/RVDT sensors are connected as analog inputs to the AI-254. For a 4-wire device (Mode 1), the output signal from the secondary (V_{out}) is connected to S1+ and S1-, as shown in **Figure 1-4**.

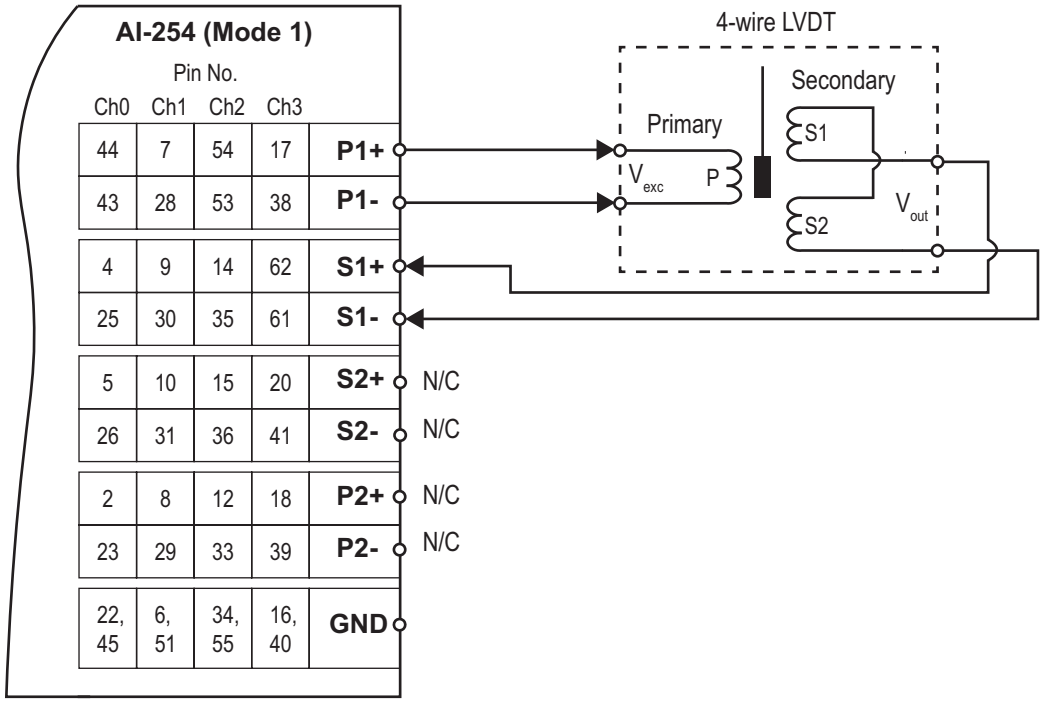


Figure 1-4 4-wire LVDT Device with AI-254 in Analog Input Mode, Internal Excitation

1.8.1.2 5/6-wire configuration (Mode 0)

For a 6-wire device (Mode 0), the S_a signal from the S1 secondary winding is connected to S1+ and S1- and the S_b signal from S2 winding is connected to S2+ and S2-, as shown in **Figure 1-5**.

For a 5-wire device, connect S1+ and S2+ with the same configuration as the 6-wire device (**Figure 1-5**), but connect S1- and S2- to the common of the sensor's secondary windings.

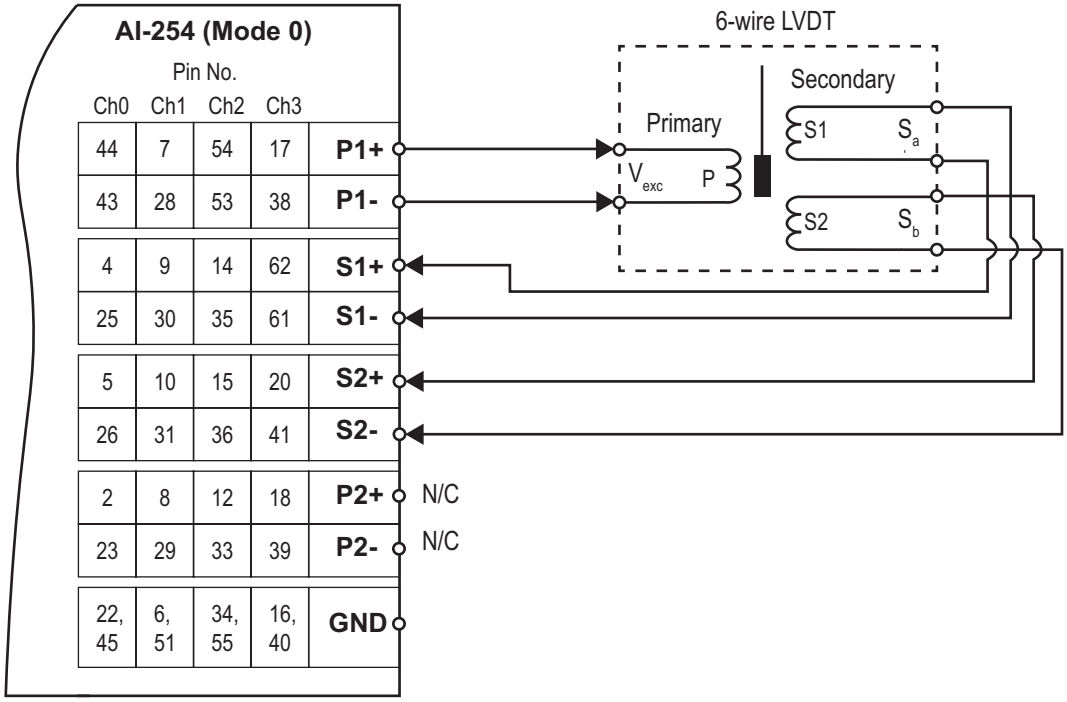


Figure 1-5 6-wire LVDT Device with AI-254 in Analog Input Mode, Internal Excitation

1.8.2 Analog Input Mode with External Excitation (Mode 2 and Mode 3)

When an AI-254 channel is configured as an analog input board with externally supplied excitation, the P1± and P2± output pins are not used and not connected to the LVDT/RVDT sensor. The excitation voltage is supplied externally and used as the V_{ref} reference to the sensor. The V_{ref} is also supplied externally to the S2± terminals of the AI-254 in 4-wire mode.

1.8.2.1 4-wire configuration (Mode 3)

In the LVDT/RVDT 4-wire configuration, the AI-254 requires the V_{ref} as an input to compute the core displacement and is supplied to the channel via the S2± input pins.

The output signals from the secondary windings of the LVDT/RVDT sensor are connected as analog inputs to the AI-254. For a 4-wire device (Mode 3), the output signal from the secondary (V_{out}) is connected to S1+ and S1-, as shown in **Figure 1-6**.

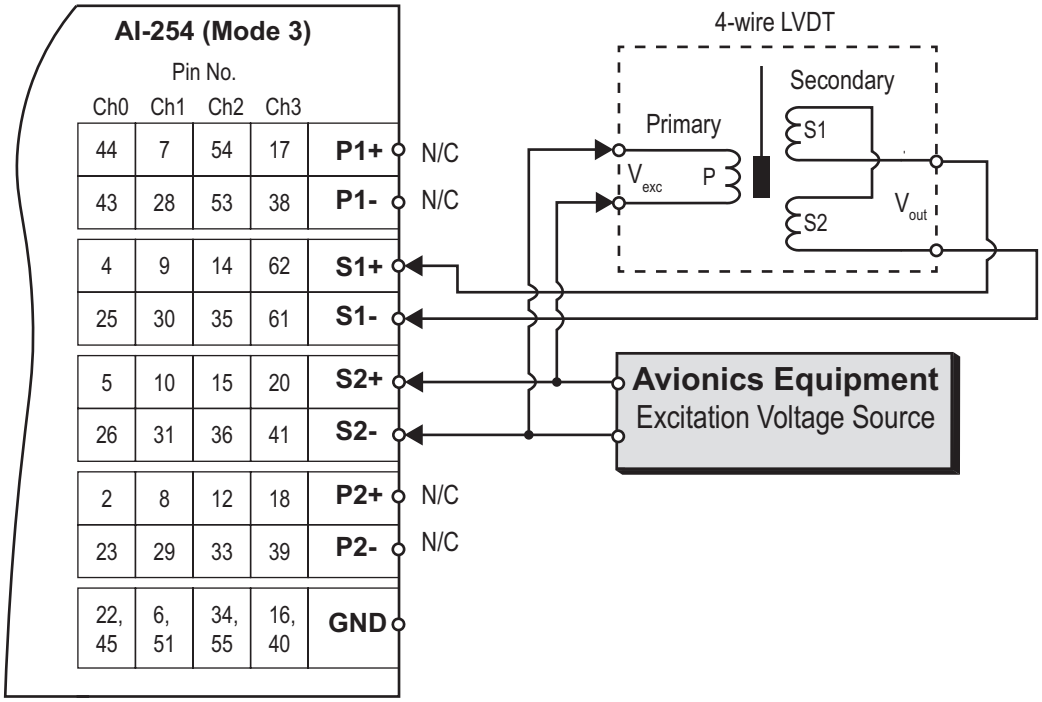


Figure 1-6 4-wire LVDT Device with AI-254 in Analog Input Mode External Excitation

1.8.2.2 5/6-wire configuration (Mode 2)

For a 6-wire device (Mode 2), the S_a signal from S1 secondary, is connected to S1+ and S1-, and the S_b signal from S2 is connected to S2+ and S2-, as shown in **Figure 1-7**. The external V_{ref} excitation voltage is not connected to the AI-254 channel in the Mode 2, 5-/6-wire configuration. Core position is calculated exclusively from the S_a and S_b values.

For a 5-wire device, S1+ and S2+ are connected with the same configuration as the 6-wire device (**Figure 1-7**), but S1- and S2- are connected to the common of the sensor's secondary windings.

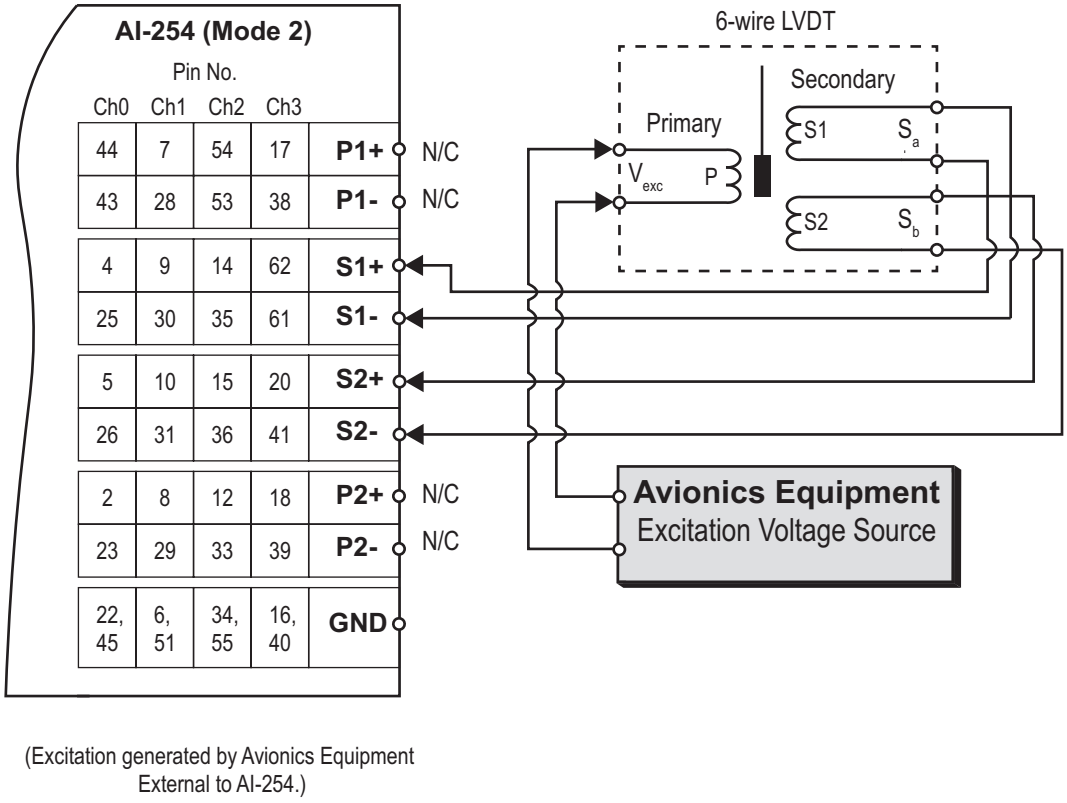


Figure 1-7 6-wire LVDT Device with AI-254 in Analog Input Mode, External Excitation

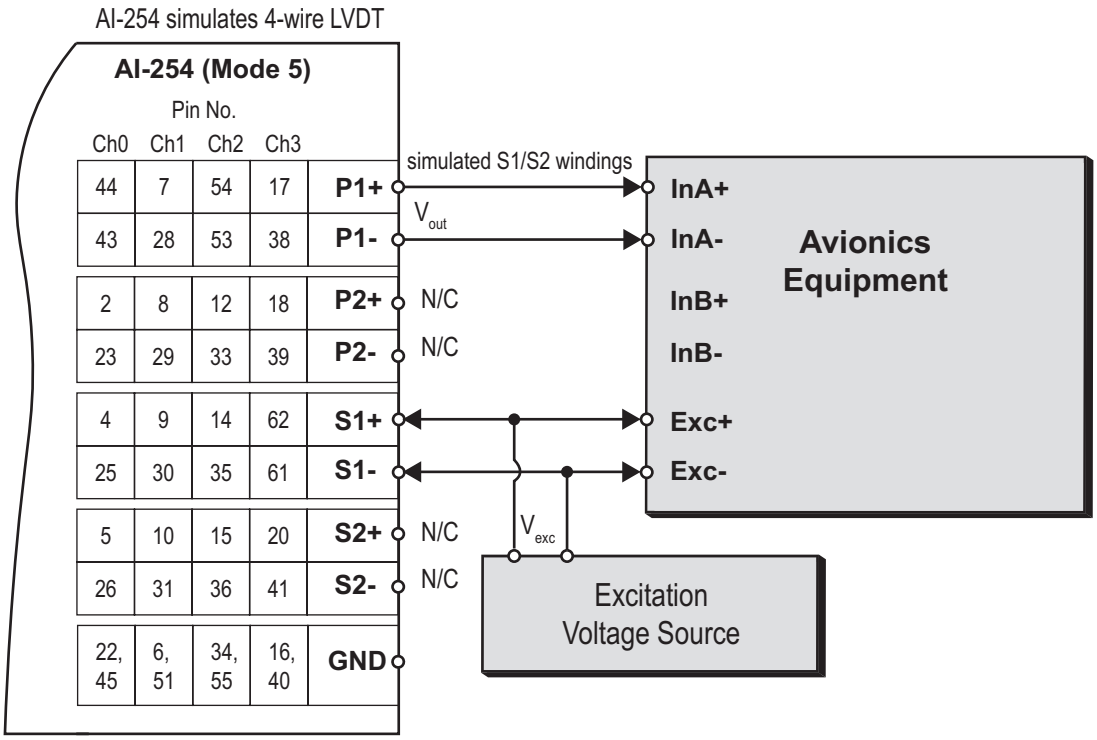
1.8.3 Simulator Output Mode with External Excitation (Mode 4 and Mode 5)

When an AI-254 channel is configured as an LVDT/RVDT simulator output (Mode 4 and Mode 5), the channel outputs provide signals with 16-bit resolution that simulate the two secondary outputs of an LVDT/RVDT, producing voltages that correlate to the calculated position of the magnetic core of a software simulated LVDT/RVDT device.

Excitation voltage is supplied from an external source both to the avionics equipment and to the S1- and S1+ pins on the AI-254, where it used as a reference.

1.8.3.1 4-wire configuration (Mode 5)

When simulating a 4-wire LVDT/RVDT sensor, the AI-254 channel configured as a simulator output drives signals from P1± that simulate the secondary windings of the LVDT/RVDT, as shown in **Figure 1-8**. The excitation voltage is provided external to the AI-254 channel and connected to S1±.



(AI-254 simulates the secondary windings of an LVDT sensor. Position is software defined. Excitation generated External to AI-254.)

Figure 1-8 4-wire LVDT Device with AI-254 in Simulator Mode

1.8.3.2 5/6-wire configuration (Mode 4)

When simulating a 6-wire LVDT/RVDT sensor, the AI-254 channel configured as a simulator output drives signals from P1± and P2± to simulate the secondary windings of the LVDT/RVDT, as shown in **Figure 1-9**. The excitation voltage is provided external to the AI-254 channel and connected to S1±.

When simulating a 5-wire LVDT/RVDT sensor, P1- and P2- should be disconnected from the Avionics Equipment, which yields a maximum output voltage of 3.4 V_{rms} instead of the differential 6.7 V_{rms}.

.

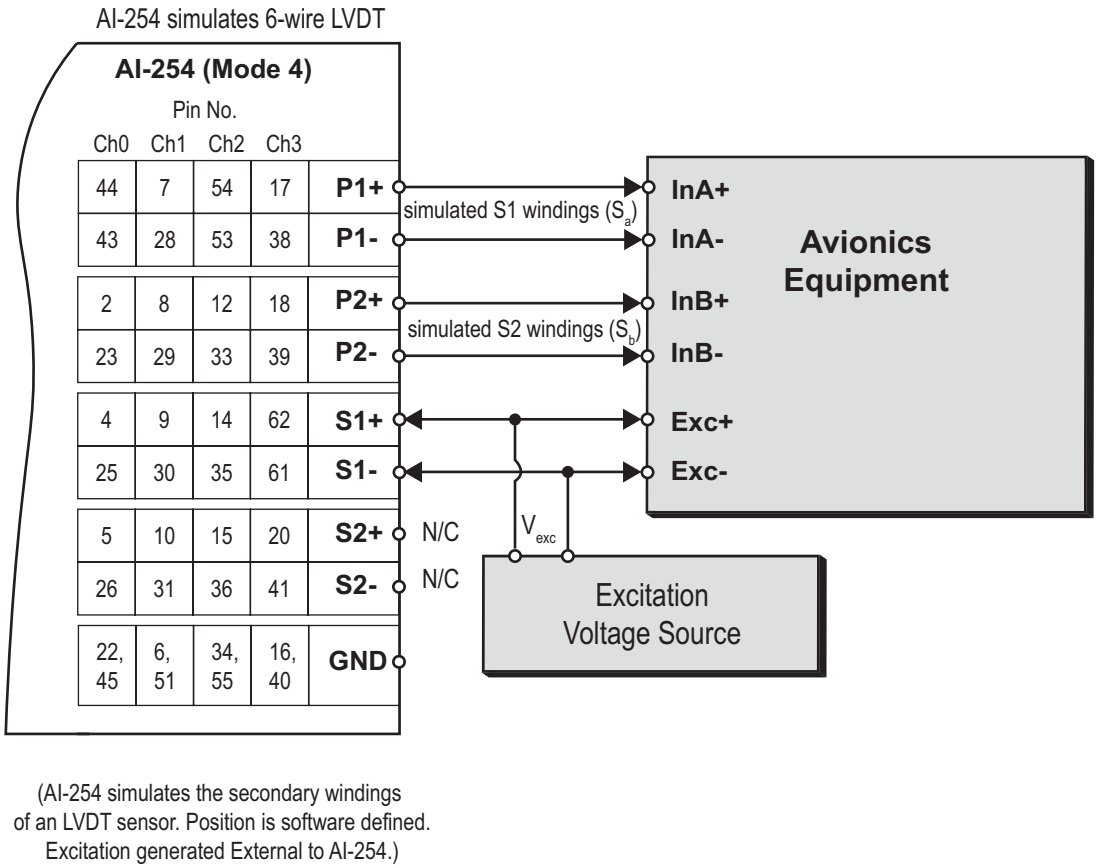


Figure 1-9 6-wire LVDT Device with AI-254 in Simulator Output Mode, External Excitation

In 5-wire simulation mode, P1+ and P2+ from the AI-254 simulate the Sa+ and Sb+ output voltages of an LVDT/RVDT sensor. The 5-wire common node on the avionics equipment will be connected to channel ground while the P1- and P2- of the AI-254 must be left open as no connects. Note that each P1 and P2 output channel uses two independent 16-bit DACs for outputting a differential voltage output pair. Because the negative AI-254 output DAC is not used in the 5-wire simulation configuration, the output voltage is limited to $3.4V_{rms}$, half the full-scale $6.7V_{rms}$.

If your system requires a higher voltage, consider using the AI-256, a 2-channel LVDT/RVDT board, or consider using a transformer card. Transformer cards are described in Appendix A on page 33.

1.8.4 Use of Custom Waveform Output for Excitation

AI-254 channels configured as Mode 0 or Mode 1 provide the capability of internally generating an excitation voltage used by an LVDT/RVDT sensor.

To initialize the parameters of the AC excitation source, users programming with low-level API can use the AI-254-specific function, **DqAdv254SetExcitation().** This function sets up the internal excitation frequency and V_{pp} amplitude.

In some situations, such as testing the effect of a particular harmonic in an excitation signal, it may be useful to use a custom waveform (with programmable phase shift) instead of a standard sine wave for the excitation signal.

In such cases, you can use the **DqAdvSetWForm()** function instead of the **DqAdv254SetExcitation()** function. The AI-254 will then output the custom waveform on excitation channels P1 and/or P2. For detailed information, refer to **Chapter 2** and **Chapter 3** of this manual, to the UEI Framework Reference Manual, or to the UEI PowerDNA API Reference Manual.

In addition to the six standard modes of operation (**Table 1-3** above), the AI-254 can also be used in a supervisory configuration to monitor the performance of an LVDT/RVDT device. This mode is similar to a “wire tapping” application in which an instrument is used to record and analyze operation of an active device.

If configured as a parallel-connected monitor of an LVDT/RVDT device with internal (AI-254-supplied) excitation, signals are transmitted from the device to both the AI-254 and to the avionics in parallel. Excitation voltage is supplied to the device from the AI-254 and is also connected to the avionics in parallel (P1+ and P1- connected to Exc+ and Exc-), as shown in **Figure 1-10**. In this manner, the avionics can continuously monitor operation of the LVDT/RVDT device.

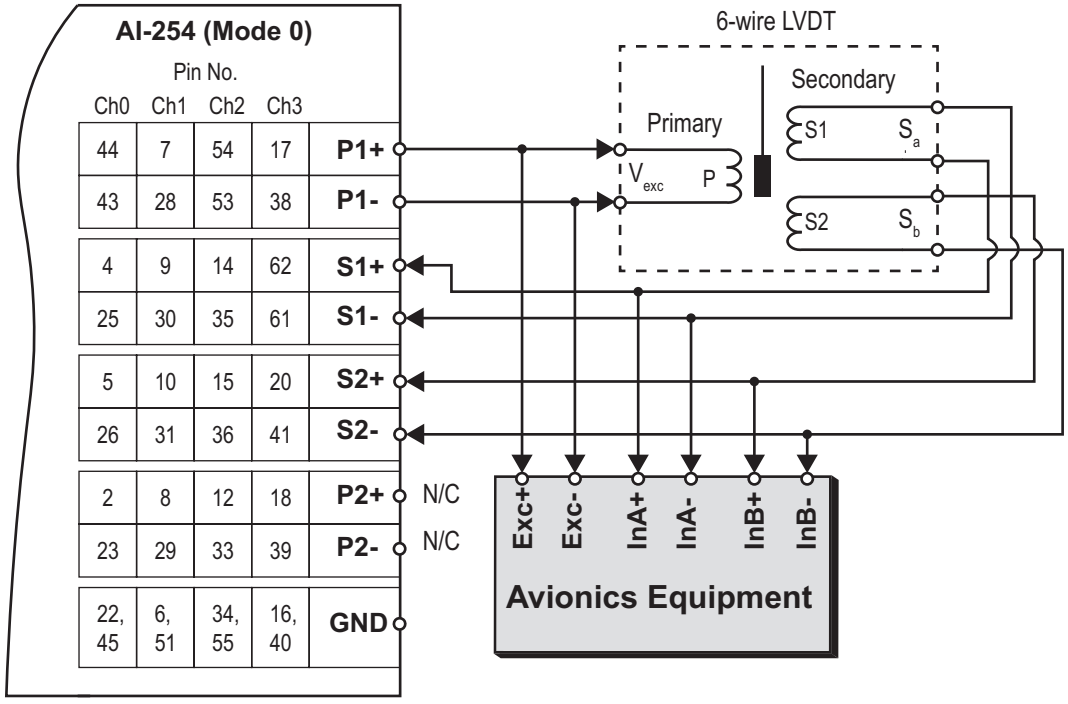


Figure 1-10 6-wire LVDT Device with AI-254 in Parallel Monitor Mode, Internal Excitation

1.8.5 Simulator Output to LVDT/RVDT Input Mode

The AI-254 can be configured to use one or more channels as simulator outputs (Mode 4 or Mode 5) and connect them to one or more channels configured as LVDT/RVDT input interfaces (Mode 0, Mode 1, Mode 2, or Mode 3) on the same or different AI-254 boards, as shown in **Figure 1-11**.

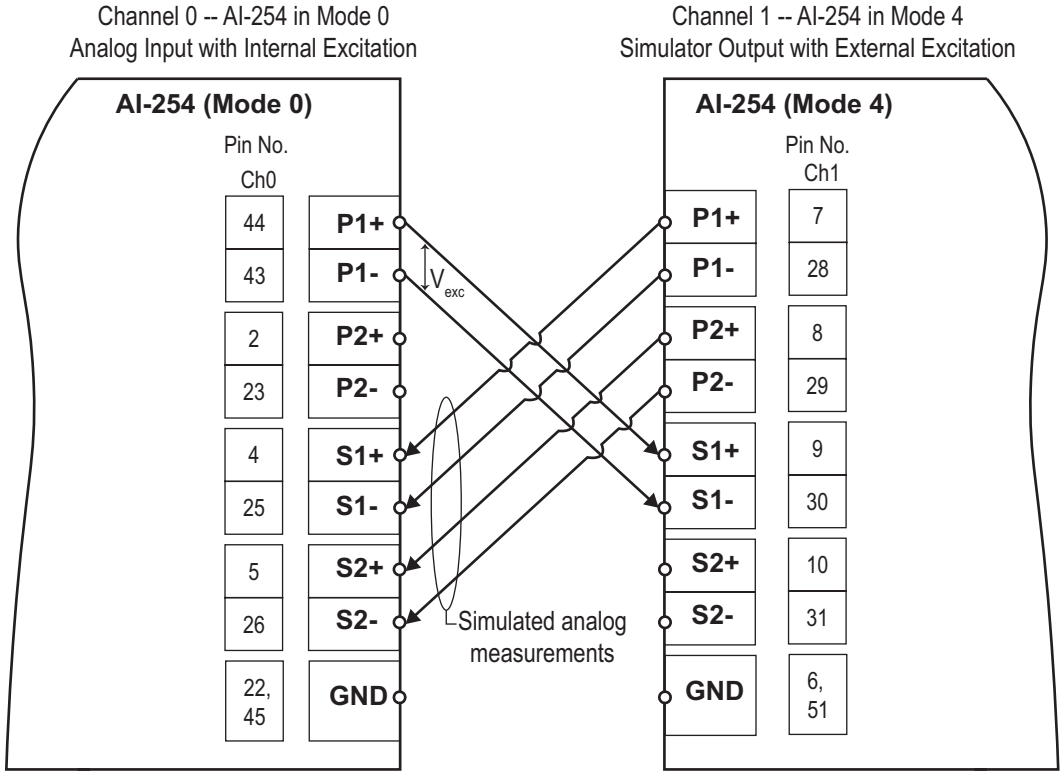


Figure 1-11 Ch1 Simulation Mode 4 Connected to Ch0 in Analog Input Mode 0 (6-wire)

As shown in the diagram, excitation voltage is provided by Channel 0 (P1+ to P1-) DAC. The Channel 0 (P2+ to P2-) DAC output is zero. Channel 1 outputs two simulated measurement signals (P1+ to P1-) and (P2+ to P2-) from its DACs to the secondary inputs on Channel 0.

1.9 Setting Operating Parameters

For detailed instructions for configuring the board and setting operating modes and parameters for AI-254, refer to the Framework function **CreateSimulatedLVDTChannel()** or the low-level API functions **DqAdv254SetMode()** and **DqAdv254SetExcitation()**.

Refer to **Chapter 2** to and the Framework API Reference Manual for more information regarding framework functions.

Refer to **Chapter 3** and to the PowerDNA API Reference Manual for more information regarding low-level API functions.

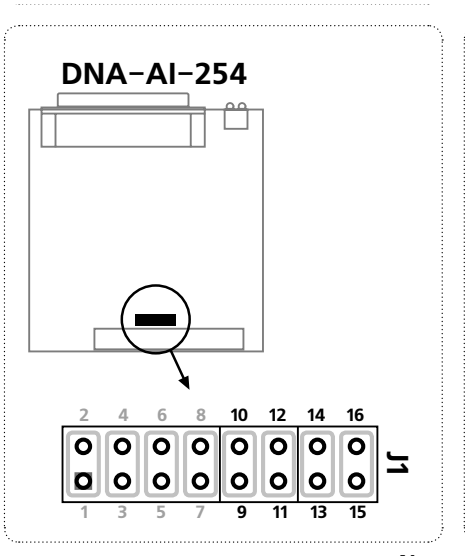
1.10 Jumper Settings for Board Position

This section briefly describes how to change jumper positions that indicate physical board positioning in the uncommon case that you must physically swap boards on the PowerDNA I/O Cube. Jumpers do not apply to boards in the RACK chassis.

All boards are assembled in Cubes with identifying labels before shipment, so you should never have to change a jumper setting unless you have to change a board from one physical position to another in the field.

Figure 1-12 shows the physical layout of DNA-AI-254 Board, highlighted to show the 16-pin jumper block for setting the board position within a PowerDNA Cube.

NOTE: Board position jumpers are not provided with the DNR versions of the AI-254. The physical position of the board within the DNR RACKTangle™ enclosure is determined automatically by the system.



See **Figure 1-13** for placement of jumpers for various board positions in a Cube.

Figure 1-12 Jumper Block for DNA-AI-254 Board Position

A diagram of the jumper block is shown in **Figure 1-13** To set the board position jumpers, place jumpers as shown in **Figure 1-13**

		Layer's Position as marked on the Faceplate*					
		I/O **1**	I/O **2**	I/O **3**	I/O **4**	I/O **5**	I/O **6**
Jx Pins	9-10	■	□	■	□	■	□
	11-12	■	■	□	□	■	■
	13-14	■	■	■	■	□	□
	15-16	■	■	■	■	■	■

* *All I/O Layers are sequentially enumerated from top to the bottom of the Cube*

□ - **Open** ■ - **Closed**

Figure 1-13 Diagram of DNA-AI-254 Board Position Jumper Settings

Chapter 2 Programming with the High-Level API

This chapter provides the following information about using the UeiDaq Framework High-Level API to control the AI-254:

- Creating a Session (Section 2.1)
- Configuring the Resource String (Section 2.2)
- Configuring for LVDT/RVDT Input (Section 2.3)
- Configuring for Simulated LVDT Output (Section 2.4)
- Configuring the Timing (Section 2.5)
- Reading Data (Section 2.6)
- Writing Data (Section 2.7)
- Cleaning-up the Session (Section 2.8)

UeiDaq Framework is object oriented and its objects can be manipulated in the same manner from different development environments, such as Visual C++, Visual Basic, or LabVIEW.

The following section focuses on the C++ API, but the concept is the same no matter what programming language you use.

Please refer to the “UeiDaq Framework User Manual” for more information on use of other programming languages.

2.1 Creating a Session

The Session object controls all operations on your PowerDNx device. The first task when programming using the high-level Framework is to create a session object:

```
// create a session object for input, and a session object for output

CUeiSession aiSession;
CUeiSession aoSession;
```

2.2 Configuring the Resource String

UeiDaq Framework uses resource strings to select which device, subsystem and channels to use within a session. The resource string syntax is similar to a web URL:

```
<device class>://<IP address>/<Device Id>/<Subsystem><Channel list>
```

For PowerDNA and RACKtangle, the device class is **pdna**.

For example, the following resource string selects analog output lines 0,1,2,3 on device 1 at IP address 192.168.100.2: “pdna://192.168.100.2/Dev1/Ao0:3”

2.3 Configuring for LVDT/ RVDT Input

The method `CreateLVDTChannel()` is used to program the input channels and parameters associated with each channel:

The following call configures the Analog input channels of an AI-254 set as device 1:

```
// Configure session synchro/resolver input

aiSession.CreateLVDTChannel("pdna://192.168.100.2/Dev1/Ai0:1",
                            -2.5,              //Minimum range
                            2.5,               //Maximum range
                            153.65,            //Sensor sensitivity
                            UeiLVDTFiveWires,  //Wiring scheme
                            3.0,               //Excitation voltage
                            5000.0,            //Excitation frequency
                            false);            //External excitation
```

`CreateLVDTChannel()` configures the following parameters:

- **Minimum range:** minimum value you expect to measure.
  The unit is the distance unit specified by your LVDT sensitivity. For example, if your LVDT sensitivity is given in mV/V/mm, the distance unit is mm. Similarly for RVDTs the unit is the angle unit used in the sensitivity.
- **Maximum range:** maximum value you expect to measure.
  The unit is the position unit specified by your LVDT sensitivity. For example if your LVDT sensitivity is given in mV/V/mm, the distance unit is mm. Similarly for RVDTs, the unit is the angle unit used in the sensitivity.
- **Sensor Sensitivity:** the sensor sensitivity specified in mV/V/<position unit>.
  The position unit specifies the unit of the min. and max. range as well as the unit of the data read from the input channels.
- **Wiring Scheme:** the wiring scheme used to connect the LVDT/RVDT to the AI-254.
- **Excitation voltage:** the amplitude in volt RMS of the excitation sine wave.
- **Excitation frequency:** the frequency of the excitation sine wave.
- **External excitation:** specifies whether you wish to provide external excitation or use the excitation provided by the AI-254.

If you want to use different parameters for each channel, you can call `CreateLVDTChannel( )` multiple times with a different set of channels in the resource string each time.

2.4 Configuring for Simulated LVDT Output

The AI-254 can be used to simulate an LVDT or RVDT output.

The following call configures an analog output channel on an AI-254 set as device 1:

```
// Configure session for synchro/resolver output

aoSession.CreateSimulatedLVTDChannel(
                          "pdna://192.168.100.2/Dev1/AO0",
                          153.65               //Sensor sensitivity
                          UeiLVDTFiveWires,    //Wiring scheme
                          3.0,                 //Excitation voltage
                          5000.0);             //Excitation frequency
```

`CreateSimulatedLVTDChannel()` configures the following parameters:

- **Sensor Sensitivity**: the sensor sensitivity specified in mV/V/<position unit>. The position unit specifies the unit of the data written to the channel.
- **Wiring Scheme**: the wiring scheme used to connect the simulated LVDT/RVDT to the reading device.
- **Excitation Voltage**: the amplitude in volt RMS of the excitation sine wave.
- **Excitation Frequency**: the frequency of the excitation sine wave.

2.5 Configuring the Timing

You can configure the AI-254 to run in simple mode (point by point) or DMAP mode.

- In simple mode, the delay between samples is determined by software on the host computer.
- In DMAP mode, the delay between samples is determined by the AI-254 on-board clock. Data is transferred one scan at a time between PowerDNA and the host PC.

The following sample shows how to configure the simple mode. Please refer to the “UeiDaq Framework User’s Manual” to learn how to use other timing modes.

```
// configure timing of input for point-by-point (simple mode)

aiSession.ConfigureTimingForSimpleIO();

// configure timing of output for point-by-point (simple mode)

aoSession.ConfigureTimingForSimpleIO();
```

2.6 Reading Data

Reading data is done using *reader* object(s). The following sample code shows how to create a scaled reader object and read samples.

```
// create a reader and link it to the analog-input session’s stream
CUeiAnalogScaledReader aiReader(aiSession.GetDataStream());
// the buffer must be big enough to contain one value per channel
double data[2];
// read one scan
aiReader.ReadSingleScan(data);
```

2.7 Writing Data

Writing data is done using a *writer* object.

The following sample shows how to create a scaled writer and write samples. The AI-254 simulates angle positions entered in radians.

```
// create a writer and link it to the session’s analog-output stream
CUeiAnalogScaledWriter aiWriter(aoSession.GetDataStream());
// to write a value, the buffer must contain one value per channel
double data[2] = { 1.0, 2.0 };
// write one scan, the buffer must contain one value per channel
aoWriter.WriteSingleScan(data);
```

2.8 Cleaning-up the Session

The session object will clean itself up when it goes out of scope or when it is destroyed. To reuse the object with a different set of channels or parameters, you can manually clean up the session as follows:

```
// clean up the sessions
aiSession.CleanUp();
aoSession.CleanUp();
```

Chapter 3 Programming with the Low-Level API

The low-level API provides direct access to the DAQBIOS protocol structure and registers in C. The low-level API is intended for speed-optimization, for programming unconventional functionality, or when programming under Linux or real-time operating systems.

When programming in Windows OS, however, we recommend that you use the UeiDaq Framework High-Level API (see **Chapter 2**). The Framework extends the low-level API with additional functionality that makes programming easier, faster, and less error-prone.

For additional information regarding low-level programming, refer to the "PowerDNA API Reference Manual" located in:

- For Linux:
  <PowerDNA-x.y.z>/Documentation
- For Windows:
  Start » All Programs » UEI » PowerDNA » Documentation

This chapter provides the following information about programming the AI-254 using the low-level API:

- Low-level Functions (Section 3.1)
- Modes of Operation (Section 3.2)
- Low-level Programming Techniques (Section 3.3)

AI-254 board is an all-digital LVDT/RVDT input and simulator with two ADCs and two DACs per channel, each capable of sampling at a rate up to 330kHz. Once sampled, all readings from secondary windings of an LVDT/RVDT sensor are processed in the digital domain. The same applies to simulation – all processing occurs in the digital domain and the D/As convert a digital representation of the simulated signal into an analog waveform at the last stage of the processing.

3.1 Low-level Functions

Low-level LVDT/RVDT functions are described in detail in the API Reference Manual. The following table provides a summary of AI-254-specific functions:

Function	Description
DqAdv254SetMode	Sets up one of the 6 operating modes supported by the AI-254.
DqAdv254SetExcitation	Sets excitation frequency and amplitude in internal exitation mode.
DqAdv254GetWFMeasurements	Returns the measured parameters of a waveform on selected input(s).
DqAdv254MeasureWF	Simple form of DqAdv255GetWFMeasurements.
DqAdv254Enable	Enable/disable operations for channels specified in channel list.
DqAdv254GetExcitation	Gets board excitation voltage parameters of excitation waveform.
DqAdv254Read	Read the calculated position or special data for selected channels.
DqAdv254ReadVrms	Reads using DqAdv254Read, but returns calculated RMS voltage.
DqAdv254Write	Write a simulated position to simulate 4 and 5/6 wire LVDTs.
DqAdv254ConvertSim	Converts position to raw data representation for gain & phase control.
DqAdv254WriteBin	Writes a simulated position or special data for selected channels.
DqAdv254SetWForm	Sets up custom waveform for excitation channels P1/P2.

3.2 Modes of Operation

The AI-254 supported modes of operation are summarized in **Table 3-1** and explained in detail in Section 1.8.

To set the mode of a channel, use the low-level function, `DqAdv254SetMode()`.:

Mode	Description
Mode 0	Input with internal excitation for 5/6-wire LVDT/RVDT sensors
Mode 1	Input with internal excitation for 4-wire LVDT/RVDT sensors
Mode 2	Input with external excitation for 5/6-wire LVDT/RVDT sensors
Mode 3	Input with external excitation for 4-wire LVDT/RVDT sensors
Mode 4	Simulated output with external excitation for 5/6-wire LVDT/RVDT sensors
Mode 5	Simulated output with external excitation for 4-wire LVDT/RVDT sensors

Table 3-1 AI-254 Modes of Operation

3.3 Low-level Programming Techniques

Application developers are encouraged to explore the existing source code examples when first programming the AI-254. Sample code provided with the installation is self-documented and serves as a good starting point.

Code examples are located in the following directories:

- For Linux: <PowerDNA-x.y.z>/src/DAQLib_Samples
- For Windows: *Start » All Programs » UEI » PowerDNA » Examples*

3.3.1 Pre-defined Mode Variables

Pre-defined variables are referenced throughout the code examples and are available in the included header files, (i.e., powerdna.h).

Variables for the modes of operation are defined with the following mapping:

Mode	#define variable	Description
Mode 0	DQ_AI254_MODE_INT_5	Internal excitation of 5/6-wire LVDT
Mode 1	DQ_AI254_MODE_INT_4	Internal excitation of 4-wire LVDT
Mode 2	DQ_AI254_MODE_EXT_5	External excitation of 5/6-wire LVDT
Mode 3	DQ_AI254_MODE_EXT_4	External excitation of 4-wire LVDT
Mode 4	DQ_AI254_MODE_SIM_5	Simulated outputs of 5/6-wire LVDT
Mode 5	DQ_AI254_MODE_SIM_4	Simulated outputs of 4-wire LVDT

Table 3-2 Pre-defined Variables for Modes of Operation

3.3.2 Programming Examples

The following sections provide example code for each of the modes of operation.

3.3.2.1 Mode 0&1: Internal Excitation, 4/5/6 Wire LVDT/RVDT

Modes 0 and 1 configure an AI-254 channel as an input with internal excitation. In these modes, the AI-254 provides the required excitation voltage to an LVDT/RVDT sensor and reads back the output of secondary windings of the sensor.

Mode 0 and mode 1 generate an excitation signal internally to supply to a 5-/6-wire LVDT/RVDT sensor and 4-wire LVDT/RVDT sensor respectively.

The `DqAdv254SetExcitation()`function configures the internal excitation source on an AI-254 channel and returns a code for error checking.

The following is a code example for setting up internal excitation:

```
exc_rate = 2600.0;    // specifies excitation frequency
exc_level = 22.0;     // specifies excitation voltage (Vpp)
adc_rate = 0;         // returns actual sampling rate

ret = DqAdv254SetExcitation(
          hd0,              // handle to IOM from DqOpenIOM() function
          DEVN,             // board (device) ID #
          CHANNEL,          // channel to apply mode to (0 thru 3)
          DQ_AI254_ENABLE_EXC_A, // Enables P1± as output
          exc_rate,         // excitation frequency in Hz (100 thru 5k)
          exc_level,        // excitation level in Vpp
                            // (2Vrms (5.658Vpp) thru 6.7Vrms (18.953Vpp))
          &adc_rate);       // returns actual sampling rate

usr_offset = 0.0;           // additional offset (for in-system
                            // calibration, keep 0 if not needed)

usr_gain = 1.0;             // additional gain (for in-system
                            // calibration, keep 1.0 if not needed)

ret = DqAdv254SetMode(
          hd0,        // hd0 (handle to chassis)
          DEVN,       // board (device) ID #
          CHANNEL,    // channel to apply mode to
          mode,       // #define mode from Table 3-1
          flags,      // reserved, (set to 0)
          meas_points,// number of sampling points per period
          usr_offset, // see description above
          usr_gain,   // see description above
          exc_freq,   // Ignored for internal excitation modes
          exc_level); // Ignored for internal excitation modes
```

3.3.2.2 Mode 2&3: External excitation, 4/5/6 wire LVDT/RVDT

Modes 2 and 3 configure an AI-254 channel as an input with external excitation. In these modes, the AI-254 monitors excitation signals from an existing avionics interface. This mode is used when either external excitation is required to excite an LVDT/RVDT sensor (for example, when the required current exceeds the capabilities of the AI-254 board), or when an AI-254 is used in the role of a wiretapping device in parallel with the existing LVDT/RVDT input device.

The `DqAdv254MeasureWF()`function reads the external excitation source on an AI-254 channel and returns an the external excitation frequency, amplitude, and offset. However, the `DqAdv254MeasureWF()` is optional. If the external excitation rate, level, and offset are known by design and don't vary, those values can be hard-coded as inputs to the `DqAdv254SetMode()` function.

The following is a code example for setting up an AI-254 channel for external excitation:

```
ret = DqAdv254MeasureWF(
          hd0,        // handle to IOM from DqOpenIOM() function
          DEVN,       // board (device) ID #
          CHANNELandGAIN, // channel and gain,(GAIN<<8 | CHANNEL)
          &exc_rate,  // returns excitation frequency in Hz for
                      //   external excitation)
          &exc_level, // returns excitation level
          &exc_offset);// returns offset of the excitation signal

usr_offset = 0.0;           // additional offset (for in-system
                            // calibration, keep 0 if not needed)

usr_gain = 1.0;             // additional gain (for in-system
                            // calibration, keep 1.0 if not needed)


ret = DqAdv254SetMode(
          hd0,        // handle to IOM from DqOpenIOM() function
          DEVN,       // board (device) ID #
          CHANNEL,    // channel to apply mode to
          mode,       // #define mode from Table 3-1
          flags,      // reserved, (set to 0)
          meas_points,// number of sampling points per period
          usr_offset, // see description above
          usr_gain,   // see description above
          exc_freq,   // Mode 3, four-wire case: provides the expected
                      //  frequency to be received S2 input
                      // Mode 2, five/six-wire case: provides expected
                      //  excitation frequency for external excitation
          Se_level);  // Mode 3, four-wire case: defines constant, Se,
                      //  which is used to divide the input RMS voltage.
                      // Mode 2, five/six-wire case: provides expected
                      //  excitation level for external excitation
```

3.3.2.3 Mode 4&5: Simulation with external excitation, 4/5/6 wire LVDT/RVDT

Modes 4 and 5 configure an AI-254 channel as a simulated output with external excitation. In these modes, the AI-254 is connected directly into the avionics and simulates (or mimics) the LVDT/RVDT sensor. This mode is used when an external device expects to receive output from an LVDT/RVDT sensor in response to an applied excitation voltage. The AI-254 calculates parameters of the externally applied excitation and generates sinewaves on its outputs in accordance with the requested LVDT/RVDT position.

The `DqAdv254MeasureWF()`function reads the excitation source on an AI-254 channel and returns an the excitation frequency, amplitude, and offset. However, the `DqAdv254MeasureWF()` is optional. If the external excitation rate, level, and offset are known by design and don't vary, those values can be hard-coded as inputs to the `DqAdv254SetMode()` function.

The following is a code example for setting up an AI-254 channel for external excitation:

```
ret = DqAdv254MeasureWF(
          hd0,        // handle to IOM from DqOpenIOM() function
          DEVN,       // board (device) ID #
          CHANNELandGAIN, // channel and gain,(GAIN<<8 | CHANNEL)
          &exc_rate,  // returns excitation frequency in Hz for
                      //   external excitation -- modes 3, 4, and 5)
          &exc_level, // returns excitation level
          &exc_offset);// returns offset of the excitation signal


usr_offset = 0.0;           // additional offset (for in-system
                            // calibration, keep 0 if not needed)

usr_gain = 1.0;             // additional gain (for in-system
                            // calibration, keep 1.0 if not needed)


ret = DqAdv254SetMode(
          hd0,        // handle to IOM from DqOpenIOM() function
          DEVN,       // board (device) ID #
          CHANNEL,    // channel to apply mode to
          mode,       // #define mode from Table 3-1
          flags,      // reserved, (set to 0)
          meas_points,// number of sampling points per period
          usr_offset, // see description above
          usr_gain,   // see description above
          exc_freq,   // specifies the expected excitation frequency to
                      //  be received S1 inputs for simulation modes
          Se_level);  // specifies the initial levels of the simulated
                      //  output
```

3.3.3 Pin Mapping for Each Mode

The following table summarizes the required connections between an AI-254 board and an LVDT/RVDT sensor or avionics system for each mode:

Table 3-3. Wiring between AI-254 and an LVDT

Mode	4-wires		5/6-wires	
	AOut	**AIn**	**AOut**	**AIn**
Mode 0&1: Input, internal excitaion	P1± connected to the primary windings	S1± connected to Vout of the secondary windings	P1± connected to the primary windings	**6-wire**: S1± connected to Sa; S2± connected to Sb **5-wire**: S1+ connected to Sa; S2+ connected to Sb; S1- and S2- connected to common of secondary
Mode 2&3: Input, external excitation	N/C	S1± connected to Vout; S2± connected to external excitation	N/C	S1± connected to Sa, S2± connected to Sb
Mode 4&5: Simulator, external excitation	P1± connected to InA+ and InA- of the device	S1± connected to Exc+ and Exc- of the device	**6-wire**: P1± connected to InA+ and InA- of the device; P2± connected to InB+ and InB- of the device; **5-wire**: P1+ connected to InA+; P2+ connected to InB+; P1- and P2- not connected.	S1± connected to Exc+ and Exc- of the device

Appendix A

A.1 Accessories

The following cables and STP boards are available for the AI-254 board.

DNA-CBL-62

This is a 62-conductor round shielded cable with 62-pin male D-sub connectors on both ends. It is made with round, heavy-shielded cable; 2.5 ft (75 cm) long, weight of 9.49 ounces or 269 grams; up to 10ft (305cm) and 20ft (610cm).

DNA-STP-62

The STP-62 is a Screw Terminal Panel with three 20-position terminal blocks (JT1, JT2, and JT3) plus one 3-position terminal block (J2). The dimensions of the STP-62 board are 4w x 3.8d x1.2h inch or 10.2 x 9.7 x 3 cm (with standoffs). The weight of the STP-62 board is 3.89 ounces or 110 grams.

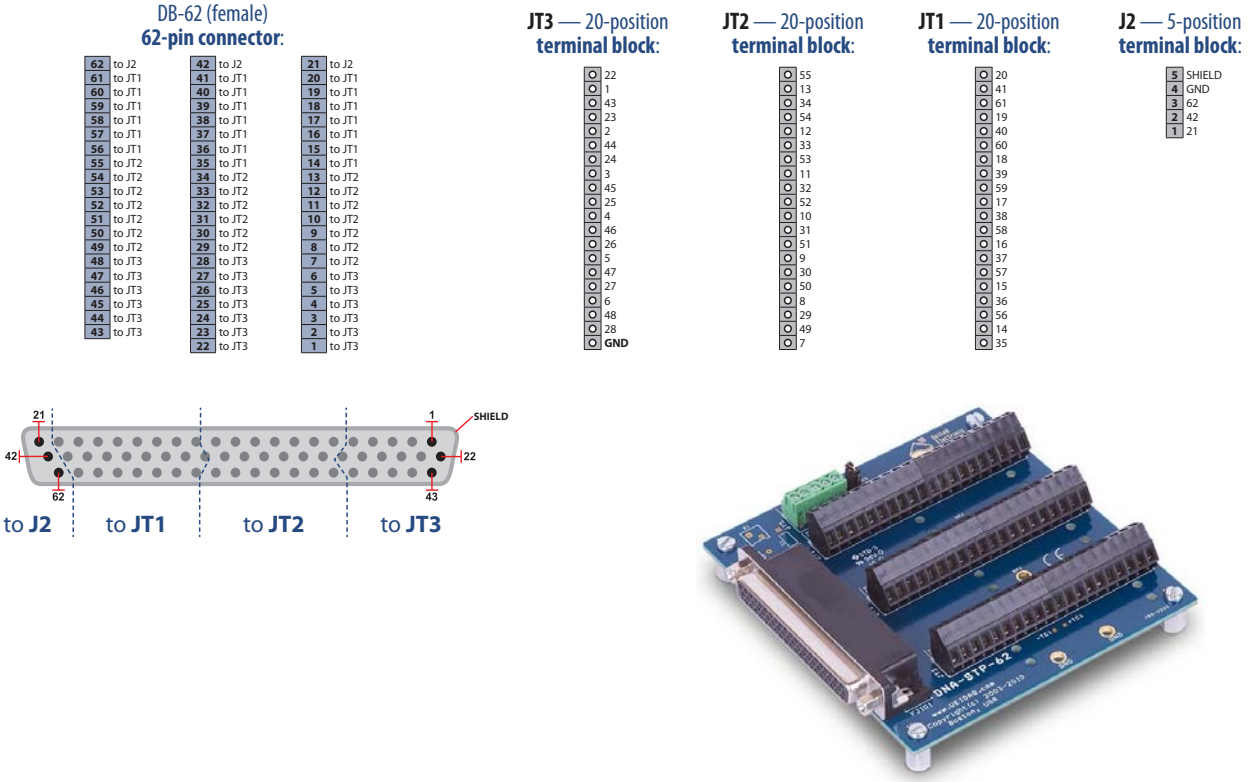


Figure A-1 Pinout and Photo of DNA-STP-62 Screw Terminal Panel

A.2 Step-up Transformer Signal Conditioners

DNA-TRF-254-122 and DNA-TRF-254-447

The DNA-TRF-254-122 and DNA-TRF-254-447 boards are step-up transformer signal conditioning extenders for the AI-254.

Figure A-2 Photo of DNA-TRF-254-122

The DNA-TRF-254-122 board provides a fixed step-up ratio of 1 to 1.22, extending the AI-254's 6.7 V_{rms} outputs to 8.1 V_{rms}.

The DNA-TRF-254-447 board provides a fixed step-up ratio of 1 to 4.47, extending the 6.7 V_{rms} outputs to 30 V_{rms}.

Note that maximum power for the board is 8.2 W. If simulated output voltages are stepped up by 1.22 or 4.47, the maximum drive current for those outputs must be reduced accordingly.

One side of the board provides a male 62-pin "D" connector that may be connected directly to the AI-254 or may be connected via cable. The other side of the board is a 62-pin female "D" connector which provides a pinout identical to the AI-254. Refer to **Figure A-3** for a block diagram of the extender board.

NOTE: When using transformer adapters while the AI-254 is in the 5-wire simulated output configuration, you will need to connect the P1- and P2- output of the transformer adapter to channel ground. This creates a single ended output from the transformer, which results in stepping up the voltage by 2 times the transformer ratio. This new step up ratio is due to the primary of the transformer being supplied by the differential output of P1+ and P1- and the output taken as single ended to ground.

For more information about the AI-254 board in 5-wire simulated output configuration, refer to Section 1.8.3.2 on page 16.

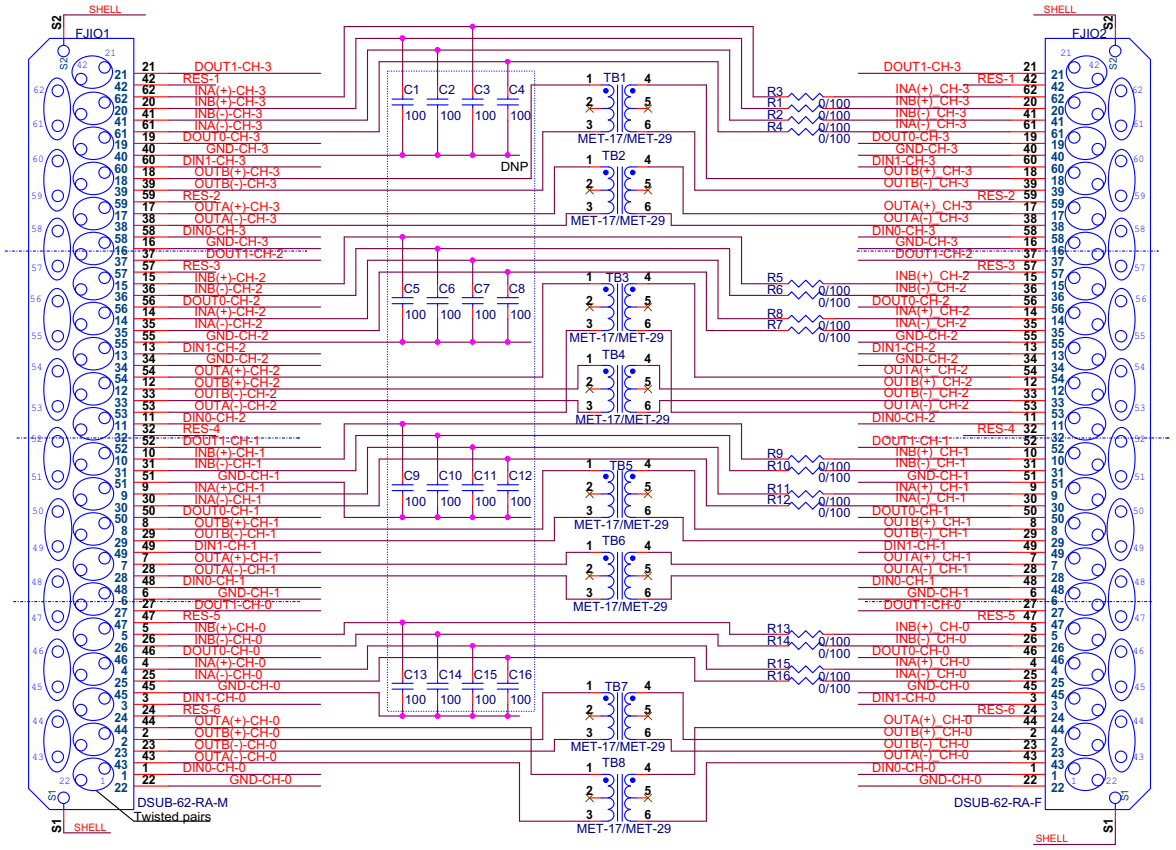


Figure A-3 DNA-TRF-254-447/122 Schematic/Block Diagram

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