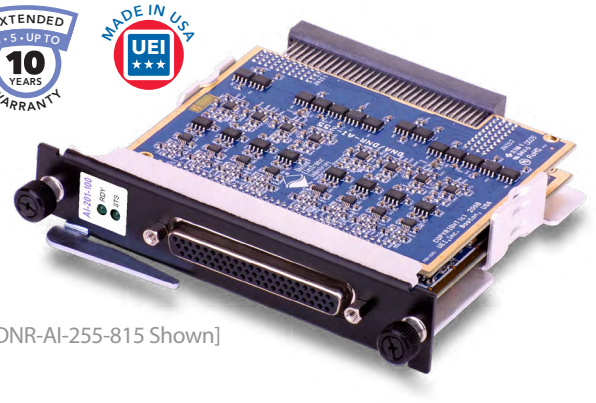
DNA/DNR-AI-255-815

2-Channel Synchro/Resolver Interface

- DNA-AI-255-815 for use with "Cube" I/O chassis
- DNR-AI-255-815 for use with RACKtangle™ I/O chassis
- 2 input / output channels
- 16-bit resolution
- 3-wire (Synchro) and 4-wire (Resolver) inputs
- Reference output per channel
- 5-115 Vrms inputs
- 50 Hz to 4000 Hz
- 2-28 Vrms output/reference at 1.2 VA without external buffer
- Fully Isolated (Chan to Chan and Chan to Cube)



[DNR-AI-255-815 Shown]

General Description

The DNA-AI-255-815 and DNR-AI-255-815 are two channel Synchro/Resolver input and output boards for UEI's powerful Cube and RACKtangle I/O chassis, respectively. The boards are suitable in a wide variety of test, measurement and control applications as well as providing simulated outputs for test and simulator applications. The board may be configured as two inputs, two or outputs, or one input and one output.

The board provides 2 input channels that will monitor either 3-wire synchros or 4-wire resolvers with inputs between 5 and 115 Vrms. For applications requiring a reference voltage greater than 28 Vrms, external excitation must be supplied. The board's high precision circuitry combined with each channel's independent 16-bit A/D converter allow measurement accuracies up to ± 2.6 arc-minute. The inputs may be read at rates up to the excitation frequency (4 kHz max).

Each channel provides its own programmable reference with outputs independently programmable from 2 to 28 Vrms at frequencies from 50 to 4,000 Hz and up to 1.2 VA. When using external references, the DNx-AI-255-815 automatically adjusts simulated outputs for variable amplitude and frequency references in one reference cycle.

The DNA/DNR-AI-255-815 also provides two channels of synchro or resolver output that are ideal for driving such items as attitude indicators or as a test source for a wide variety of synchro or resolver input devices. The outputs each accept an independent reference signal and offer 16-bit output resolution. Each channel will drive up to 28 Vrms at 1.2 VA without external buffering.

The board offers 350 Vrms of isolation between channels as well as between the I/O connections and the Cube or RACKtangle chassis. Like all PowerDNA/UEILogger I/O boards, the DNA-AI-255-815 offers operation in harsh environments and has been tested to 5g vibration, 50g shock, -40 to +85 °C temperatures and altitudes up to 70,000 feet in Cube based systems.

An easy to use yet powerful API is provided for applications written for Linux and most real-time operating systems including QNX, RTX, Intime, and VxWorks. Windows programmers may also use the the UEIDAQ Framework shich provides an even simpler API that supports all popular Windows programming languages. Finally, the Framework supplies complete support for those creating applications in LabVIEW, MATLAB/Simulink or any application supporting ActiveX or OPC servers.

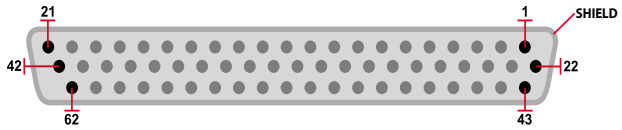
Technical Specifications:

Inputs	
Number of channels	2
Configuration	Synchro (3-wire) or Resolver (4-wire) may be selected via software
Resolution	16-bit
Accuracy	± 2.6 arc-minute
Frequency	50 Hz to 4.0 kHz
Signal Inputs	5-115 Vrms. (external reference required if operating at greater than 28 Vrms)
Acceleration	300 rps/s @ 60 Hz 450 rps/s @ 400 Hz 1000 rps/s @ 4000 Hz
Step response	800 mS - 179° @ 60 Hz 150 mS - 179° @ 2500 Hz
Update rate	Maximum update rate is equal to the excitation frequency.
Reference output	
Number of channels	2 (one per input channel)
Output voltage	28 Vrms up to 1.2 VA.
Voltage resolution	1.2 mVrms
Reference Frequency	50 Hz to 4 kHz (+/-1%)
Synchro / Resolver Outputs	
Number of channels	2 (total number of synchro/resolver inputs and simulated outputs is limited to 2.)
Configuration	Synchro (3-wire) or Resolver (4-wire)
Resolution	16-bit
Output Voltage	28 Vrms up to 1.2 VA.
Output Accuracy	±4 arc-minutes
General Specifications	
Operating temperature	Tested -40 °C to +85 °C (for operation above 60 °C in non GigE Cubes the DNA-FAN is required.)
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500 Hz, broad-band random
Shock *IEC 60068-2-27*	100 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations
Humidity	5 to 95%, non-condensing
Altitude	0 to 70,000 feet
MTBF	275,000 hours
Power consumption	4.5 Watt at idle, up to 10W at full load

Ordering Guide

Part Number	Description
DNA-AI-255-815	High Performance Dual channel synchro / resolver board for Cube I/O chassis
DNR-AI-255-815	High Performance Dual channel synchro / resolver board for RACKtangle I/O chassis
DNA-STP-62	62 conductor screw terminal panel
DNA-CBL-62	62 conductor shielded cable

Pinout Diagram:



	Pin	Signal	Pin	Signal	Pin	Signal
Chan 0	1	Rsvd	22	Gnd	43	Out A-
	2	Out B+	23	Out B-	44	Out A+
	3	Rsvd	24	n/c	45	Gnd
	4	In A+	25	In A-	46	Rsvd
	5	In B+	26	In B-	47	n/c
	6	Gnd	27	Rsvd	48	Rsvd
	7	Out C+	28	Out C-	49	Rsvd
	8	Out D+	29	Out D-	50	Rsvd
	9	In C+	30	In C-	51	Gnd
	10	In D+	31	In D-	52	Rsvd
Chan 1	11	Rsvd	32	n/c	53	Out A-
	12	Out B+	33	Out B-	54	Out A+
	13	Rsvd	34	Gnd	55	Gnd
	14	In A+	35	In A-	56	Rsvd
	15	In B+	36	In B-	57	n/c
	16	Gnd	37	Rsvd	58	Rsvd
	17	Out C+	38	Out C-	59	n/c
	18	Out D+	39	Out D-	60	Rsvd
	19	Rsvd	40	Gnd	61	In C-
	20	In D+	41	In D-	62	In C+
	21	Rsvd	42	n/c		

Dashed Line represents the isolation barrier between channels

Connection Notes:

The DNx-AI-255-815 may be used with Synchros or Resolvers, with internally provided excitation, or with external excitation, and may be used in input (to measure the output of a Synchro or Resolver) or simulated Synchro/Resolver output modes. The following connection guide depicts typical connections in each of the 8 ways the DNx-AI-255-815 is commonly utilized. The tables map each channels "In" and "Out" terminals as shown on the pinout diagram above to standard designations used in Synchro and Resolver applications.

Input Mode, Internally generated excitation

Inputs	Synchro	Resolver
In A+	S1	S1
In A-	C	S3
In B+	S3	S2
In B-	C	S4
In C+	S2	NC
In C-	C	NC
In D+	NC	NC
In D-	NC	NC

Outputs	Synchro	Resolver
Out A+	NC	NC
Out A-	NC	NC
Out B+	NC	NC
Out B-	NC	NC
Out C+	NC	NC
Out C-	NC	NC
Out D+	R1	R1
Out D-	R2	R3

Input Mode, External excitation

Inputs	Synchro	Resolver
In A+	S1	S1
In A-	C	S3
In B+	S3	S2
In B-	C	S4
In C+	S2	NC
In C-	C	NC
In D+	Exc+	Exc+
In D-	Exc-	Exc-

Outputs	Synchro	Resolver
Out A+	NC	NC
Out A-	NC	NC
Out B+	NC	NC
Out B-	NC	NC
Out C+	NC	NC
Out C-	NC	NC
Out D+	NC	NC
Out D-	NC	NC

Simulator Mode, Internal excitation

Inputs	Synchro	Resolver
In A+	NC	NC
In A-	NC	NC
In B+	NC	NC
In B-	NC	NC
In C+	NC	NC
In C-	NC	NC
In D+	NC	NC
In D-	NC	NC

Outputs	Synchro	Resolver
Out A+	S1	S1
Out A-	C	S3
Out B+	S3	S2
Out B-	C	S4
Out C+	S2	Opt+
Out C-	C	Opt-
Out D+	Exc+	Exc+
Out D-	Exc-	Exc-

SimulatorMode, External excitation

Inputs	Synchro	Resolver
In A+	NC	NC
In A-	NC	NC
In B+	NC	NC
In B-	NC	NC
In C+	NC	NC
In C-	NC	NC
In D+	Exc+	Exc+
In D-	Exc-	Exc-

Outputs	Synchro	Resolver
Out A+	S1	S1
Out A-	C	S3
Out B+	S3	S2
Out B-	C	S4
Out C+	S2	NC
Out C-	C	NC
Out D+	NC	NC
Out D-	NC	NC