United Electronic Industries

The High-Performance Alternative

DNx-CT-602-804

—

User Manual

Synchronous Serial Communication Interface Board with Differential Inputs/Outputs for the PowerDNA Cube and RACK Series Chassis

September 2017

PN Man-DNx-CT-602-804

CE

Contacting United Electronic Industries

Mailing Address:

27 Renmar Avenue
Walpole, MA 02081
U.S.A.

For a list of our distributors and partners in the US and around the world, please contact a member of our support team:

Support:

Telephone: (508) 921-4600
Fax: (508) 668-2350

Also see the FAQs and online “Live Help” feature on our web site.

Internet Support:

Support: support@ueidaq.com
Web-Site: www.ueidaq.com
FTP Site: ftp://ftp.ueidaq.com

Product Disclaimer:

WARNING!

DO NOT USE PRODUCTS SOLD BY UNITED ELECTRONIC INDUSTRIES, INC. AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

Products sold by United Electronic Industries, Inc. are not authorized for use as critical components in life support devices or systems. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness. Any attempt to purchase any United Electronic Industries, Inc. product for that purpose is null and void and United Electronic Industries Inc. accepts no liability whatsoever in contract, tort, or otherwise whether or not resulting from our or our employees' negligence or failure to detect an improper purchase.

Specifications in this document are subject to change without notice. Check with UEI for current status.

Table of Contents

List of Figures

Chapter 1 Introduction

This document outlines the feature set and use of the DNx-CT-602-804 interface board for synchronous serial-line communication applications.

The following sections are provided in this chapter:

- Organization of this Manual (Section 1.1)
- CT-602-804 Board Overview (Section 1.2)
- Features (Section 1.3)
- Specification (Section 1.4)
- Indicators (Section 1.5)
- Device Architecture (Section 1.6)
- Device Description (Section 1.7)
- Wiring & Connectors (pinout) (Section 1.8)

1.1 Organization of this Manual

This CT-602-804 User Manual is organized as follows:

- **Introduction**
  Chapter 1 provides an overview of DNx-CT-602-804 features, device architecture, connectivity, and logic.
- **Programming with the High-Level API**
  The CT-602-804 is not currently supported in the high-level API. (Chapter 2 customarily provides an overview of the how to create a session, configure the session, and interpret results with the high-level framework API).
- **Programming with the Low-Level API**
  Chapter 3 is an overview of low-level API commands for configuring and using the CT-602-804 series board.
- **Appendix A - Accessories**
  This appendix provides a list of accessories available for use with the DNx-CT-602-804 board.
- **Index**
  The index provides an alphabetical listing of the topics covered in this manual.

NOTE: A glossary of terms used with the PowerDNA Cube/RACK and I/O boards can be viewed or downloaded from www.ueidaq.com.

Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:

Tips are designed to highlight quick ways to get the job done or to reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.

CAUTION! *Caution advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

Text formatted in **bold** typeface generally represents text that should be entered verbatim. For instance, it can represent a command, as in the following example: “You can instruct users how to run setup using a command such as **setup.exe**.”

Bold typeface will also represent field or button names, as in “Click **Scan Network**.”

Text formatted in `fixed` typeface generally represents source code or other text that should be entered verbatim into the source code, initialization, or other file.

Examples of Manual Conventions

Before plugging any I/O connector into the Cube or RACKtangle, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

Usage of Terms

Throughout this manual, the term “Cube” refers to either a PowerDNA Cube product or to a PowerDNR RACKtangle™ rack mounted system, whichever is applicable. The term DNR is a specific reference to the RACKtangle, DNA to the PowerDNA I/O Cube, and DNx to refer to both.

1.2 CT-602-804 Board Overview

The DNx-CT-602-804 boards are high performance synchronous serial communication boards.

DNA-CT-602-804, DNR-CT-602-804, and DNF-CT-602-804 boards are compatible with the Cube, RACKtangle, and FLATRACK chassis respectively. These board versions are electronically identical and differ only in mounting hardware. The DNA version is designed to stack in a Cube chassis. The DNR/F versions are designed to plug into the backplane of a RACK chassis.

CT-602-804 boards provide four independent channels, each having overvoltage protection and opto-isolation.

The CT-602-804 channels can be configured independently as four RX or TX synchronous serial channels. Alternatively, an even channel can be configured as an RX or TX synchronous serial channel in an extended pin functionality mode, where odd channel pins are repurposed into additional trigger input, ACK input, and/or clock input/output pins.

1.2.1 Synchronous Serial Mode

The CT-602-804 supports general purpose synchronous serial (GPSS) communication and “Clock/Data/Strobe” legacy synchronous protocols.

1.2.2 Data Rates

Supported data rates are between 300 bps to 16 Mbps, with a maximum sustained rate for the board at 2 MB/sec and 4 MB/sec aggregate for all boards in a single Cube or RACK chassis.

The clock source can be generated internally (with 0.1% or better accuracy) or provided externally 1 TX/RX bit per clock.

1.2.3 Data Word Length

Supported data word lengths are programmable from 3 to 32 bits.

1.2.4 FIFO Storage

TX and RX data storage is provided via two 1024 word x 32 bit FIFOs, with a user-programmable TX and RX watermark allowing synchronous event/interrupt generated upon FIFO full.

1.2.5 Software Support

Software included with the DNx-CT-602-804 provides a comprehensive yet easy to use API that supports all popular operating systems including Windows, Linux, real-time operating systems such as QNX, RTX, VxWorks and more.

1.3 Features

A summary of features of the CT-602-804 general purpose synchronous serial communication is provided below:

- Up to 4 independent simplex serial channels. (In some modes, a channel is dedicated to generating the baud rate clock)
- Electrical specifications: RS-485/422 complaint. Fully differential I/O using at RS-422 / RS-485 logic voltage levels
- Data rates: 300 bps - 16 Mbps (maximum sustained rate for the board is 2MB/sec, 4MB/sec aggregate for all boards in a single DNx chassis)
- Data word length: 3-32 bits
- Clock source: internal (with 0.1% or better accuracy), or external (1 TX/RX bit per clock)
- FIFO 1024x32 for TX and RX with watermark. Asynchronous event/interrupt generated upon FIFO full
- Programmable FrameSync length (1 bit / N bits / Word / Frame)
- Programmable DataIn/DataOut encoding (NRZ / NRZI), formatting (signal may be pre-/post- inverted)
- Trigger output for every TX channel
- Start/pause/stop all channels simultaneously
- 32-bit prescaler per channel
- Works with either internal (66 MHz) or external (max 16.5 MHz) timebases;
- Debouncing/glitch removal on external clock and data inputs
- Protection 7 kV ESD, 350V isolation
- Power consumption 2W

1.4 Specification

Technical specifications for the DNx-CT-602-804 board are listed in **Table 1-1**.

Table 1-1 DNx-CT-602-804 Technical Specifications

SYNCHRONOUS SERIAL Ports	
Baud Rate	300 to 16 Megabaud (2 Mb sustained, 4 Mb max per DNA/DNR chassis
Baud Rates available	User selectable 0.1% accuracy or better
Data Word Length	3 - 32 bits
FIFO (on each channel)	Input: 1024 word, Output: 1024 word
FrameSync phase control	Programmable in 15.15 nS increments
GENERAL SPECIFICATIONS	
Protection	7 kV ESD, 350V isolation
Input High / Low voltage	RS-422/485 compatible
Electrical Isolation	350 Vrms, chan-chan and chan-chassis
Output High / Low voltage	RS-422/485 compatible
Input/output buffer chip	LTC1686 or equivalent
Power consumption	2W
Operating range	Tested -40 to +85 °C
Humidity range	0 - 95%, noncondensing
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500 Hz, broad-band random
Shock *IEC 60068-2-27*	50 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations

1.5 Indicators

The DNx-CT-602-804 indicators are described in **Table 1-2** and illustrated in **Figure 1-1**.

Table 1-2 CT-602-804 Indicators

LED Name	Description
RDY	Indicates board is powered up and operational
STS	Indicates which mode the board is running in: • **OFF**: Configuration mode, (e.g., configuring channels, running in point-by-point mode) • **ON**: Operation mode

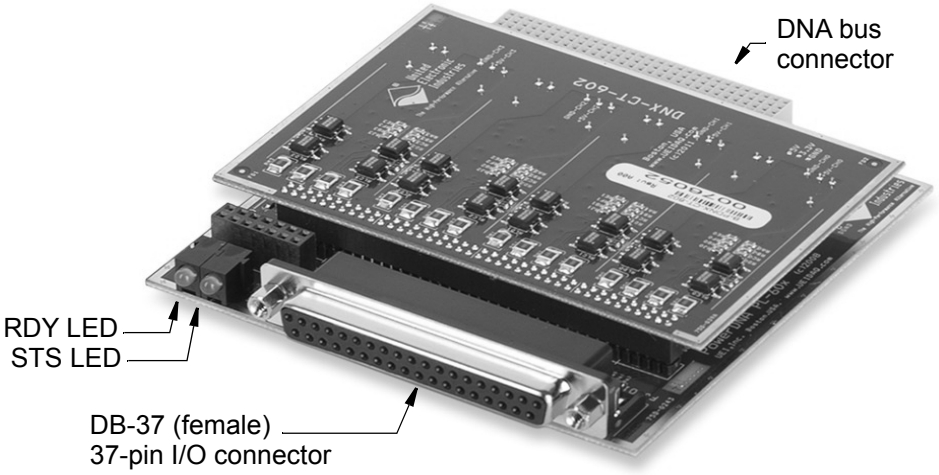


Figure 1-1 Photo of DNA-CT-602-804 Synchronous Serial Board

1.6 Device Architecture

The CT-602-804 board is based on the CT-602 board, where FPGA circuitry is repurposed for general purpose synchronous serial (GPSS) application support. All inputs and outputs are optically isolated and overvoltage protected.

Figure 1-2 provides a block diagram of the CT-602-804. Refer to Section 1.8 for pin mappings with respect to channel configuration.

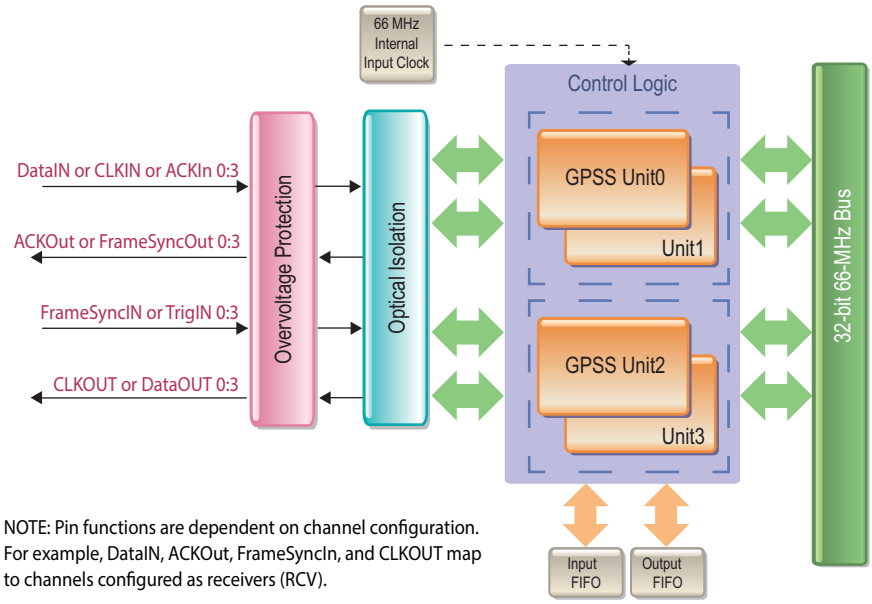


Figure 1-2 Block Diagram of CT-602-804

1.7 Device Description

The CT-602-804 is a highly configurable synchronous serial communication interface that supports point-to-point serial connections.

1.7.1 Transmit Description

When transmitting in the default condition, the CT-602-804 receives a continuous differential clock signal at the programmed baud rate.

The FrameSync signal is output from the transmitter, indicating a data frame is transmitting. The data frame consists of a user-programmed number of words, with each word consisting of a user-programmed number of bits.

Data is shifted out as most significant bit (MSB) first, synchronized with the clock pulse train from the receiver (or other controller). No particular start or stop sequence is required (no start bit or stop bit).

Refer to **Figure 1-3**.

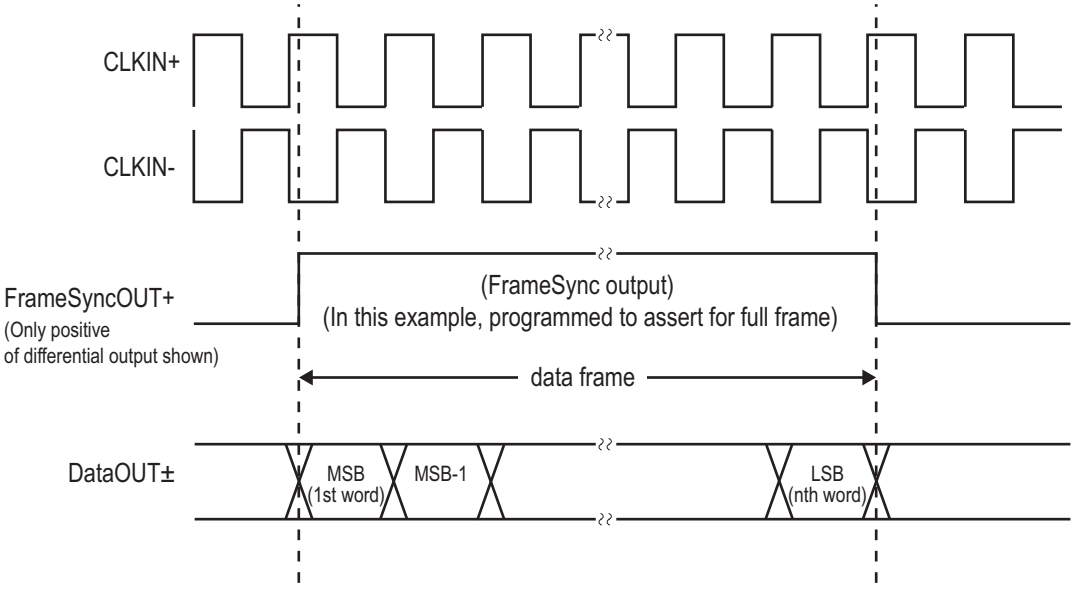


Figure 1-3 Transmit Waveform Example

1.7.2 Receive Description

By default, a CT-602-804 that is programmed as a receiver generates an output clock (CLKOUT) at the user-specified baud rate.

The receiver inputs a FrameSync signal, which indicates a data frame is being received.

Data is shifted in as most significant bit (MSB) first, with no particular start or stop sequence required (no start bit or stop bit). The data frame consists of a user-programmed number of words, with each word consisting of a user-programmed number of bits.

If enabled, a differential acknowledge (ACKOUT±) is asserted when the full frame is received. Refer to **Figure 1-4**.

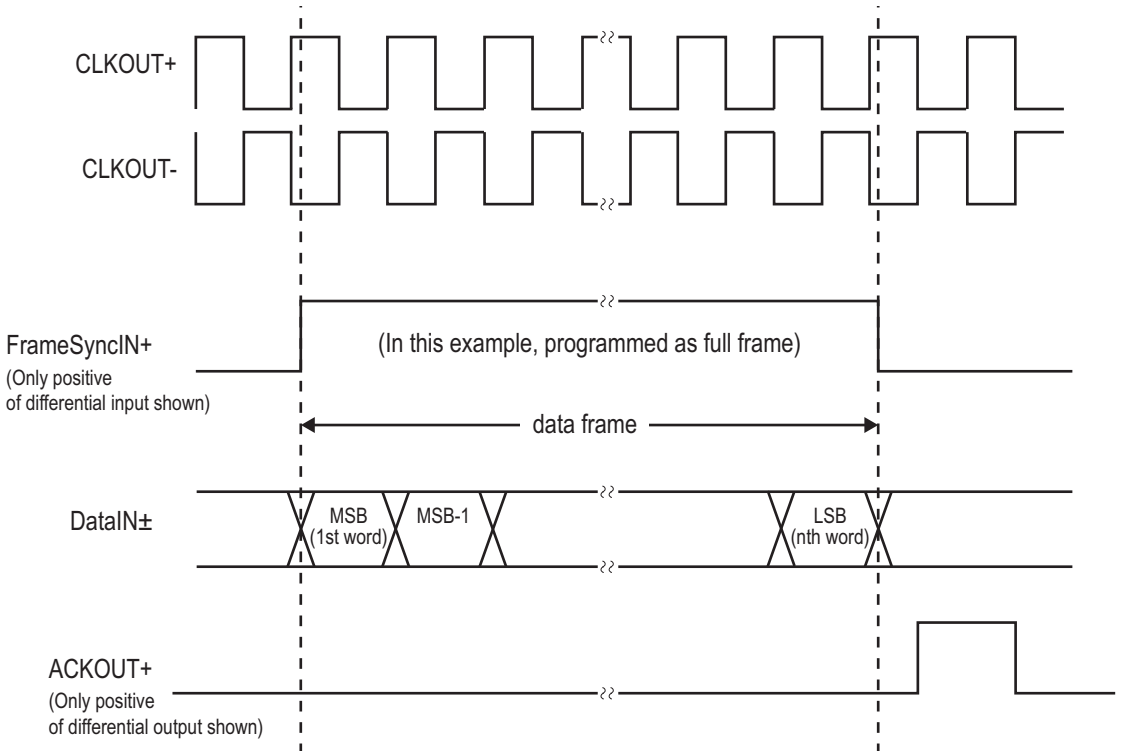


Figure 1-4 Receive Waveform Example

1.7.3 Serial Port Configuration Options

Polarity of I/O signals. In the examples shown in **Figure 1-3** and **Figure 1-4**, the polarity of the CLK, FrameSync, and Data signals is programmed to be positive (POS). If the polarity was programmed as NEG, the + and - waveforms would be swapped on the corresponding differential pins.

External Frame Sync I/O pin configuration. In the above examples, the FrameSync strobe is programmed to assert for the full frame. Alternatively it could be programmed to assert for a single bit, or a user-specified number of bits, and/or programmed to assert once per data frame or on every word in a data frame. It could also be programmed to assert for a full word-length for a user-specified number of words.

Data frame length. The data frame length is the number of transmit words that will be shifted out in a data frame (or number of receive words shifted in with each frame for receivers). The number of TX/RX words in a data frame is user programmable.

Data word length. The number of bits in the data word can be customized by the user. Supported word lengths are 3 bits (MSB, MSB-1, LSB) to 32 bits.

Data encoding. Transmit data encoding is user-programmable. NRZ or NRZi encoding are supported (as well as positive and negative).

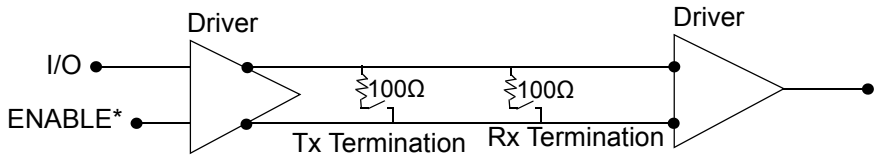
Trigger modes, clock out, and input acknowledge pins can also be programmed by the user for channels configured as transmitters. Trigger modes and clock in pins can be set up for channels configured as receivers.

Refer to **Chapter 3** for more information about programming the CT-602-804.

1.7.4 Termination

The CT-602-804 features termination resistors on both the receiver and transmitter lines to provide a driver load impedance of 100 Ω.

Refer to **Figure 1-5**.



* Note: Only used channels are enabled. Unused channels are automatically disabled by the firmware.

Figure 1-5 Settable Termination Circuit Diagram

Each of these lines can be set through software in the low-level API. Refer to **Chapter 3** for more information.

1.7.5 Electrical Specification for Serial Port Lines

The CT-602-804 is compliant with RS-422 and RS-485 standards for electrical characteristics of drivers and receivers used in serial communication.

Refer to TIA/EIA-422 and TIA/EIA-485 Standards documentation for more information.

1.8 Wiring & Connectors (pinout)

Figure 1-6 below illustrates the pinout of the CT-602-804. The OUT_ and IN_ pins are described in **Table 1-3** by RX/TX channel configuration.

Each of the four channels on the CT-602-804 can be configured as a transmit serial channel or as a receive serial channel. Additionally, channel 0 or channel 2 can be configured to use additional pins remapped from channel 1 and channel 3, respectively, for extended functionality.

The CT-602-804 board uses a 37-pin D-sub connector.

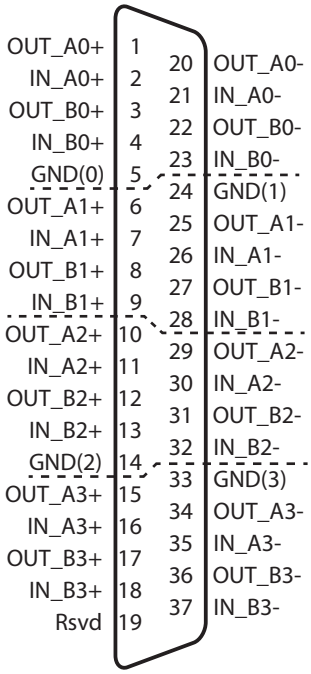


Figure 1-6 Pinout Diagram of the CT-602-804 Board

All signals are referenced relative to isolated ground (iGND).

Pin No.	Pinout Name	Pin Function in Normal Mode		Ch0/1 & Ch2/3 with Added Pin Enable	
		Channel as XMT	Channel as RCV	Channel as XMT	Channel as RCV
1	OUT_A0+	Ch0 SER DataOUT+	Ch0 SER CLKOUT+	Ch0 SER DataOUT+	Ch0 SER CLKOUT+
20	OUT_A0-	Ch0 SER DataOUT-	Ch0 SER CLKOUT-	Ch0 SER DataOUT-	Ch0 SER CLKOUT-
2	IN_A0+	Ch0 EXT TrigIN+	Ch0 FrameSyncIN+	Ch0 EXT TrigIN+	Ch0 FrameSyncIN+
21	IN_A0-	Ch0 EXT TrigIN-	Ch0 FrameSyncIN-	Ch0 EXT TrigIN-	Ch0 FrameSyncIN-
3	OUT_B0+	Ch0 FrameSyncOUT+	Ch0 ACKOUT+	Ch0 FrameSyncOUT+	Ch0 ACKOUT+
22	OUT_B0-	Ch0 FrameSyncOUT-	Ch0 ACKOUT-	Ch0 FrameSyncOUT-	Ch0 ACKOUT-
4	IN_B0+	Ch0 SER CLKIN+	Ch0 SER DataIN+	Ch0 SER CLKIN+	Ch0 SER DataIN+

Table 1-3 Channel Pin Mapping per Configuration for the CT-602-804 Board

Pin No.	Pinout Name	Pin Function in Normal Mode		Ch0/1 & Ch2/3 with Added Pin Enable	
		Channel as XMT	Channel as RCV	Channel as XMT	Channel as RCV
23	IN_B0-	Ch0 SER CLKIN-	Ch0 SER DataIN-	Ch0 SER CLKIN-	Ch0 SER DataIN-
6	OUT_A1+	Ch1 SER DataOUT+	Ch1 SER CLKOUT+	Ch0 SER CLKOUT+	not used
25	OUT_A1-	Ch1 SER DataOUT-	Ch1 SER CLKOUT-	Ch0 SER CLKOUT-	not used
7	IN_A1+	Ch1 EXT TrigIN+	Ch1 FrameSyncIN+	not used	Ch0 EXT TrigIN+
26	IN_A1-	Ch1 EXT TrigIN-	Ch1 FrameSyncIN-	not used	Ch0 EXT TrigIN-
8	OUT_B1+	Ch1 FrameSyncOUT+	Ch1 ACKOUT+	not used	not used
27	OUT_B1-	Ch1 FrameSyncOUT-	Ch1 ACKOUT-	not used	not used
9	IN_B1+	Ch1 SER CLKIN+	Ch1 SER DataIN+	Ch0 ACKIN+	Ch0 SER CLKIN+
28	IN_B1-	Ch1 SER CLKIN-	Ch1 SER DataIN-	Ch0 ACKIN-	Ch0 SER CLKIN-
10	OUT_A2+	Ch2 SER DataOUT+	Ch2 SER CLKOUT+	Ch2 SER DataOUT+	Ch2 SER CLKOUT+
29	OUT_A2-	Ch2 SER DataOUT-	Ch2 SER CLKOUT-	Ch2 SER DataOUT-	Ch2 SER CLKOUT-
11	IN_A2+	Ch2 EXT TrigIN+	Ch2 FrameSyncIN+	Ch2 EXT TrigIN+	Ch2 FrameSyncIN+
30	IN_A2-	Ch2 EXT TrigIN-	Ch2 FrameSyncIN-	Ch2 EXT TrigIN-	Ch2 FrameSyncIN-
12	OUT_B2+	Ch2 FrameSyncOUT+	Ch2 ACKOUT+	Ch2 FrameSyncOUT+	Ch2 ACKOUT+
31	OUT_B2-	Ch2 FrameSyncOUT-	Ch2 ACKOUT-	Ch2 FrameSyncOUT-	Ch2 ACKOUT-
13	IN_B2+	Ch2 SER CLKIN+	Ch2 SER DataIN+	Ch2 SER CLKIN+	Ch2 SER DataIN+
32	IN_B2-	Ch2 SER CLKIN-	Ch2 SER DataIN-	Ch2 SER CLKIN-	Ch2 SER DataIN-
15	OUT_A3+	Ch3 SER DataOUT+	Ch3 SER CLKOUT+	Ch2 SER CLKOUT+	not used
34	OUT_A3-	Ch3 SER DataOUT-	Ch3 SER CLKOUT-	Ch2 SER CLKOUT-	not used
16	IN_A3+	Ch3 EXT TrigIN+	Ch3 FrameSyncIN+	not used	Ch2 EXT TrigIN+
35	IN_A3-	Ch3 EXT TrigIN-	Ch3 FrameSyncIN-	not used	Ch2 EXT TrigIN-
17	OUT_B3+	Ch3 FrameSyncOUT+	Ch3 ACKOUT+	not used	not used
36	OUT_B3-	Ch3 FrameSyncOUT-	Ch3 ACKOUT-	not used	not used
18	IN_B3+	Ch3 SER CLKIN+	Ch3 SER DataIN+	Ch2 ACKIN+	Ch2 SER CLKIN+
37	IN_B3-	Ch3 SER CLKIN-	Ch3 SER DataIN-	Ch2 ACKIN-	Ch2 SER CLKIN-

Table 1-3 Channel Pin Mapping per Configuration for the CT-602-804 Board (Cont.)

Pin descriptions for XMT / RCV functionality:

- Pin Usage for Transmission:
  - SER CLKIN - serial input SyncClock from UUT. Transmission clock can also be derived internally from the PLL with post-divide on prescaler
  - SER DataOUT - serial data transmitted out of the channel
  - EXT TrigIN - external input trigger: transmission can be triggered either by the software or by this line; edge or level is software selectable
  - FrameSync OUT - frame/sync strobe: produces FrameSync when external baud clock is applied to ClkIn or SyncClock when baud rate is derived internally
  - ACK (optional) - Acknowledge
- Pin Usage for Reception:
  - SER CLKOUT - serial clock out: output baud clock generated for UUT transmissions
  - SER DataIN - serial input data received from UUT
  - FrameSyncIN - input FrameSync strobe from UUT

NOTE: If you are using a accessory panel with the CT-602-804, please refer to the Appendix for a description of the panel.

Chapter 2 Programming with the High-Level API

UeiDaq Framework library is object oriented and its objects can be manipulated in the same manner from different development environments, such as Visual C++, Visual Basic, or LabVIEW.

The DNx-CT-602-804 is not currently supported in the high-level framework.

For more information about programming the CT-602-804, please review **Chapter 3**, Programming with the Low-Level API.

Chapter 3 Programming with the Low-Level API

This chapter provides the following information about programming the CT-602-804 using the low-level API:

- About the Low-level API (Section 3.1)
- Low-level Functions (Section 3.2)
- Low-level Programming Techniques (Section 3.3)

3.1 About the Low-level API

The low-level API provides direct access to the DAQBIOS protocol structure and registers in C. The low-level API is intended for speed-optimization, when programming unconventional functionality, or when programming under Linux or real-time operating systems.

For additional information regarding low-level programming, refer to the “PowerDNA API Reference Manual” located in the following directories:

- On Linux systems:
  <PowerDNA-x.y.z>/docs
- On Windows systems:
  Start » All Programs » UEI » PowerDNA » Documentation

3.2 Low-level Functions

Table 3-1 provides a summary of CT-602-804-specific functions. In addition to CT-602-804-specific functions, in the CT-602-804 can supports CT-601- and CT-602-specific functions. All low-level functions are described in detail in the PowerDNA API Reference Manual.

Table 3-1 Summary of Low-level API Functions for DNx-CT-602-804

Function	Description
`DqAdv602SetGPSSConfig`	Configures general purpose synchronous serial channels: sets channel as RCV/XMT; sets baud rate; sets word length; configures encoding of data; configures clock, data, framesync
`DqAdv602SetTermination`	Configures onboard termination on transmit / receive lines
`DqAdv601Enable`	Enables or disables serial channels on the board
`DqAdv602SendGPSSMessage`	Writes a block of data to a synchronous serial port
`DqAdv602RecvGPSSMessage`	Reads a block of data from a synchronous serial port

3.3 Low-level Programming Techniques

Application developers are encouraged to explore the existing source code examples when first programming the CT-602-804. Sample code provided with the installation is self-documented and serves as a good starting point.

Code examples are located in the following directories:

- On Linux systems: <PowerDNA-x.y.z>/src/DAQLib_Samples
- On Windows: *Start » All Programs » UEI » PowerDNA » Examples*

Code examples specifically for the CT-602-804 have GPSS specified in the name, (i.e., `Sample602GPSS.c`).

3.3.1 Configuring Serial Interface

CT-602-804 is a highly flexible synchronous serial communication board. Each channel can be configured as a transmitter or receiver, and I/O signals can additionally have polarity, encoding, debouncing and more customized.

The CT-602-804 is configured using the `DqAdv602SetGPSSConfig()`API:

```
DqAdv602SetGPSSConfig(
      int hd,           // Handle to IOM received from DqOpenIOM()
      int devn,         // Board device # inside the IOM chassis
      int chan,         // Channel to be configured
      pCT602_GPSS_CFG config);// Structure to hold config settings
```

The `pCT602_GPSS_CFG` structure consists of the following elements:

```
// GPSS channel configuration
typedef struct {
    uint32 mode;      // TX or RX
       uint32 flags;  // mode modification flags, like Rx timestamp
        uint32 baud;        // baud rate
        uint32 word_len;    // data word length in bits, 1=variable
        uint32 frame_len;   // length of the frame in entries,
                            // (i.e., # of data words in frame)
        uint32 en_clock1;   // enable clock on channel+1
        uint32 en_ack1;     // enable acknowledge on channel+1
        uint32 dbc_fs;      // FrameSync debouncer value
                            // (0 == disabled)
        uint32 dbc_data;    // Data debouncer value
                            // (0 == disabled)
        uint32 clk_edge;    // clock edge, positive or negative
        uint32 data_mode;   // data encoding and polarity
        uint32 trig_mode;   // trigger mode and polarity
        uint32 fs_mode;     // FrameSync type and polarity
        uint32 fs_len;      // length of FrameSync signal
        uint32 frame_clk;   // frame clock in Hz (0 == disabled)
        uint32 wordlen_prg; // <reserved>
        int wordlen_shift;  // <reserved>

    } CT602_GPSS_CFG, *pCT602_GPSS_CFG;
```

Table 3-2 lists configuration options for each element.

Table 3-2 CT-602-804 Configuration Options

Configuration Parameter	Options
mode	#define CT602_MODE_RX: channel is receiver (RX) #define CT602_MODE_TX: channel is transmitter (TX)
flags	#define CT602_FLAG_TSTAMP: add timestamp to the received data by the end of the frame
baud	uint32 300 baud to 16 Megabaud (2 Mb sustained, 4 Mb max per chassis)
word_len	#define CT602_WORD_LEN(N): 3 to 32 bits in the word
frame_len	Number of words in frame
en_clock1	#define CT602_CLK1_EN: enable clock out (Tx) or external clock in (Rx) on channel+1
en_ack1	#define CT602_ACK1_POS: acknowledge is positive #define CT602_ACK1_NEG: acknowledge is negative #define CT602_ACK1_EN: enable ack out (Rx) or ack in (Tx) on channel+1
dbc_fs	#define CT602_DBC_FS(N): enable (if >0) debouncer on FrameSync strobe
dbc_data	#define CT602_DBC_DATA(N): enable (if >0) debouncer on data
clk_edge	#define CT602_CLK_EDGE_NEG: negative edge clocks in data (falling) #define CT602_CLK_EDGE_POS: positive edge clocks in data (rising)
trig_mode	#define CT602_TRIG_POS: trigger is positive #define CT602_TRIG_NEG: trigger is negative #define CT602_TRIG_LEVEL: trigger is level sensitive #define CT602_TRIG_EDGE: trigger is edge-sensitive #define CT602_TRIG_INTERNAL: trigger is internal #define CT602_TRIG_EXTERNAL: trigger is external #define CT602_TRIG_ONE_WORD: TX, one word per trigger; RX, one frame per trigger #define CT602_TRIG_IN_FIFO: output FIFO per trigger #define CT602_TRIG_NOTRIG: trigger is always enabled #define CT602_TRIG_ASSERTED: TX/RX, until trigger active (level only, full words transmitted) #define CT602_TRIG_FFE: TX, one frame per trigger or FIFO empty (parameters can be logically ORed together)

Table 3-2 CT-602-804 Configuration Options

Configuration Parameter	Options
fs_mode	#define CT602_FS_POS: FrameSync strobe is positive #define CT602_FS_NEG: FrameSync strobe is negative #define CT602_FS_EVERYWORD: every word output assigned a FrameSync strobe #define CT602_FS_BITS: FrameSync strobe length is in bits #define CT602_FS_WORDS: FrameSync strobe is in words #define CT602_FS_FRAME: FrameSync strobe is asserted for the whole frame
fs_len	Number of bits/words FrameSync strobe is asserted for (bits or words is set per fs_mode programming)

Appendix

A.1 Accessories

The following cables and STP boards are available for the CT-602-804 board.

DNA-CBL-37

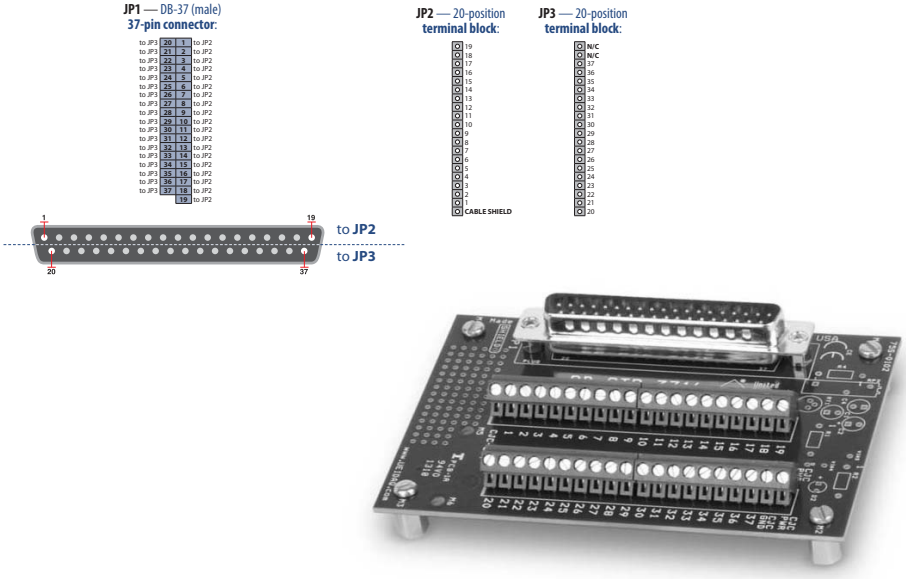
3ft, 37-way flat ribbon cable; connects CT-602-804 to panels to DNA-STP-37.

DNA-CBL-37S

3ft, 37-way shielded cable; connects CT-602-804 to panels to DNA-STP-37.

DNA-STP-37

37-way screw terminal panel.



DNA-STP-37D

37-way direct-connect screw terminal panel.

Index