United Electronic Industries

The High-Performance Alternative

DNA/DNR-CT-651 Precision Timing Interface Board

—

User Manual

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Note: Specifications shown in this document are subject to change without notice. Please check with UEI for current status.

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Chapter 1 Introduction

This document outlines the feature-set and operation of the UEI DNA- and DNR-CT-651 Precision Timing Interface boards for use with UEI's Cube and RACKtangle data acquisition systems.

1.1 Organization of this manual

This DNA-CT-651 User Manual is organized as follows:

- **Chapter 1- Introduction**
  This section provides an overview of the document content, device architecture, functional description, connectivity, and logic of the board.
- **Chapter 2 – Programming with the High Level API**
  This section explains how to program the CT-651 using the UEIDaq Framework High Level API.
- **Chapter 3 – Programming with the Low Level API**
  This section describes how to program the CT-651 using the Low Level API.
- **Appendix – A. Accessories**
  This appendix contains a list of associated equipment typically used with the unit.
- **Index**
  This is an alphabetical listing of topics covered in this manual.

Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:

Tips are designed to highlight quick ways to get the job done, or reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.

CAUTION! Caution advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.

Text formatted in bold typeface generally represents text that should be entered verbatim. For instance, it can represent a command, as in the following example: "You can instruct users how to run setup using a command such as setup.exe."

Frequently Asked Questions

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1.2 DNx-CT-651 Precision Timing Interface Board Features

The DNx-CT-651 Precision Timing Interface board s have the following features:

- Provides 4 independent channels of synchronous 1 PPS timing signals
- 7 Operating Modes
  — Input Follower.
  — Input Follower w/ user-set pulse width.
  — Auto-follower
  — Auto- Follower w/ user-set pulse width.
  — Free-run/Flywheel oscillator
  — Sync_x Pass-through
  — Disabled (OFF)
- Fully software configurable
- Standard ICD-GPS-060 output levels
- Uses standard coaxial connectors
- High accuracy / high stability on-board oscillator
- UEI 10-year Availability Guarantee

1.3 Photos

DNA-CT-651

DNR-CT-651

Figure 1-1. DNA-and DNR-CT-651 Precision Timing Interface Boards

1.4 DNx-CT-651

The purpose of the DNx-CT-651 is to provide an industry-standard precision timing interface for use with UEI Cube and RACKtangle Ethernet-based DAQ systems to provide a wide variety of synchronization, timing reference, and system heartbeat signals.

Each of four output channels may be set independently by software commands from the host over the Ethernet port on the Cube or RACKtangle chassis to any of the following configurations:

- Slaved to the 1 PPS external input signal in “follower” modes
- Same as above with user-set pulse width
- Slaved to the 1 PPS external input signal in “auto-follower” mode (switches to flywheel oscillator if input pulse is invalid)
- Same as above with user-set pulse width

- Free running (flywheel) 1 PPS output signal based on the on-board reference oscillator
- Sync-x Pass-through of DNA Bus Signals to outputs
- Disabled (OFF)

Two green LEDs are mounted on the front of the boards to indicate Power ON, and Logic Active.

A functional block diagram of the CT-651 is illustrated in **Figure 1-2** below.

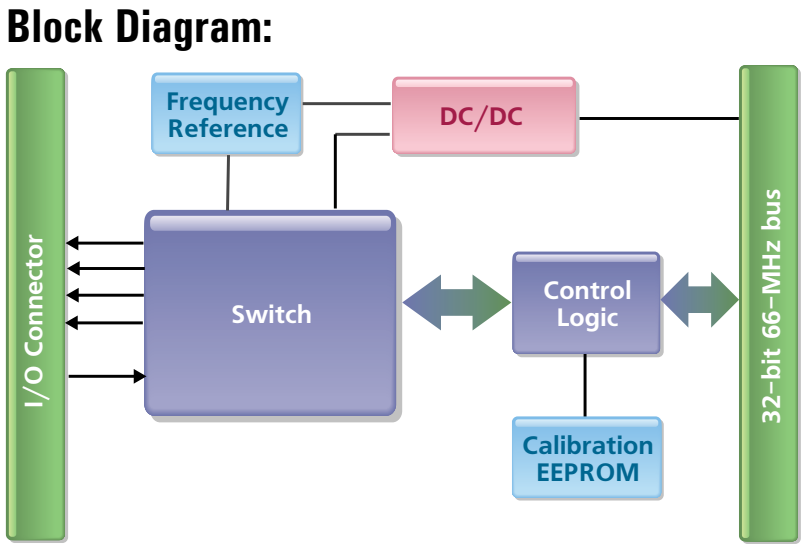

Figure 1-2. Block Diagram of DNx-CT-651 Precision Timing Reference

1.5 Functional Description

The 651 has four outputs, each of which can operate in any of five modes:

- **Input follower** – accepts input pulses (10V) at a nominal rate of 1 pps with a pulse width of 20 to 30 uS into a 50 ohm load and distributes them to up to four outputs. This mode preserves the digital shape of the input pulse and inserts minimal delay (skew) of 15-20 nS, but does not perform any validation of the input.
- **Input follower with user-set duty cycle** – similar ti input follower mode but has a user-defined duty cycle.
- **Input Auto-follower** – output follows the external input signal until it passes validation criteria. If the input becomes invalid, it switches automatically to the flywheel timing source, which adds a 30-40nS delay.
- **Input Auto- follower with user-set duty cycle –** similar to input auto-follower mode but has a user-defined duty cycle.
- **Flywheel oscillator** – output is driven by an internal flywheel counter at a user-settable rate (100/160 MHz) and duty cycle.
- **Pass-through –** timing pulses from the Sync_x buses on the Cube or RACKtangle chassis are passed through the CT-651 layer to its output channels unchanged.

- **Disabled** (OFF)

1.5.1 Registers

The 651 uses the following registers:

- **LCR** – Layer Control Register
  As the name implies, this register controls the layer.
- **FWCFG** – Output Mode Config Register
  This register selects the operating mode and sub-modes for each channel, such as input follow and input auto-follow operation
- **DW** – DAC Write Register
  This register sets the hysteresis of input signal monitoring and also adjusts the internal 20 MHz reference clock as needed. It also controls all write and operating functions of the DACs.
- **FWDC** – Flywheel Duty Cycle Register
  This register sets the duty cycle of the flywheel counter pulse
- **FWDIV** – Flywheel Output Period Register
  This register sets the total period of the flywheel counter pulse
- **FWCLK_MIN** – Flywheel Clock Divider Auto-correction Low Limit
  This register sets the low limit for monitoring flywheel period.
- **FWCLK_MAX** – Flywheel Clock Divider Auto-correction High Limit
  This register sets the high limit for monitoring flywheel period.
- **FWCRH –** Input clock “High” count in 100/160 MHz ticks
- **FWCRP –** Input clock “Period” count in 100/160 MHz ticks
- **STS** – General Status Register
  indicates when input clock fails validation and when a DAC write is in progress.

1.5.2 Operation

The general sequence of operation at startup is as follows:

1. Using the **DqAdvSetRegister( )** function, write to the LCR. This will enable the DC/DC converter for power, select 100 or 160 MHz internal flywheel clock rate “clock_fw”, and if desired, enable the 50-ohm cable termination.
2. Use the **DqAdv SetRegister ( )** function to set the following registers:
   – FWCFG output mode selection
   – DW to adjust hysteresis for input pulse conditioning
   – FWDC to control flywheel clock duty cycle
   – FWDIV to control flywheel clock period
   – FWCLK_MIN to set the FW clock divider auto-correction low limit
   – FWCLK_MIN to set the FW clock divider auto-correction high limit
3. The **DqAdv GetRegister ( )** function may be used to check the contents or status of any of the readable registers (R) or (W) listed above.

NOTE: For a more detailed description of functional operation, refer to the API User Manual.

1.6 Specifications

The following table lists the technical specifications of the CT-651 board.

Technical Specifications:

Outputs	
Output channels	4
Output selection	7 modes: 1 PPS input follower; Follower w/ user-set pulse width; Auto follower w/auto switch to flywheel; Auto follower w/ switch to flywheel and w/ user-set pulse width; 1PPS flywheel oscillator; Sync-x pass-through; Disabled (off)
Output Signal Levels	Conform to ICD-GPS-060
Output High	+10 VDC, +2/-1 VDC (@ 50 Ω)
Output Low	0 VDC, +2/-1 VDC (@ 50 Ω)
Output Clamping	Output not to exceed 13 VDC regardless of load impedance
Output chan to chan skew	2.5 nS max
Output Signal Dynamics	Conform to ICD-GPS-060 (Rv B, Fig 3-2)
Output Rise Time	< 50 nS (10% to 90%)
Output Fall Time	< 1 µS (90% to 10%)
Output Pulse Width	20 µS typical (16 µS min, 30 µS max)
Sync Input	
Input Range	0 - 10 VDC (-2 VDC min, +20 VDC max)
Input Impedance	50 Ω ±10% or >10 kΩ (SW selectable)
Switch Threshold	2.5 VDC ±5% (SW programmable between 0.5VDC and 9.5 VDC)
Sync Input to Output skew	35 nS max (@ 2.5 VDC)
Flywheel Oscillator	
Output Frequency	1 PPS
Initial Accuracy	±1 PPM
Output Stability	300 parts per billion per day
Connector	(D-sub style with 5 coaxial connections)
On-board connector	Conec 3017W5SCT78N40X or equiv
Mating connector	Conec 3017W5PXK99A10X or equiv
General	
Power dissipation	< 3 W
Operating Temp. Range	Tested -40 to +85 °C
Operating Humidity	95%, non-condensing
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500 Hz, broad-band random
Shock *IEC 60068-2-27*	50 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations
MTBF	300,000 hours
Testing Conditions	All testing assumes 50 Ω terminations at 150 foot coaxial cable unless otherwise noted

1.7 Wiring and Connectors

All external connections to the CT-651 are made through the front-accessible D-sub combination male connector. This connector has five coaxial connectors and 12 pins. The mating female connector (supplied by user) is a standard Conec Type 3017W5PXK99A10X or equivalent, which is widely available from a number of suppliers.

1.8 Pinout

The pinout of the CT-651 is illustrated below in **Figure 1-3**. Note that channels are numbered from 0 to 3.

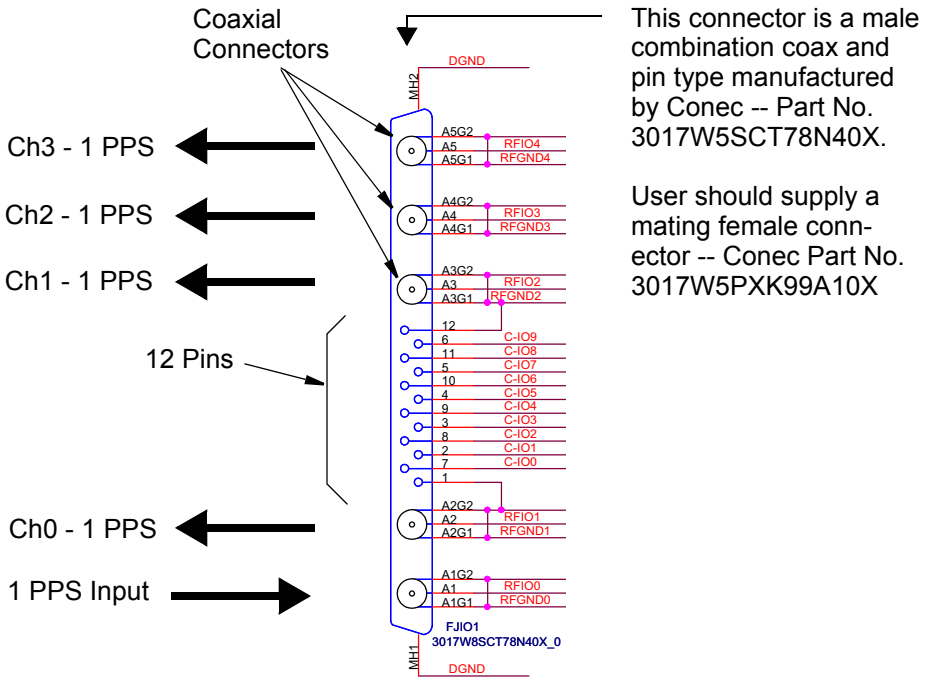

Figure 1-3. Pinout Diagram of the DNx-CT-651

1.9 Jumper Settings for DNA Version

The DNA-CT-651 module (layer) has a jumper block that assigns the position of the module within a PowerDNA Cube. The jumpers must be set to match the physical position of an I/O board or layer in the Cube.

NOTE: Since all layers are assembled in Cubes before shipment to a customer, you should never have to change a jumper setting.

In case a jumper may have been inadvertently misplaced, a diagram of the jumper block is shown in **Figure 1-4**. To set the layer address, place jumpers as shown for I/O position 1in **Figure 1-4**.

		Layer's Position as marked on the Faceplate*					
		I/O **1**	I/O **2**	I/O **3**	I/O **4**	I/O **5**	I/O **6**
Jx Pins	9-10	●●	○○	●●	○○	●●	○○
	11-12	●●	●●	○○	○○	●●	●●
	13-14	●●	●●	●●	●●	○○	○○
	15-16	●●	●●	●●	●●	●●	●●

* *All I/O Layers are sequentially enumerated from top to the bottom of the Cube*

○○ - **Open** ●● - **Closed**

Figure 1-4. Diagram of DNA-CT-651 Layer Position Jumper Settings

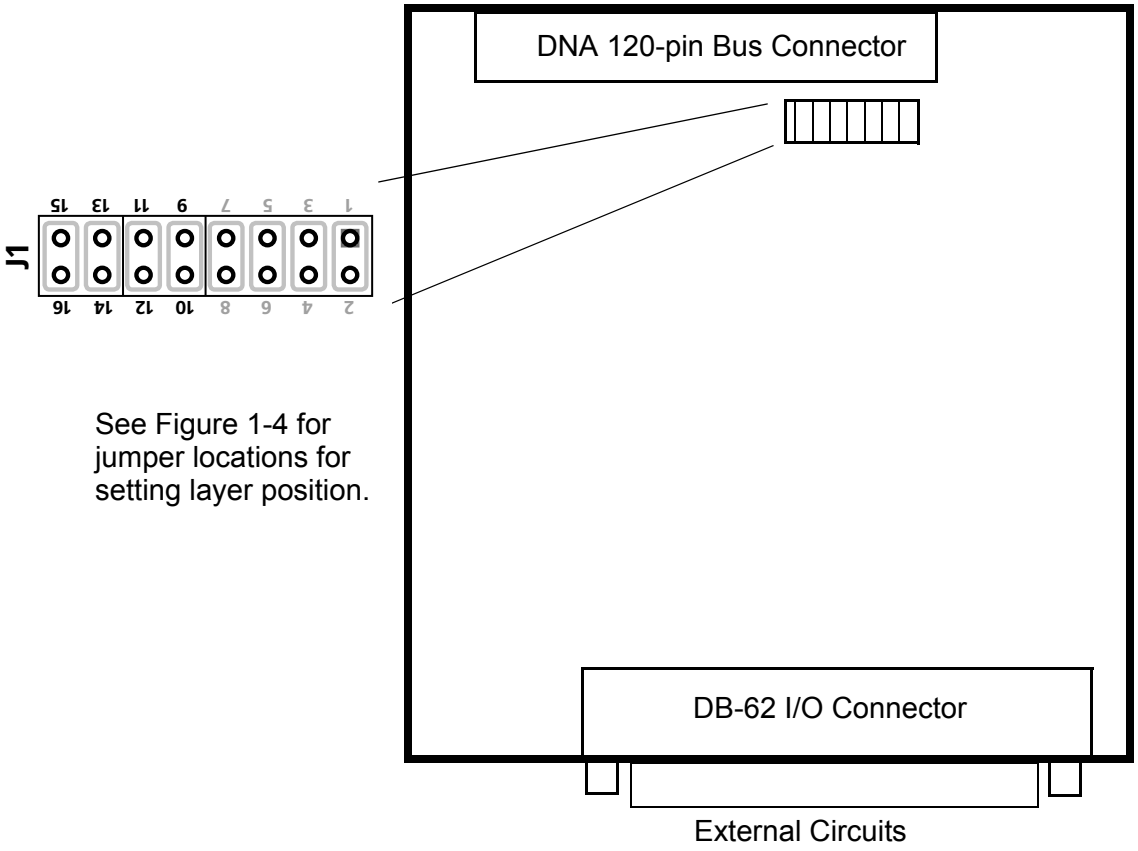

Figure 1-5. Physical Layout of DNA-CT-651 Layer Board

Chapter 2 Programming with the High-Level API

No Framework support for the CT-651 is currently available. Although it will be provided in the near future, the schedule has not yet been determined. Check with UEI periodically for current status.

Chapter 3 Programming with the Low-Level API

This section describes how to program the PowerDNA cube using the low-level API. The low-level API offers direct access to PowerDNA DAQBios protocol and also allows you to directly access device registers.

We recommend that you use UeiDaq High-level Framework (see Chapter 2), when it is available, because it is easier to use than the low-level API.

You should only need to use the low-level API if you are using an operating system other than Windows.

3.1 Data Representation

Register data is represented as 32-bit words, unless otherwise specified.

3.2 Configuration Settings

Configuration settings are passed in using the **DqAdv651SetRegister** function described below.

The following bits are used:

```
#define DQ_LN_ACTIVE     (1L<<1)   // "STS" LED status
#define DQ_LN_DCEN    (1L<<0)   // enable operations
```

`DQ_LN_ACTIVE` flag is needed to switch on “STS” LED on CPU layer.

`DQ_LN_DCEN` flag enables DC power and all operations with the layer

3.3 Layer-specific Commands and Parameters

The CT-651 layer API provides two functions that directly access configuration registers. See register definition for details. See the PowerDNA API Reference Manual for a complete description of these functions.

- **DqAdv651SetRegister()**
  This function writes `value` to the selected `reg` register. `reg` specifies the register of interest.
- **DqAdv651GetRegister()**
  This function reads `value` from the selected `reg` register. `reg` specifies the register of interest.

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