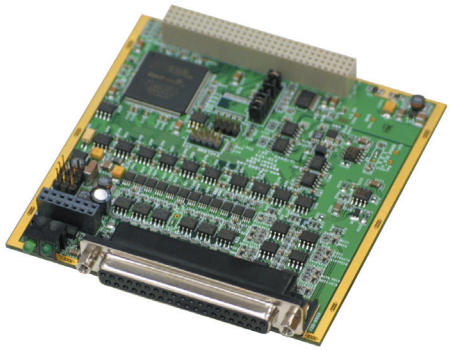
# DNA/DNR-DIO-404

## 24-Channel Industrial Digital Input/Output Interface

- DNA-DIO-404 for use with "Cube" I/O chassis
- DNR-DIO-404 for use with RACKtangle™ I/O chassis
- 12 digital inputs, 12 digital outputs (configured as current sources)
- Supports wide range of digital logic levels
- I/O throughput rate of 100kS/sec
- User-programmable hysteresis
- Outputs provide drive capability of 350 mA/channel (max peak - 500mA)
- **Requires external 3.3-36V (24V nominal) power source or can be poweredinternally using the DNA-PC-912[1] power conversion layer**



[1] When ordered with DNA-PC-912 power conversion layer, DNA-DIO-404 comes factory-configured for internal powering.

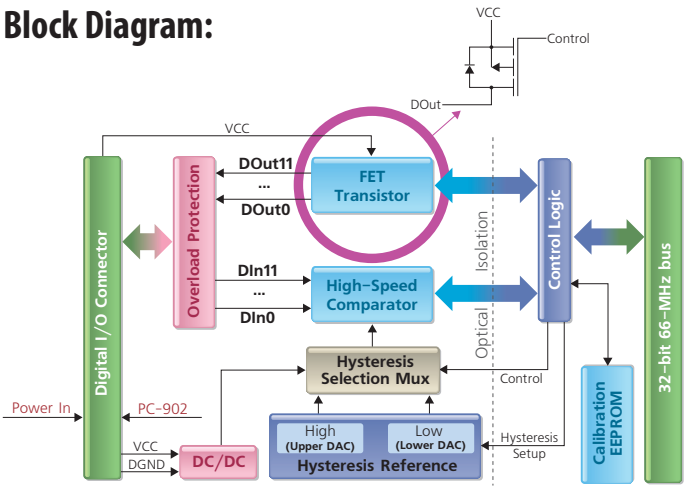
Supports **UEIDaq Framework** Data Acquisition Software Library for Windows. Linux and QNX drivers available. Visit our website for more details.

## General Description:

The DNA-DIO-404 and DNR-DIO-404 are 24 channel digital I/O interfaces for UEI's "Cube" and RACKtangle I/O chassis respectively. The DNA/DNR-DIO-404 is packed with a number of unique features: as many as 24 DIO lines 350V RMS isolated as a group, pre-configured with 12 inputs and 12 outputs, powerful user-programmable hysteresis that improves noise immunity of the digital input signals. When powered from user-provided ultra-wide voltage range (3.3-36VDC) or internal 24VDC (DNA-PC-912) power source, the DNA/DNR-DIO-404 layer is capable of continuously driving up 350mA/channel of current from all outputs, and provides readings on all inputs with available change-of-state detection.

Outputs feature low impedance FET transistors that are configured in a "high-side" mode (logic 1 connects output to the VCC via FET, logic low keeps output floating), user loads should be connected between output and ground. This layer is also capable of driving solenoids – output FET transistor has a reverse protection diode, for extra protection it is recommended to add a reverse diode directly at the inductive load. The DNA/DNR-DIO-404 has a maximum update rate of 100kS/s and is a very poplular interface in a wide variety of data acquisition, data logging and control applications..

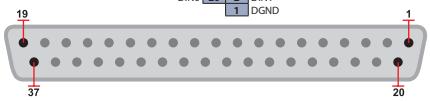
## Block Diagram:




## Pinout Diagrams:

DB-37 (female)
**37-pin connector**:

| | | | |
|---|---|---|---|
| VCC | 37 | 19 | VCC |
| DGND | 36 | 18 | VCC |
| DOUT11 | 35 | 17 | DGND |
| DOUT9 | 34 | 16 | DOUT10 |
| DOUT8 | 33 | 15 | DGND |
| DOUT6 | 32 | 14 | DOUT7 |
| DOUT5 | 31 | 13 | DGND |
| DOUT3 | 30 | 12 | DOUT4 |
| DOUT2 | 29 | 11 | DGND |
| DOUT0 | 28 | 10 | DOUT1 |
| DIN11 | 27 | 9 | DGND |
| DIN9 | 26 | 8 | DIN10 |
| DIN8 | 25 | 7 | DGND |
| DIN6 | 24 | 6 | DIN7 |
| DIN5 | 23 | 5 | DGND |
| DIN3 | 22 | 4 | DIN4 |
| DIN2 | 21 | 3 | DGND |
| DIN0 | 20 | 2 | DIN1 |
| | | 1 | DGND |




**Note:** Connect external power source to **VCC** pins. All VCC and at least 3 **DGND** pins should be used to supply external power.

## Technical Specifications:

| | | | | | |
|---|---|---|---|---|---|
| Digital Lines | 12 inputs; 12 outputs (source) | | | | |
| Logic Level | 3.3-36V; rated for 3.3V, 5V, 12V, 24V, 36V | | | | |
| Input Current | 360µA max | | | | |
| Input FIFO | 512 samples | | | | |
| Input Protection | ±40V over/under voltage, 3 kV ESD | | | | |
| Default Hysteresis Values | Lower Limit: 0; Upper Limit: 300 | | | | |
| Input High Voltage: (with default hysteresis) | @3.3V | @5V | @12V | @24V | @36V |
| | 1.6V | 2.7V | 7.5V | 12V | 17V |
| Input Low Voltage: (with default hysteresis) | @3.3V | @5V | @12V | @24V | @36V |
| | 1.5V | 1.8 | 2.0V | 3.0V | 12.5V |
| Output Drive Capacity | continuous: 350mA per channel<br>maximum peak: 500mA per channel | | | | |
| Output FIFO | 1024 samples | | | | |
| Output High Voltage:<br>3.3V at 10Ω load<br>5V at 18Ω load<br>24V at 66Ω load<br>36V at 100Ω load | <br>3.1V<br>4.5V<br>23.4V<br>35.4V | | | | |
| Output Low Voltage | Floating when driven with Logic "0" | | | | |
| Output Protection | 500mA resettable PTC fuse | | | | |
| I/O Throughput Rate | 100kHz max | | | | |
| Power Requirements (VCC) | 3.3-36V (24V nominal) - external source<br>or DNA-PC-912 internally | | | | |
| Power Consumption | 0.7W (no load) @ 3.3V VCC;<br>1.8W (no load) @ 36V VCC;<br>~ 0.22W/per output channel at 350mA load | | | | |
| Physical Dimensions | 3.875" x 3.875" (98 x 98 mm) | | | | |
| Operating Temp. Range | Tested -40 to +85 °C | | | | |
| Operating Humidity | 0 - 95%, non-condensing | | | | |

## Connection Options:

| Cable | Screw Terminal Panel | Description |
|---|---|---|
| DNA-CBL-37S | DNA-STP-37 | Shielded cable connection to 37-way terminal panel. |
| DNA-CBL-37 | DNA-STP-37 | Ribbon cable connection to 37-way terminal panel. |

# Hysteresis Setup:

Hysteresis is a very powerful feature that improves noise immunity on the digital inputs in industrial environments. Hysteresis on the DNA-DIO-404 is implemented as follows:

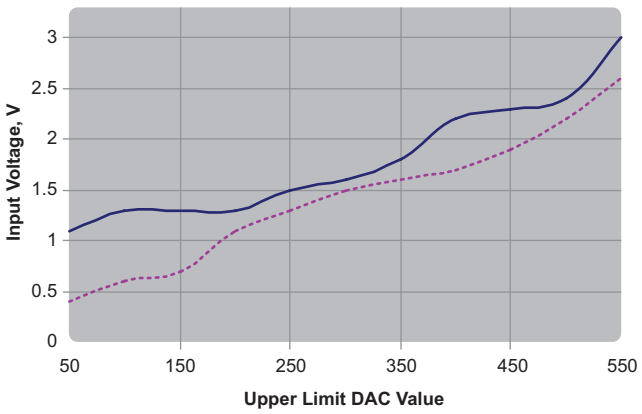
Two user programmable digital-to-analog converters are used to set upper and lower limits for the hysteresis function. These D/A converters are referred to as Lower limit DAC and Upper limit DAC. DAC outputs are connected to the high speed comparators via a multiplexer.

- All inputs initially are read from the comparators while comparing with the Lower DAC
- Another read is performed while comparators are connected to the Upper limit DAC
- If the digital input values from both reads are the same, the input signal state is assigned to the last read value
- If input values from Lower DAC and Upper DAC read are different, the input signal state remains unchanged
- This process repeats itself 1000000 times per second

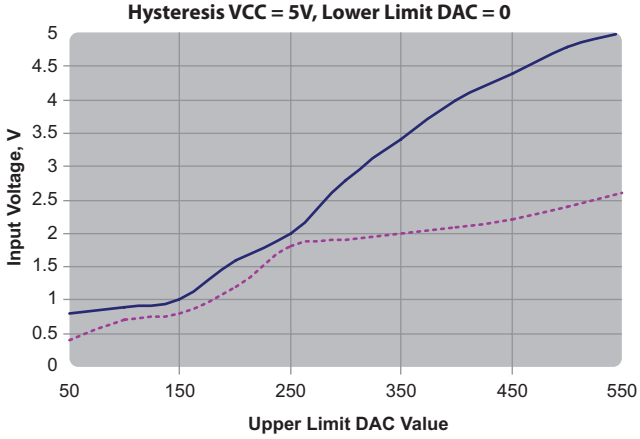
Set the hysteresis values by programming the Lower and Upper DACs. Below is a set of graphs to set hysteresis for all rated voltages, and also the function in the PowerDNA API which automatically selects the closest values of the Lower and Upper DACs based on user - requested hysteresis settings. Upper and Lower DACs may be programmed with an arbitrary integer number from 0 to 1023. The value of the Upper DAC should always be greater than LowerDAC by at least 50. Actual DAC values should be selected based on user requirements from the graphs below.

On all graphs below, the blue solid line represents voltage required on the input for the low-to-high transition, and pink dashed line represent voltage required on the input line for the high-to-low transition.

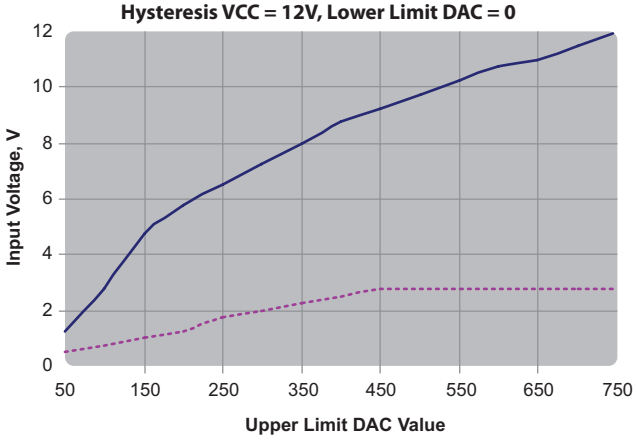
**Hysteresis VCC = 3.3V, Lower Limit DAC = 0**



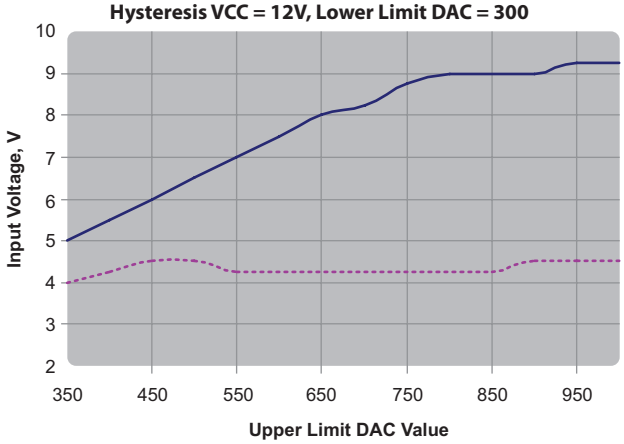

**Hysteresis VCC = 5V, Lower Limit DAC = 0**



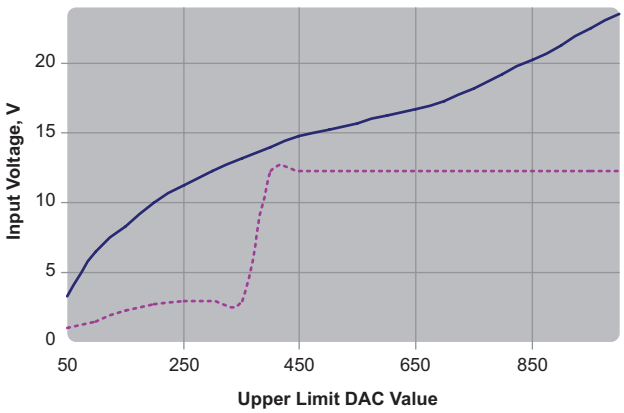

**Hysteresis VCC = 12V, Lower Limit DAC = 0**



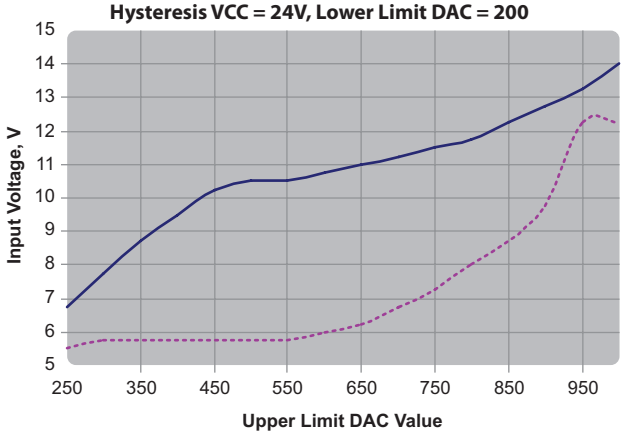

**Hysteresis VCC = 12V, Lower Limit DAC = 300**



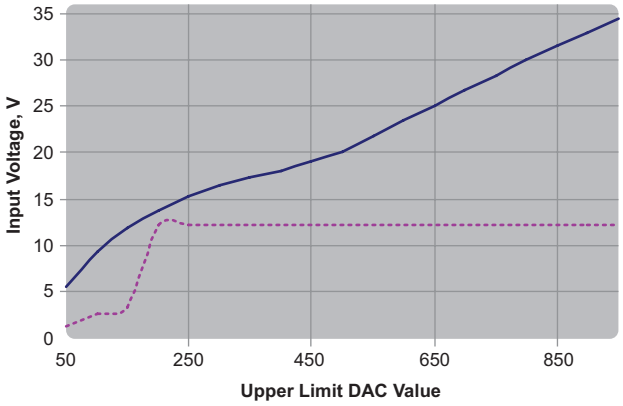

**Hysteresis VCC = 24V, Lower Limit DAC = 0**




**Hysteresis VCC = 24V, Lower Limit DAC = 200**



**Hysteresis VCC = 36V, Lower Limit DAC = 0**




**Hysteresis VCC = 36V, Lower Limit DAC = 300**