United Electronic Industries

The High-Performance Alternative

DNx-DIO-448
Digital Input Layer
User Manual

48-channel Digital Input Layers
for PowerDNA Cube and PowerDNR RACKtangle Systems

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Contacting United Electronic Industries

Mailing Address:

27 Renmar Avenue
Walpole, MA 02081
U.S.A.

For a list of our distributors and partners in the US and around the world, please see
http://www.ueidaq.com/partners/

Support:

Telephone: (508) 921-4600
Fax: (508) 668-2350

Also see the FAQs and online “Live Help” feature on our web site.

Internet Support:

Support: support@ueidaq.com
Web-Site: www.ueidaq.com
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Chapter 1 Introduction

This document outlines the feature set and use of the DNA-DIO-448 digital input layer when used with the UEI PowerDNA I/O Cube. The DNA-DIO-448 is a 48-channel Digital Input Layer designed for use with the PowerDNA 3- or 6-layer Ethernet-based Cube. The DNR-DIO-448 is designed for use with a PowerDNR RACKtangle™ rack-mounted system.

1.1 Organization of this manual

This PowerDNA DIO-448 User Manual is organized as follows:

- **Introduction**
  This chapter provides an overview of DNx-DIO-448 Digital Input board features, accessories, and what you need to get started.
- **The DIO-448 Layer**
  This chapter provides an overview of the device architecture, connectivity, and logic of the DIO-448 layer.
- **Programming with the High-Level API**
  This chapter provides a general description of the how to create a session, configure the session for digital data acquisition/output, and format relevant data, using the Framework High-Level API.
- **Programming with the Low-Level API**
  This chapter describes Low-level API commands for configuring and using the DIO-448 layer.
- **Appendices**

  A. Accessories
  This appendix describes the accessories available for use with the DIO-448 layer.
- **B. Layer Verification**
  This appendix outlines how to verify calibration for the DIO-448 layer.
- **Index**
  This is an alphabetical listing of the topics covered in this manual.

Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:

Tips are designed to highlight quick ways to get the job done, or reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.

CAUTION! *advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

Text formatted in **bold** typeface generally represents text you should be entered verbatim. For instance, it can represent a command, as in the following example: “You can instruct users how to run setup using a command such as **setup.exe**.”

1.2 The DIO-448 Layer

The DNx-DIO-448 is a 48-channel, high performance, digital input layer designed for use in a wide variety of digital monitoring applications. To maximize throughput, the board has two 24-bit ports, each of which sends data to the PowerDNA cube in a single 24-bit write. The board can monitor all 48 bits at sustained sampling rates of more than 1 kS/second.

Each of the 24-bit ports is configured with 33kOhm pullup or pulldown resistors, which makes the board ideal for monitoring contact closures as well as common voltage inputs. The resistors on each port are configured by connecting the PLEVEL pins for each group of 24 inputs on the I/O connector either to Vcc (for pullup) or ground (for pulldown). (Refer to **Figure 1-4** on page 6.)

A novel feature of the board is the use of an A/D converter to sense the signal level of each digital input. Using this feature, you can program the specific switching signal level for each digital input on the board, offering you the flexibility needed to function in a wide variety of applications. Hysteresis (deadband setting) is independently programmable on each 24-bit port over the full input range. For detailed information on setting hysteresis values, refer to Chapter 2 of this manual and to the **DqAdv448SetLevels** function in the Framework API Reference Manual.

The board also offers user-programmable debouncing with delay intervals that can be set independently for each channel from 0 to 6.5 Sec. In addition, a diagnostic input mode monitors the static analog voltage on each input channel, which enables you to immediately detect and localize a short, open, marginal, or failing drive circuit. For more information, refer to Chapter 2 of this manual and to the **DqAdv448SetDebouncer** function in the Framework API Reference Manual.

Each board provides 350 Vrms isolation between the I/O, cube, and other installed I/O layers. All inputs are protected against overvoltage to ±40VDC and also against ESD.

The DIO-448 is fully supported by the UEIDAQ Framework software API, which provides a simple and complete interface to all popular programming languages, operating systems, and data acquisition/control applications, such as LabVIEW, DASYLab, and MATLAB.

1.2.1 Technical Specifications

The technical specifications for the DNA-DIO-448 layer are listed in **Table 1-1**.

Table 1-1. Technical Specifications

Technical Specifications:

Number of channels	48 digital inputs
Port configuration	Two 24-bit ports
Input high voltage	Programmable from 0 to Vcc (default: 12 V @ Vcc = 28 VDC)
Input OFF voltage	Programmable from 0 to Vcc (default: <1.25 V @ 28 VDC)
Hysteresis (voltage input)	Programmable, 0 to Vcc (default 10.25 VDC)
Input impedance	> 33 k Ohm.
Input open circuit state	Programmable high or low via 33 kOhm pull up/pull down. Each pull up/down selection sets the configuration for 24 channels)
Input FIFO	256 words
Input Throughput Rate	1 kHz max
Diagnostic voltage measurement accuracy	± 25 mV (Source impedance ≤ 100 Ohm)
Input protection	- 25 to + 75 V, and ESD
Input Isolation	350 Vrms
Power dissipation	2 W
Operating Temp. Range	Tested -40 to +85 °C
Operating Humidity	95%, non-condensing
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500 Hz, broad-band random
Shock *IEC 60068-2-27*	50 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations
MTBF	TBD hours

1.2.2 Photos

Figure 1-1 shows a photo of the DNA-DIO-448 board. The DNR version is basically the same except that it has a 120-pin connector that plugs into a backplane on the RACKtangle rack-mounted enclosure. See **Figure 1-2**. The DNR version also does not have a jumper block for setting layer position within the enclosure as the DNR version determines layer position automatically.

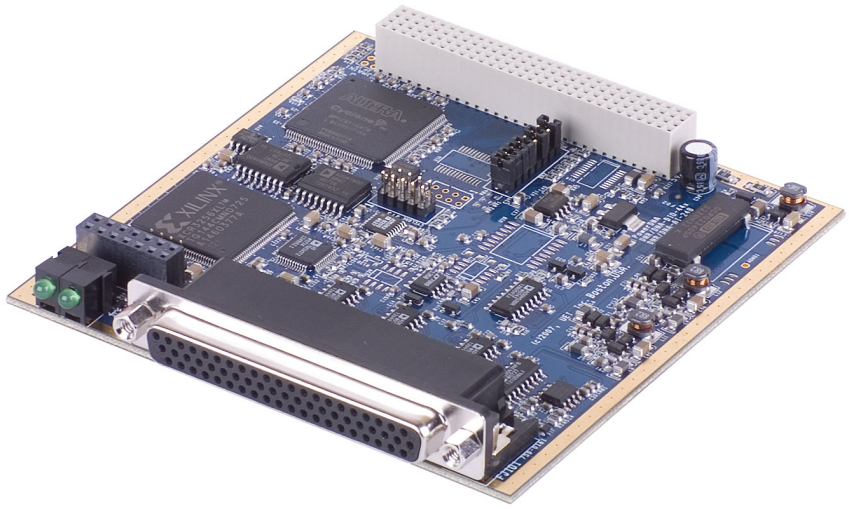


Figure 1-1 DNA-DIO-448 Digital I/O Layer

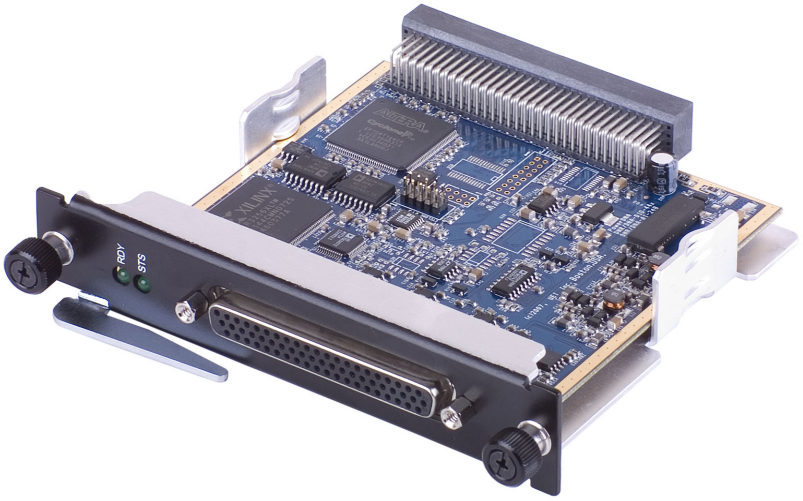


Figure 1-2. DNR-DIO-448 Digital I/O Layer

1.3 Device Architecture

The DIO-448 Layer accepts 48 digital inputs. A block diagram of the board layer is shown in **Figure 1-3**.

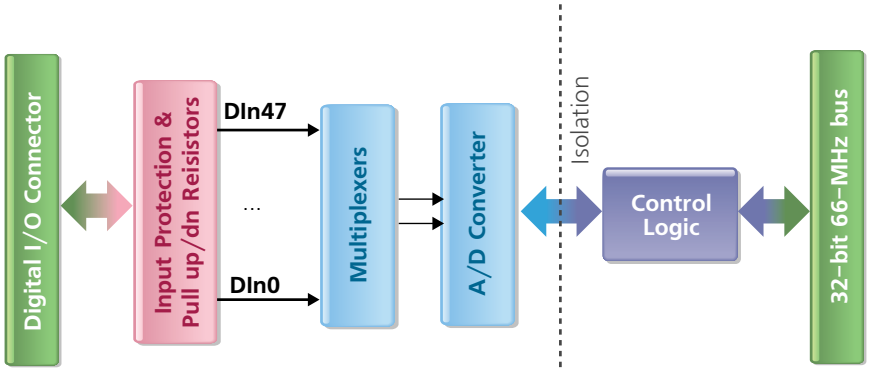


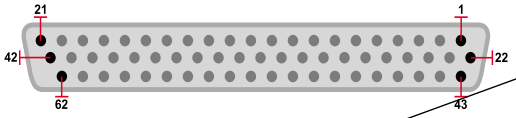
Figure 1-3 Block Diagram of DIO-448 Device Architecture

Note that the I/O part of the layer is isolated from the logic interface by inductive isolators and that overvoltage protection is provided on all inputs

1.4 Layer Connectors and Wiring

The pinout of the DB-37 62-pin female connector for the DIO-448 Layer board is shown in **Figure 1-4**.

PLEVEL 0-23 selects pullup/pulldown resistors for channels 0 to 23



PLEVEL 24-47 selects pullup/pulldown resistors for channels 24 to 47

Pin	*Signal*	*Pin*	*Signal*	*Pin*	*Signal*
1	PLEVEL 0-23	22	PLEVEL 24-47	43	Gnd
2	Rsvd	23	Gnd	44	NC
3	Rsvd	24	Gnd	45	Gnd
4	Rsvd	25	NC	46	DIn 47
5	DIn 45	26	DIn 46	47	DIn 44
6	DIn 42	27	DIn 43	48	DIn 41
7	DIn 39	28	DIn 40	49	DIn 38
8	DIn 36	29	DIn 37	50	DIn 35
9	DIn 33	30	DIn 34	51	DIn 32
10	DIn 30	31	DIn 31	52	DIn 29
11	DIn 27	32	DIn 28	53	DIn 26
12	DIn 24	33	DIn 25	54	DIn 23
13	DIn 21	34	DIn 22	55	DIn 20
14	DIn 18	35	DIn 19	56	DIn 17
15	DIn 15	36	DIn 16	57	DIn 14
16	DIn 12	37	DIn 13	58	DIn 11
17	DIn 9	38	DIn 10	59	DIn 8
18	DIn 6	39	DIn 7	60	DIn 5
19	DIn 3	40	DIn 4	61	DIn 2
20	DIn 0	41	DIn 1	62	NC
21	NC	42	Gnd		

NC - No Connection (Do not use)
Rsvd - Reserved (Do not use)

Figure 1-4 DB-62 I/O Connector Pinout

Note that the DIO-448 inputs are numbered from DIn0 through DIn47.

When power is provided to the layer, the RDY LED turns on. When no power is supplied, the RDY LED is off, and the DIO-448 layer cannot operate.

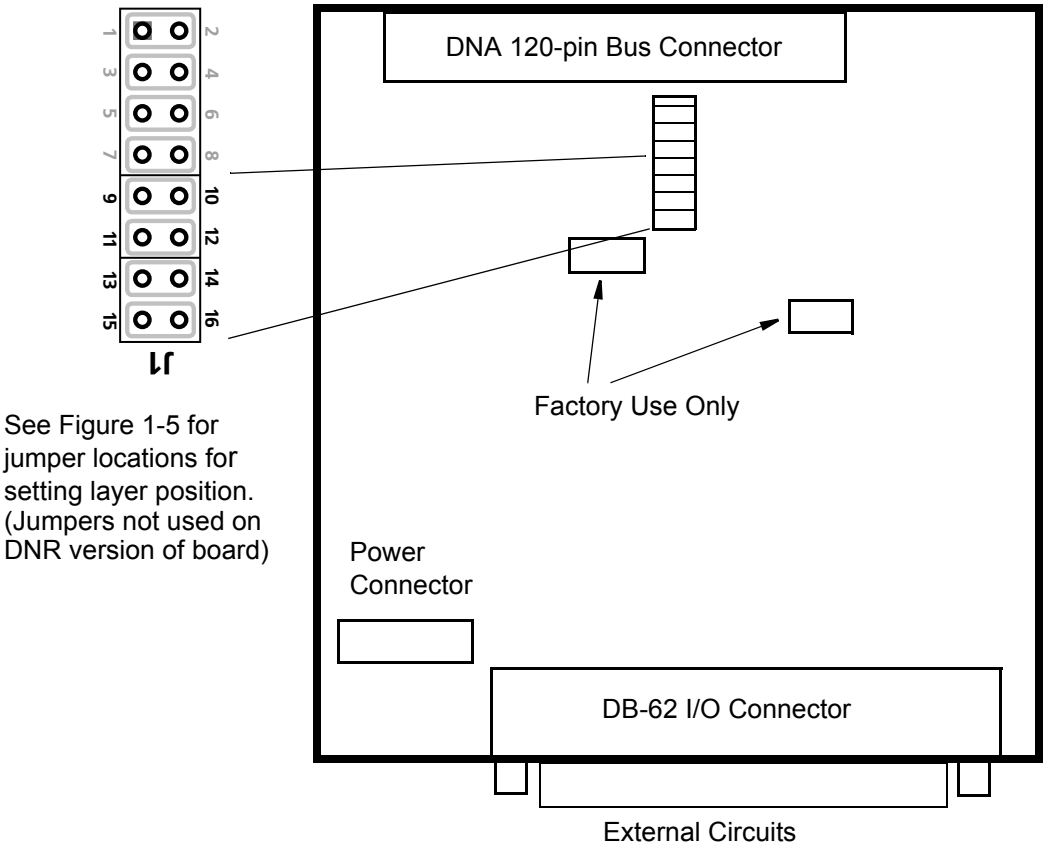


Figure 1-5. Physical Layout of DNA-DIO-448 Layer Board

1.4.0.1 Jumper Settings

A diagram of the jumper block is shown in **Figure 1-6**. To set the layer position jumpers, place jumpers as shown in **Figure 1-6**. (Not applicable to DNR version.)

		Layer's Position as marked on the Faceplate*					
		I/O **1**	I/O **2**	I/O **3**	I/O **4**	I/O **5**	I/O **6**
Jx Pins	9-10	● ●	○ ○	● ●	○ ○	● ●	○ ○
	11-12	● ●	● ●	○ ○	○ ○	● ●	● ●
	13-14	● ●	● ●	● ●	● ●	○ ○	○ ○
	15-16	● ●	● ●	● ●	● ●	● ●	● ●

* *All I/O Layers are sequentially enumerated from top to the bottom of the Cube*

○ ○ - **Open** ● ● - **Closed**

Figure 1-6. Diagram of DNA-DIO-448 Layer Position Jumper Settings

1.4.0.2 Input Circuits Each input circuit is configured as shown in **Figure 1-7** or **Figure 1-8**.

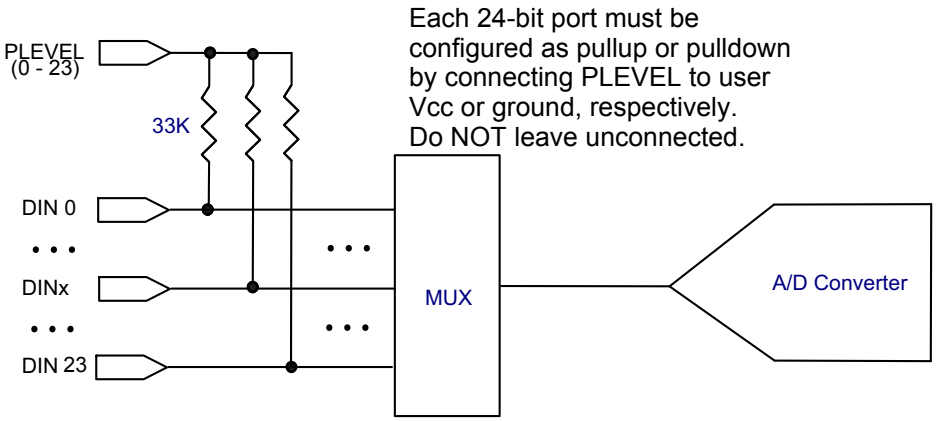


Figure 1-7. Typical Input Circuit Diagram for Channels 0 to 23 (Port 1)

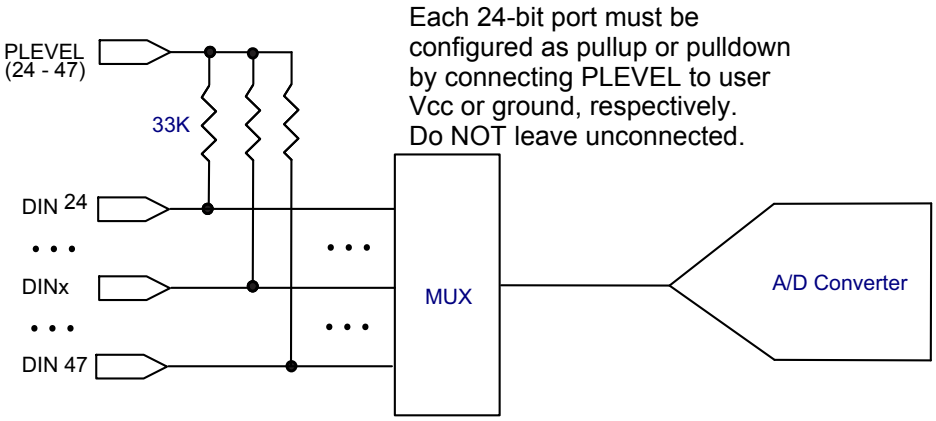


Figure 1-8. Typical Input Circuit Diagram for Channels 24 to 47, Port 2

Chapter 2 Programming with the High Level API

This section describes how to control the DIO-448 with the UEIDAQ high-level API, called Framework.

Framework is object oriented; its objects can be manipulated in the same manner from a wide range of development environments such as Visual C++, Visual Basic or LabVIEW.

The following section focuses on the C++ API, but the concept is the same no matter what programming language you use.

Please refer to the “UeiDaq Framework User Manual” for more information on using other programming languages.

2.1 Creating a Session

The Session object controls all operations on your PowerDNA device. Therefore, the first task is to create a session object:

```
CUeiSession session;
```

2.2 Configuring the Resource String

Framework uses resource strings to select which device, subsystem and channels to use within a session. The resource string syntax is similar to a web URL:

```
<device class>://<IP address>/<Device Id>/<Subsystem><Channel list>
```

For PowerDNA, the device class is **pdna**.

For example, the following resource string selects digital input ports 0,1 on device 1 at IP address 192.168.100.2: "pdna://192.168.100.2/Dev1/Di0,1"

NOTE: In Framework, a digital channel corresponds to a physical port on the device. You cannot configure a session only to access a subset of lines within a digital port.

NOTE: Sessions are unidirectional. If your device has both input and output ports or has bidirectional ports, you need to configure two sessions: one for input and one for output.

Use the method **CreateDIIndustrialChannel()** to program the advanced features of the DIO-448, such as the levels at which the input line states change, as well as a digital filter to eliminate glitches and spikes

The following call configures the digital input ports of a DIO-448 set as device 1:

```
session.CreateDIIndustrialChannel("pdna://192.168.100.2/Dev1/Di0:1",
                                  1.5,
                                  5.0,
                                  1.0);
```

It configures the following parameters:

- Low Threshold: the low hysteresis threshold.
- High Threshold: the high hysteresis threshold.
- Digital input filter (debouncer): the minimum pulse width in ms. Use 0.0 to disable the digital input filter.

To read the voltage and current flowing through each of the digital input lines, you must treat the DIO-448 like an analog input device and create a new analog input session (different from the one you are using to read the digital states of the input lines) and configure the input lines you want to read from:

```
CUeiSession aiSession

// Read voltage from all 48 lines. Only the first parameter
// "resource" is used with the DIO-448, the other parameters
//  are ignored.
aiSession.CreateAIChannel("pdna://192.168.100.2/Dev1/Ai0:47",
                  -10, 10,UeiAIChannelInputModeDifferential);
```

2.3 Configuring the Timing

You can configure the DIO-448 to run in simple mode (point by point), buffered mode (ACB mode), or DMAP mode.

- In simple mode, the delay between samples is determined by software on the host computer.
- In DMAP mode, the delay between samples is determined by the DIO-448 on-board clock, and data is transferred one scan at a time between PowerDNA and the host PC.
- In buffered mode, the delay between samples is determined by the DIO-448 on-board clock, and data is transferred in blocks between PowerDNA and the host PC.

The following sample shows how to configure the simple mode. Please refer to the "UeiDaq Framework User Manual" to learn how to use the other timing modes.

```
session.ConfigureTimingForSimpleIO();
aiSession.ConfigureTimingForSimpleIO();
```

2.4 Reading Data

Reading analog and digital data from the DIO-448 is done using reader objects.

The following sample code shows how to create a scaled reader object and read samples.

```
// Create a reader and link it to the digital session's stream
CUeiDigitalReader diReader(session.GetDataStream());

// Create a reader and link it to the digital session's stream
CUeiAnalogScaledReader aiReader(aiSession.GetDataStream());

// read one digital scan, the buffer must be big enough to contain
// one value per port
uInt32 data[2];
reader.ReadSingleScan(data);

// Read voltages from all input lines
double volts[48];
aiReader.ReadSingleScan(volts);
```

2.5 Cleaning-up the Session

The session object will clean itself up when it goes out of scope or when it is destroyed. However, you can manually clean up the session (to reuse the object with a different set of channels or parameters).

```
session.CleanUp();
 aiSession.CleanUp();
```

Chapter 3 Programming with the Low-Level API

The low-level API offers direct access to PowerDNA DAQBios protocol and allows you to directly access device registers.

We recommend that you use the UeiDaq Framework (*see Chapter 2*), which is easier to use.

You should need to use the low-level API only if you are using an operating system other than Windows.

Please refer to the `API Reference Manual` document under:

Start » Programs » UEI » PowerDNA » Documentation

for pre-defined types, error codes, and functions for use with this layer.

Appendix

A. Accessories

The following cables and STP boards are available for the DIO-448 layer.

DNA-CBL-62

A 3ft, 62-way flat ribbon cable that connects the layer to a terminal panel.

DNA-STP-62

62-way screw terminal panel.

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