The following FAQ is for the DNx-PL-820 board, a highly customizable programmable logic interface for the PowerDNA Cube and RACK chassis.

What is the PL-820?

The PL-820 is a two board device that consists of a Cyclone II FPGA base-board and an Altera MAX 10 complex programmable logic device (CPLD) daughter-board.

The MAX 10 CPLD daughter-board can be programmed with a custom FPGA design. The FPGA of the base-board interfaces the Altera MAX 10 to the PowerDNA system.

How are the board and I/O pins physically configured in a UEI system?

The PL-820 requires two slots in a UEI chassis. In Cube chassis, the board requires two consecutive slots. In a RACK chassis, the board requires mounting in the last slot.

The PL-820 provides two 62-pin I/O connectors (female DB62):

- 105 GPIO pins are available for connection to user I/O: 54 pins are provided on the base-board's I/O connector, and 51 pins are provided on the MAX 10 board connector.
- JTAG interface on the MAX 10 DB62 connector for FPGA programming

Each user I/O pin is protected with a 165 Ω series resistor and ESD protection diodes. The layout of both I/O connectors is mostly symmetrical.

What is the feature set of the user-programmable MAX 10 FPGA?

The MAX 10 FPGA is a 10M50DCF484 series device with the following features:

- Two reference clocks, 1 kHz and 33 MHz, provided by the Cyclone II base-board
- Up to 50,000 FPGA cells available
- Up to 1683 kByte available block memory
- 144 (18x18) embedded multipliers
- 4 PLLs available
- Up to 736 kByte user flash memory
- Instant-on capability on the MAX 10, allowing MAX 10 applications to run immediately independent to the Cube or RACK boot-up state
- User and dual configuration FLASH, DSP blocks, and Nios II embedded processor functionality

Does the MAX 10 FPGA ship with an initial image?

The MAX 10 chip is initialized at the factory with an FPGA image that configures registers, the two serial peripheral interfaces (SPIs), and the synchronous serial interface (SSI), as well as clocks and other access hardware. Our initial image sets each I/O pin as a general purpose DIO. With the UEI API, users can set each I/O bit independently as an input or output.

NOTE: UEI provides the FPGA code for our initial MAX 10 image. Users must wrap their FPGA design around our initial image and keep the same register map and SSI configuration to use our established API.

How do I download my FPGA image to the MAX 10 target?

The Altera Quartus II 64-bit Programmer, release 15.0, includes support for programming MAX 10 series devices. The MAX 10 chip can be programmed via the JTAG interface accessible on the DB62 connector using this version of the Quartus programmer.

The MAX 10 chip is fully programmable by the user using the Altera development tools.

How do I communicate with the PL-820 and my custom design?

UEI provides a high level, easy to use API that allows you to read and write registers established in our initial image and configure and use the two SPI ports connecting the Cyclone and MAX 10 chips. The API allows you to program the MAX 10 chip from your host PC through the Cube/RACK's Ethernet port and allows you to control/monitor all the GPIO included on the Cyclone II board (and the MAX 10 in its default state).

UEI supplies example code for PL-820 C programming. Our API is compatible with Windows, Linux, VxWorks, QNX and other operating systems.

What security features does the PL-820 offer?

The following features prevent unauthorized reading and writing of the MAX 10 image:

- The PL-820 provides jumpers on the board that allow the JTAG interface to be disconnected from the I/O pins
- The MAX 10 supports a nonvolatile security key, which prevents the MAX 10's FPGA image from being read or written

For more information:

Please contact UEI support at support@ueidaq.com or call 508.921.4600 with any questions.