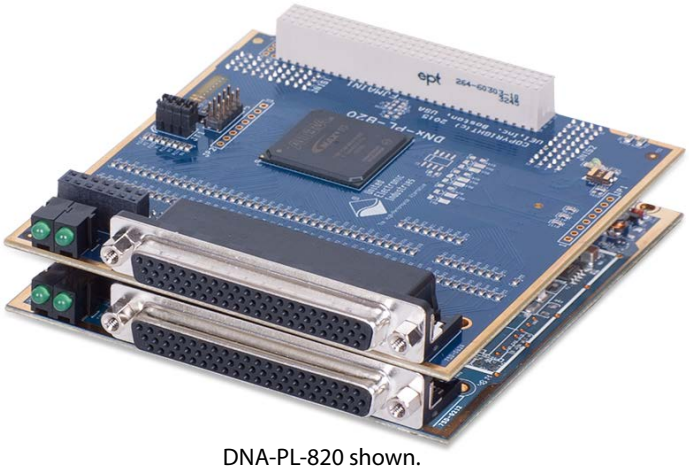
DNA/DNR-PL-820

Programmable FPGA board

- DNA-PL-820 for use in "CUBE" chassis
- DNR-PL-820 for RACKtangle™ I/O chassis
- Ideal for development of custom high speed controllers
- MAX 10 FPGA with 50k usable logic elements
  - 1638 kB usable embedded memory,
  - 144 embedded multipliers
  - 4 internal PLLs for timing/clock generation
  - Instant-on functionality
- Uses standard Altera Quartus II toolkit
- Reprogrammable in-system with UEI software or through external JTAG connection
- DB62 I/O connectors

10-Year Availability Guarantee



DNA-PL-820 shown.
There is a mimumum quantity purchase on the DNx-PL-820. Please call us for details.

General Description:

The DNA-PL-820 and DNR-PL-820 are user programmable FPGA boards compatible with UEI's popular Cube and RACKtangle chassis respectively. The board allows an FPGA programmer to add custom FPGA functionality to the DNx family and the various platforms it supports. The DNA/DNR versions are electronically identical and differ only in the mechanical features required for installation in the RACKtangle or Cube.

The DNx-PL-820 is a two board, base/daughter card product. The bottom board (left in a DNR RACK) includes a Cyclone II FPGA while the upper board (right in the RACK) provides a MAX 10 FPGA. The Cyclone board is used exclusively as the interface between the DNx bus and the MAX 10 FPGA chip. The MAX 10 chip is fully programmable by the user using popular Altera development tools, including the embedded Nios II processor.

The MAX 10 board allows user developed FPGA applications to be installed and run on the board. 104 GPIO pins are brought out from the MAX 10 FPGA and are available for connections to user I/O. 51 bits are provided on the Cyclone board's I/O connector while 53 are provided on the MAX 10 board connector.

The MAX 10 has a variety of unique and powerful features that make it an ideal choice as a custom FPGA target. Included in these features is a unique, instant-on capability that allows the MAX 10 application to begin running immediately, without regard to whether the Cube or RACKtangle has completed its boot-up process. The MAX 10 also supports user and dual configuration FLASH, DSP blocks and Nios II embedded processor functionality.

The MAX 10 chip may be programmed by a JTAG interface that is brought out to the I/O connector or by the DNA backplane (via the Cyclone chip)by a utility provided by UEI. A set of jumpers on the board allows the JTAG interface to be disabled when security concerns mandates it. Security is further provided by the MAX 10's implementation of a nonvolatile security key. Without the key the MAX 10's FPGA image cannot be read or written.

The unit is shipped with an FPGA Image installed in the MAX 10 that simply sets each I/O pin as a general purpose DIO pin. The UEI API can then set each I/O bit independently as input or output. The PL-820 includes a test adaptor that connects the I/O pins from the Cyclone II board's I/O connector to the MAX 10 board's I/O connector (recall all GPIO pins are connected to the MAX 10). This allows each I/O pin to be exercised as both input and output and allows a quick self-test to ensure all I/O pins are fully functional

Technical Specifications:

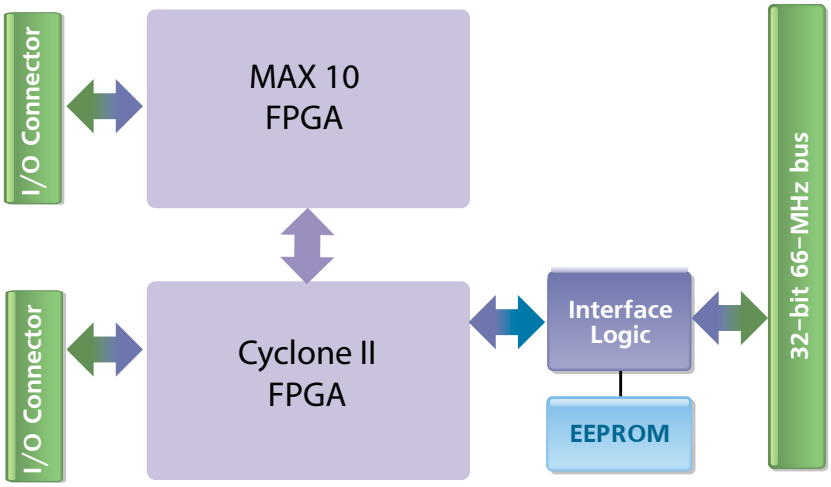
Formats	DNA-series for "Cube" chassis DNR-series for RACKtangle chassis
FPGA type	MAX 10, 10M50DCF484 series
Clock Frequency	two programmabe clocks,up to 33 MHz, provided by Cyclone II chip
FPGA Cells available	up to 50,000
Available block memory	up to 1,638 kiloByte
Embedded multipliers	144 (18 x 18)
PLLs available	4
User Flash memory	up to 736 kByte
A/D converters	2 plus one internal temp sensor
I/O connectors	62-pin "D" (female DB62)
I/O configuration	Cube: Requires two consecutive slots RACK: Requires mounting in slot 12
Power consumption	5.0 W not including power sourced to external circuitry
Operating temp. (tested)	-40°C to +85°C
Operating humidity	95%, non-condensing
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500Hz, broadband random
Shock *IEC 60068-2-27*	50 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations
MTBF	500,000 hours

The Cyclone chip communications with the MAX 10 utilizing two, fully programmable SPI interfaces. An fixed SSI interface is also included but it is currently reserved for system level configuration purposes. The Cyclone chip also provides two programmable clock signals to the MAX 10.

Unlike most DNx series boards, the DNx-PL-820 is not isolated from the DNx chassis. However, all I/O pins are protected with 165 Ohm series resistors and low capacitance bidirectional protection diodes.

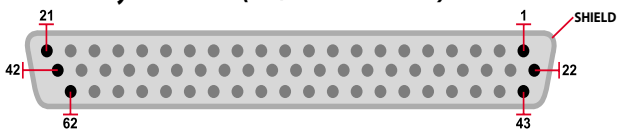
Software for the DNx-PL-820 includes a high level, easy to use interface that allows you to configure and use the two SPI ports that connect the Cyclone and MAX 10 chips. It also allow you to program the MAX 10 chip from your host PC through the Cube/RACK's Ethernet port. Finally the software provided allows you to control/monitor all the GPIO included on the Cyclone II board (and the MAX 10 in its default state). The API provided is compatible with Windows, Linux, VxWorks, QNX and more.

Block Diagram:



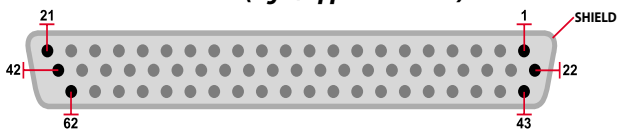
Pinout: (62-pin female dSub connectors)

Cyclone Board (left/lower connector)



Pin	*Signal*	*Pin*	*Signal*	*Pin*	*Signal*
1	+3.3 V	22	GND	43	GND
2	DIO 52	23	DIO 51	44	DIO 53
3	DIO 55	24	DIO 54	45	DIO 56
4	DIO 58	25	DIO 57	46	DIO 59
5	DIO 61	26	DIO 60	47	DIO 62
6	DIO 64	27	DIO 63	48	DIO 65
7	DIO 67	28	DIO 66	49	DIO 68
8	DIO 69	29	GND	50	DIO 70
9	DIO 72	30	DIO 71	51	DIO 73
10	DIO 75	31	DIO 74	52	DIO 76
11	DIO 78	32	DIO 77	53	DIO 79
12	DIO 81	33	DIO 80	54	DIO 82
13	DIO 84	34	DIO 83	55	DIO 85
14	GND	35	DIO 86	56	DIO 87
15	DIO 89	36	DIO 88	57	DIO 90
16	DIO 92	37	DIO 91	58	DIO 93
17	DIO 95	38	DIO 94	59	DIO 96
18	DIO 98	39	DIO 97	60	DIO 99
19	DIO 101	40	DIO 100	61	DIO 102
20	DIO 104	41	DIO 103	62	GND
21	GND	42	rsvd		

MAX 10 Board (right/upper connector)



Pin	*Signal*	*Pin*	*Signal*	*Pin*	*Signal*
1	+3.3 V	22	GND	43	GND
2	DIO 49	23	DIO 50	44	DIO 48
3	DIO 46	24	DIO 47	45	DIO 45
4	DIO 43	25	DIO 44	46	DIO 42
5	DIO 40	26	DIO 41	47	DIO 39
6	DIO 37	27	DIO 38	48	DIO 36
7	DIO 34	28	DIO 35	49	DIO 33
8	DIO 32	29	GND	50	DIO 31
9	DIO 29	30	DIO 30	51	DIO 28
10	DIO 26	31	DIO 27	52	DIO 25
11	DIO 23	32	DIO 24	53	DIO 22
12	DIO 20	33	DIO 21	54	DIO 19
13	DIO 17	34	DIO 18	55	DIO 16
14	GND	35	DIO 15	56	DIO 14
15	DIO 12	36	DIO 13	57	DIO 11
16	DIO 9	37	DIO 10	58	DIO 8
17	DIO 6	38	DIO 7	59	DIO 5
18	DIO 3	39	DIO 4	60	DIO 2
19	DIO 0	40	DIO 1	61	JTAG TCK
20	JTAG TDO	41	JTAG TMS	62	GND
21	GND	42	JTAG TDI		