# PD2-A0-32/16HC

## 32-Channel PCI Card for High-Current Analog Output

- 32 analog outputs (16-bit resolution)
- 8 digital inputs; 8 digital outputs
- Output current up to ±90 mA continuous, per channel
- Maximum peak current 100 mA per channel
- Three 24-bit counters/timers; three clock/interrupt lines
- Channel list (64 locations)
- Independent waveform on each channel
- · Simultaneous channel update; update on external event
- 2k samples onboard buffer size (upgradable to 64k samples)



Board comes with a "Y"-split power cable (with molex-type connectors) and a set of jumpers for sensing configuration (refer to the table below for more details).

Supports UEIDag Framework Data Acquisition Software Library for Windows, Linux and QNX drivers available. Visit our website for more details.

## **General Description:**

Most analog output cards for the PCI bus generate voltages in the range of 10V and currents peaking at 20 mA. Thus, when test engineers find that their applications need more "oomph", they almost always turn to external I/O modules on a rack, which adds cost and inconvenience. Thanks to United Electronic Industries that extra rack is no longer necessary. UEI has developed two special versions of its popular 32-channel PD2-AO-32/16 analog-output card. The PD2-AO-32/16HC is a high-current version that supplies 90 mA per channel continuously on each of its output lines.

In more detail, the PD2-AO-32/16HC can source or sink 90 mA continuously per channel with the peak output of 100 mA/channel for no longer than 1 min. Further,

the maximum aggregate output current is 1.725A at 10V or 1.625A at -10V. Note that adequate cooling is needed if the board sinks more than 1.25A total, but simply adding a fan in the chassis is generally sufficient.

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Analog Outputs		
Number of channels	32	
Resolution	16 bits	
Update rate	100 kS/s per channel;	
	450kS/s aggregate in non-DMA mode;	
	up to 1100 kS/s aggregate in DMA mode	
DSP buffer size	2k samples (2 buffers x 1k sample)	
Type of D/A	double-buffered	
Data transfer modes	DMA, interrupt, software	
Accuracy	±3 LSB max	
DNL	±3 LSB max	
Monotonicity over temp.	15 bits, -40 to 85°C	
Calibrated gain error	3mV typ, 6mV max @ ±9.8V	
Calibrated offset error	2mV typ, 4mV max @ 0.0V	
Output range	±10V	
Output coupling	DC	
Output impedance	0.15Ω max	
Output current	±90 mA; 100 mA max (per channel)	
Gain error vs load	±0.05% @ 0-20 mA, ±0.1% @ 21-60 mA	
Aggregate output current	1.725A @ 10V and 1.625A @ -10V	
Capacitive loads	180 pF min	
Settling time	10μs to 0.003%	
Slew rate	10V/μs	
Gain bandwidth	1 MHz	
Noise	less than 2 LSB RMS, 0-10000 Hz	
Output protection	short to ground, ±15V	
Power-on state	0.0000V ±5mV (default),	
	user programmable	
Gain drift	25 ppm/°C	

Digital I/O	
Number of channels	8 inputs, 8 outputs
Compatibility	CMOS/TTL, 2kV ESD protected
Power-on state	logic zero (default),
	user programmable
Data transfer modes	DMA, interrupt, software
Input termination	4.7kΩ pull-up to 5V
Output high level	3.0V typ @ -32mA, 3.4V typ @ -16mA, 4.2V
	@ -2mA
Output low level	0.55V max @ 64mA
Input low voltage	0.0 - 0.8V
Input high voltage	2.0 - 5.0V
Counter/Timer	
Number of channels	3
Resolution	24 bits
Max frequency	16.5 MS/s for external clock,
	33 MS/s for internal DSP clock
Min frequency	0.00002 Hz for internal clock,
	no low limit for external clock
Min pulse width	20 ns
Output high level	2.9V typ @ -4 mA
Output low level	0.5V min @ 4 mA
Protection	7 kV ESD, ±30V over/undershoot
Input low voltage	0.0 - 0.8V
Input high voltage	2.0 - 5.0V

#### **Connection Schemes:**

Connector On The Board	Cable Required	Target Panel	Description	
J1	PD-CBL-96	PD2-AO-STP-32	Carries analog output lines to 32-channel terminal panel	
J2	PD-CBL-37	PD2-AO-STP-32	Carries 8 digital input and 8 digital output lines to 32-channel terminal panel	
J1	PD-CBL-96	PD-BNC-64* Carries analog output lines to 64-channel BNC terminal panel		
J2	PD-CBL-37	PD-BNC-64	Carries 8 digital input and 8 digital output lines to 64-channel BNC terminal panel	
J2	PD-CBL-3650-8/8	PD2-DIO-BPLANE16	Carries digital lines to digital isolation panel for adding relays to the DIO lines	

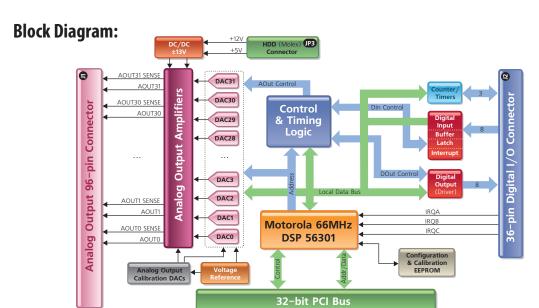
<sup>\*</sup> PD-BNC-64 was initially designed for analog input subsytem of UEI's multifunction boards. Thus the analog output signals transferred via PD-CBL-96 will not match the signal designations on PD-BNC-64's J1 connector. See PowerDAQ Analog Output Manual for more details and remapping diagram.

# **Sensing Configuration:**

Partial disassembly of the board is required for setting jumpers to the required position. An appropriate jumpers configuration of the PD2-AO-STP-32 is required as well.

		PD2-AO-32/16HC		PD2-AO-STP-32		
		Jumper Position (W1 - W32) <sup>1</sup>	Signals	Jumper Position (JP1 - JP32) <sup>3</sup>	Signals	
	Local	00	AOUTX <sup>2</sup> and AOUTX SENSE <sup>2</sup> carry the same signal. No compensation for the voltage drop across the cable (PD-CBL-96).	A B C D	OUTX <sup>3</sup> carries actual analog output signal; SNSX <sup>3</sup> carries analog ground	
Sensing	Remote on STP	0 0	AOUT <b>X</b> SENSE <sup>2</sup> line is used to sense and compensate for the voltage drop across the cable (PD-CBL-96). Voltage drop across the load wiring is not compensated.	0 0 0		
	Remote at load	(default)	AOUT <b>X</b> SENSE <sup>2</sup> line is used to sense and compensate for the voltage drop across the cable (PD-CBL-96). Voltage drop across the load wiring is compensated.	A B C D O O O	OUTX <sup>3</sup> carries actual analog output signal; SNSX <sup>3</sup> carries actual analog output sense signal; OUTX <sup>3</sup> and SNSX <sup>3</sup> should be tied together at the load	

<sup>1</sup> As designated on the PD2-AO-32/16HC board; 2 As designated in pinout diagram for the J1 connector (PD2-AO-32/16HC); 3 As designated on the PD2-AO-STP-32 terminal panel



## **Pinout Diagrams:**

