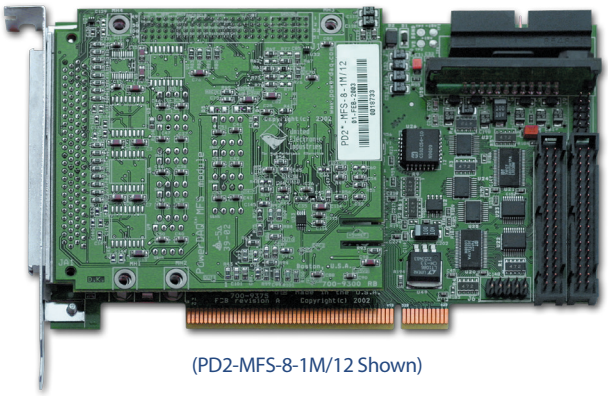
PD2-MFS

PowerDAQ II Simultaneous-Sampling Multifunction Boards

- 4/8 single-ended or 4/8* differential A/D channels (*optional)
- 300 kS/s — 2 MS/s sampling rate
- 12-, 14-, 16-bit resolution; optional gains 1, 2, 5, 10
- Two 12-bit analog outputs; 32 digital I/O; three 16-bit counter/timers
- Simultaneous operation of all subsytems
- Stream-to-disk capability
- Multiple boards operate in one PC
- Optional differential inputs
- Extensive triggering for A/D and D/A
- Full PCI-bus implementation



(PD2-MFS-8-1M/12 Shown)

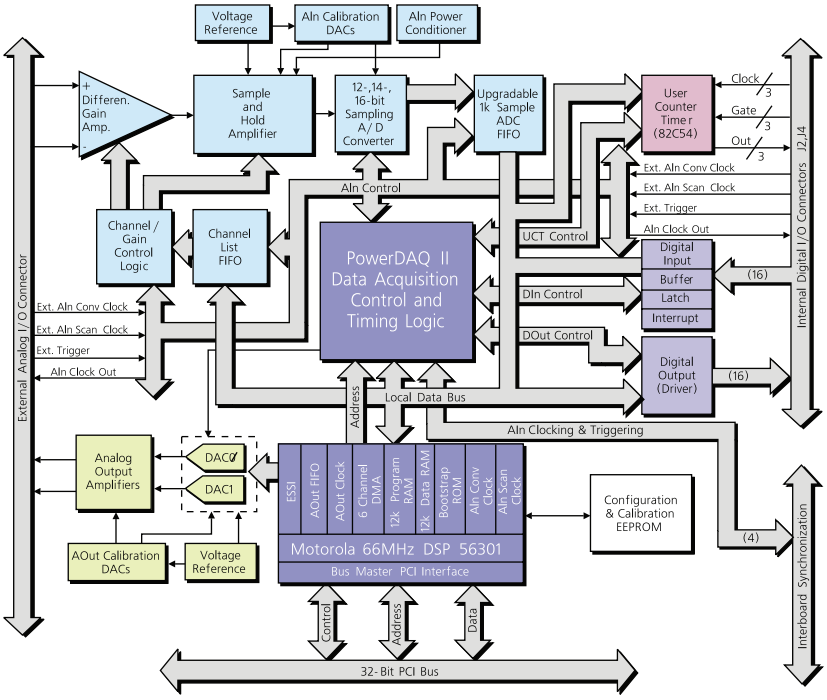
Supports **UEIDaq Framework** Data Acquisition Software Library for Windows. Linux and QNX drivers available. Visit our website for more details.

General Description:

For some applications, it's essential to sample several channels at the same time within a few nanoseconds—a feat not possible with multiplexed multi-channel boards no matter how fast their burst rate across all the channels. For these tasks, UEI is proud to offer the PD2-MFS Series, the only PCI boards currently available with as many as eight sample/hold amplifiers. This approach eliminates the need for expensive, bulky external simultaneous-sampling units. Not only do they offer the best in simultaneous sampling, they also come with the MF Series' array of other I/O capabilities including analog outputs, digital I/O and counter/timers.

PD2-MFS boards build on all the power of the PD2-MF Series including DSP control of all I/O subsystems. Here you have a choice of four or eight inputs running in either single-ended or differential modes. Three resolution grades and corresponding sampling rates are available: 16 bits (300 or 500 kS/s), 14 bits (500 kS/s, 800 kS/s and 2 MS/s) or 12 bits (1 MS/s). In addition, you can purchase models with individual per-channel programmable-gain amplifiers.

Block Diagram:



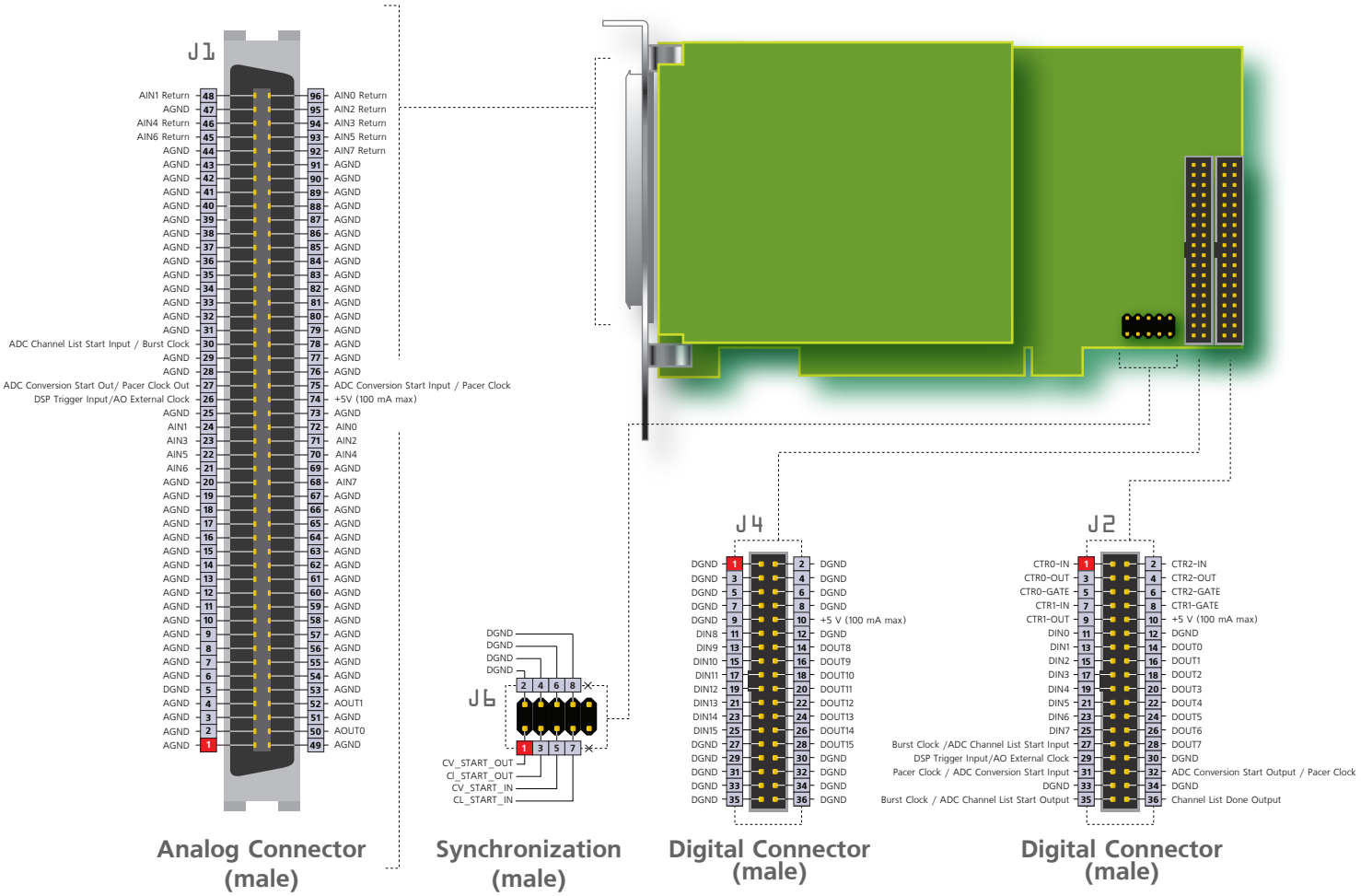
We supply a complete set of drivers for all popular programming languages and third-party applications including LabVIEW and Agilent VEE -- and at no additional charge! The support package also comes with example programs, complete with source code, that are so extensive that some of them might be enough to solve your problem straight out of the box.

To achieve optimum performance under Windows, we wrote the boards' 32-bit driver from scratch without relying on any legacy code. This advanced protocol-based driver works with shareable buffers in system RAM and makes obsolete traditional register-based drivers and double-buffering schemes. MF Series boards can stream data to disk continuously, gapfree, at the hardware?s peak acquisition rates!

Technical Specifications:

Model: PD2-MFS-xx-	2M/14	1M/12	800/14	500/16	500/14	300/16
Resolution	14 bits	12 bits	14 bits	16 bits	14 bits	16 bits
Number of Channels Single-Ended Differential	4 (8 optional) 4 (8 optional)					
Maximum Sampling Rate (multiple channels)	2 MS/s	1 MS/s	800 kS/s	500 kS/s	500 kS/s	300 kS/s
Onboard FIFO Size (upgradeable to 16k, 32k, 64k)	4k samples			1k samples		
Input Ranges	0-5 V, ±5 V, 0-8 V, ±8 V @ 10 V ranges	0-5 V, 0-10 V ±5 V, ±10 V (software selectable)				
Channel-Gain List	256 entries					
Programmable Gains (by channel)	G=1 (or 1, 2, 5, 10 with -DG option)					
Drift Zero Gain	±30 µV/°C ±30 ppm/°C					
Input Impedance	1 MΩ					
Input Bias Current	±100 pA					
Input Overvoltage	±18 V SE ±40 V DI					
A/D Conversion Time	0.45 µs	0.8 µs	1.25 µs	2.0 µs	2.0 µs	3 µs
SSH Amp Settling Time	0.7 µs	0.9 µs	1.0 µs	1.2 µs	1.2 µs	1.2 µs
A/D Settling Time	0.4 µs	0.6 µs	1.25 µs	1.5 µs	1.2 µs	2.7 µs
DC Accuracy						
Nonlinearity (no missing codes)	±2 LSB	±0.5 LSB	±0.5 LSB	±1 LSB	±1 LSB	±1 LSB
AC Accuracy						
Effective Number of Bits	12.1	11.3	12.7	13.8	12.7	13.8
Channel Crosstalk	-80 dB @ 1 kS/s					
Clocking and Trigger Input						
Maximum A/D Pacer Clock	1500 kS/s @ 4 ch, 1700 kS/s @ 8 ch	975 kS/s @ 4 ch, 1095 kS/s @ 8 ch	800 kS/s	500 kS/s	500 kS/s	300 kS/s
External A/D Sample Clock Maximum Frequency	1500 kS/s @ 4 ch, 1700 kS/s @ 8 ch	975 kS/s @ 4 ch, 1095 kS/s @ 8 ch	800 kS/s	500 kS/s	500 kS/s	300 kS/s
Minimum Pulse Width	20 ns					
External Digital (TTL)Trigger High-level Input Voltage Low-level Input Voltage Minimum Pulse Width	2.0V min 0.8V min 20 ns					

Pinout Diagrams:



Analog Connector (male)

Synchronization (male)

Digital Connector (male)

Digital Connector (male)

Connection Schemes:

Connector On The Board	Cable Required	Target Panel	Description
J1	PD-CBL-96	PD2-AO-STP-16	Carries analog output lines to 16-channel terminal panel
J2	PD-CBL-37	PD2-AO-STP-16	Carries 8 digital input and 8 digital output lines to 16-channel terminal panel
J1	PD-CBL-96	PD-BNC-64*	Carries analog output lines to 64-channel BNC terminal panel
J2	PD-CBL-37	PD-BNC-64	Carries 8 digital input and 8 digital output lines to 64-channel BNC terminal panel
J2	PD-CBL-3650-8/8	PD2-DIO-BPLANE16	Carries digital lines to digital isolation panel for adding relays to the DIO lines
J1	PD-CBL-96	PD-AO-AMP-100	Amplifies analog outputs to ±100V per channel
J1	PD-CBL-96	PD-AO-AMP-115	Amplifies analog outputs to ±115V per channel

* PD-BNC-64 was initially designed for analog input subsytem of UEI's multifunction boards. Thus the analog output signals transfered via PD-CBL-96 will not match the signal designations on PD-BNC-64's J1 connector. See PowerDAQ Analog Output Manual for more details and remapping diagram.

Specifications: (PD2-MFS-all models)

Digital I/O	
Input Bits (8 can generate IRQ)	16
Output Bits	16
Inputs High-level Input Voltage Low-level Input Voltage High-level Input Current Low-level Input Current	 2.0 V (min) 0.8 V (max) 20 µA -20 µA
Outputs	
Output Driver High Voltage Output Driver Low voltage:	2.5 V min, 3.0 V typ (IOH = -32 mA) 0.55V max (IOL = 64 mA)
Current Sink	-32/64 mA max, 250 mA per port
Pulse Width	20 ns min, interrupt bit latched on rising, falling or either edge
Power-on Voltage	Logic Zero

Counter/Timer	
Number of channels	3 available to user (Intel 82C54)
Resolution	16 bits on each counter
Clock Inputs Software configurable High-level Input voltage Low-level Input voltage High-level Input current Low-level Input current	 Internal 1 MS/s, External ≤ 10 MS/s 2.0V min 0.8V max 20 µA -20 µA
Gate Inputs Maximum Pulse Width	 100 ns (High) 100 ns (Low)
Counter Outputs Output Driver High Voltage Output Driver Low Voltage	Inverted 2.5V min (I_{OH} = 24 mA) 0.55V max (I_{OH} = 48 mA)

Analog Outputs	
Number of channels	2
Resolution	12 bits
Update Rate	200 kS/s each
Onboard FIFO Size	2k samples (on DSP)
Analog Output Range	±10 V
Error Gain Zero	 ± LSB Calibrated to 0
Current Output	±20 mA max
Output Impedance	0.3Ω typ
Capacitive Drive Capability	1000 pF
Nonlinearity	±1 LSB
Protection	Short circuit to analog ground
Power-on Voltage	0V ±10 mV
Setting Time to 0.01% of FSR	10 µs, 20V step 1 µs, 100-mV step
Slew Rate	30 V/µs

General Specifications	
Power Requirements	5V
Physical Dimensions	10.5 x 3.8" (262 x 98 mm)
Environmental Operating Temperature Range Storage Temperature Range Relative Humidity	 0 to 70 °C -25 to 85 °C to 95%, noncondensing
Connector J1	96-pin high-density Fujitsu connector (male) (Fujitsu PN#FCN-245P096-G/U)
Connector J2	36-pin header connector (male) (Thomas and Betts PN#609-3627)
Connector J4	36-pin header connector (male) (Thomas and Betts PN#609-3627)
Connector J6	8-pin male connector (Adam-Tech PN#PH2-SMT-8-SGA

Ordering Guide:

Part Number	Description
PD2-MFS-4-2M/14	2 MS/s, 14-bit, 4SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MFS-8-2M/14	2 MS/s, 14-bit, 8SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MFS-4-1M/12	1 MS/s, 12-bit, 4SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MFS-8-1M/12	1 MS/s, 12-bit, 8SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MFS-4-800/14	800 kS/s, 14-bit, 4SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MFS-8-800/14	800 kS/s, 14-bit, 8SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MFS-4-500/14	500 kS/s, 14-bit, 4SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MFS-8-500/14	500 kS/s, 14-bit, 8SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MFS-4-500/16	500 kS/s, 16-bit, 4SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MFS-8-500/16	500 kS/s, 16-bit, 8SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MFS-4-300/16	300 kS/s, 16-bit, 4SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MFS-8-300/16	300 kS/s, 16-bit, 8SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
Upgrade Options	
PD2-MFS-4-DG4	Upgrade 4SE to 4DI with gains (1, 2, 5, 10)
PD2-MFS-8-DG4	Upgrade 8SE to 8DI with gains (1, 2, 5, 10)
Upgrade FIFO	
PD-16KFIFO	Upgrade 1K FIFO to 16K FIFO
PD-32KFIFO	Upgrade 1K FIFO to 32K FIFO
PD-64KFIFO	Upgrade 1K FIFO to 64K FIFO