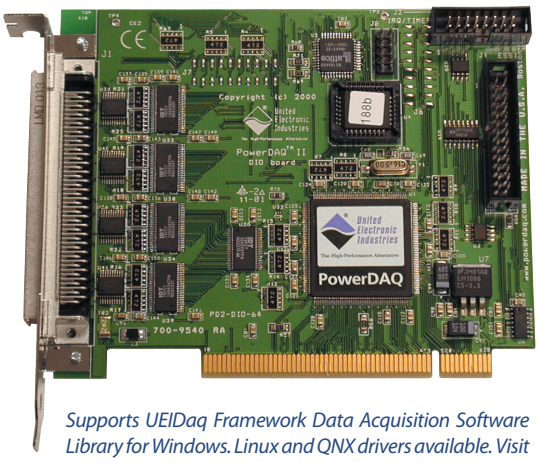
PDL-DIO

PowerDAQ Lab PCI Digital I/O Boards

- 64 or 128 lines (5V/TTL) of I/O in 16-bit ports
- Generate interrupts on any line
- Four separate high-speed IRQ lines (100 ns)
- Custom logic chip replaces obsolete 8255 and equivalents
- Ideal for solid-state relays
- User-defined power-up state in 16-bit groups (High, Low, Tri-stated)
- 0-kΩ onboard pull-down resistors for all I/Os
- Onboard FIFO: 1k samples in/2k samples out
- Two Enhanced Synchronous Serial Interfaces (ESSIs)
- Optional 192kb on-board SDRAM
- Three 24-bit counter/timers
- Port-scan list
- Start/Stop external trigger line
- Rigid 96-conductor pinless SCSI connector
- MTBF greater than 500,000 hours



Supports UEIDaq Framework Data Acquisition Software Library for Windows. Linux and QNX drivers available. Visit our website for more details.

General Description

For applications that involve a high number of digital points, UEI offers three models in the PDL-DIO family with 64 I/O lines. Instead of following the industry trend of implementing discrete I/O with cumbersome and limiting 8255-type devices, we work with 16-bit line drivers under control of a DSP and custom logic.

As a result, you no longer need to create external circuitry to guarantee power-on startup states; our software allows you to configure startup states in groups of 16-bit ports. You no longer need to design separate interrupt circuitry; our hardware comes with four high-speed interrupts waiting for you to use. The digital I/O lines are protected against electrostatic discharge and automatically detect shorts on power up.

Besides digital I/O, the board features three 24-bit counter/timers as well as two high-speed ESSI (Enhanced Synchronous Serial Interface) ports. The onboard DSP and optimized PCI-bus interface also allow the card to optionally stream digital data to or from disk at rates as high as 2 MB/s and count events up to 16.5 MHz.

The PDL-DIO can be configured for 16- or 32-bit pattern I/O. It supports change detection, handshaking lines to clock parallel digital I/O and externally clocked pattern generation.

Distribution panels make all the board's I/O capabilities available for field connection. Further, an optional accessory (PDL-DIO-CONN64-4) distributes the 64 digital I/O points into four sets of 16 lines through industry-standard 50-pin IDC connectors. They, in turn, attach directly to relay panels available from UEI and many other sources.

The PDL-DIO is ideally suited for OEM applications. Optional SDRAM and firmware development kit allow customers to develop their own DSP code based on examples provided in the SDK or use this memory as a buffer for I/O operations.

Technical Specifications:

DC Electrical Characteristics Over Operating Range		
Input High Level	Guaranteed logic High level	2.0V min
Input Low Level	Guaranteed logic Low level	0.8V max
Input High Current	V_I = 5V	±1 µA max
Input Low Current	V_I = Gnd	±1 µA max
3-State Output Current	V_O = 2.7V	±1 µA max
3-State Output Current	V_O = 0.5V	±1 µA max
Short-Circuit Current	V_O = Gnd (momentary)	-80 mA min -140 mA typ -250 mA max
Input Hysteresis		100 mV typ

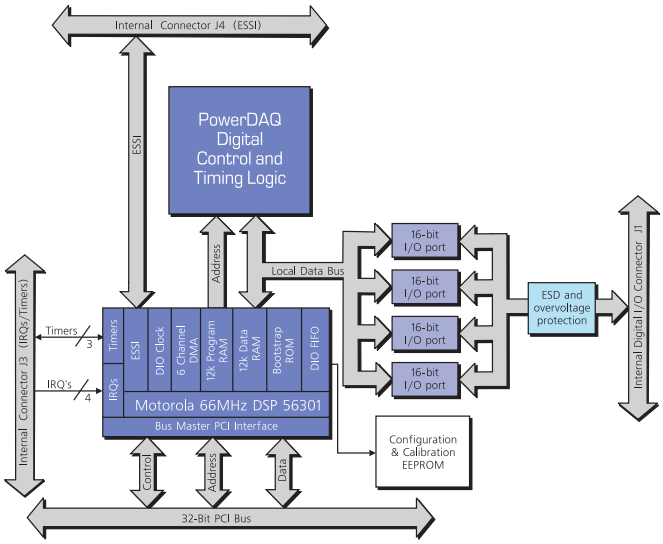
Output Drive Characteristics		
Output Drive Current	V_O = 2.5 V	-32 mA per pin -180 mA per port
Output High Voltage	I_{OH} = -3 mA	3.5V typ, 4.8V max
Output High Voltage	I_{OH} = -15 mA	3.5V typ, 4.7V max
Output High Voltage	I_{OH} = -32 mA	2.4V min, 3.0V typ
Output High Voltage	I_{OL} = 64 mA	0.2V typ, 0.55V max
I/O Power Off Leakage	$V_{I/O} \leq$ 4.5V	±1 µA max

Counter /Timer	
Prescaler	1 (21-bit)
Number of Channels	3
Resolution	24 bits
Maximum Frequency	16.5M S/s for external clock and 33M S/s for internal DSP clock
Minimum Frequency	0.0000002 S/s for internal clock, no low limit for external clock
Minimum Pulse Width	20 ns
Output High Level	2.0V min @ -4 mA
Output Low Level	0.5V max @ 4 mA
Protection	7 kV ESD, ±30V overshoot/undershoot
Input Low Voltage	0.0-0.8V
Input High Voltage	2.0-5.0V

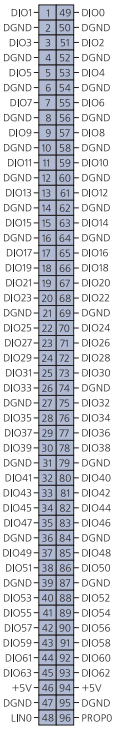
ESSI Characteristics

The Motorola 56301 DSP contains two fast Enhanced Synchronous Serial Interfaces. The PowerDAQ DIO board allows access to both. Each ESSI port contains three transmitters and one receiver and has a maximum operational speed of 15M bits/sec.

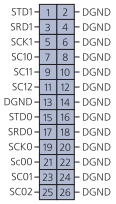
Block Diagram:



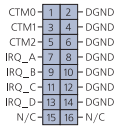
Pinout Diagrams:



PowerDAQ PDL-DIO
Digital I/O Connector (J1)



PowerDAQ PDL-DIO
ESSI Male Connector (J4)



PowerDAQ PDL-DIO
Counter/Timers/IRQ Lines
Male Connector (J3)

Ordering Information:

Part Number	Description
PDL-DIO-64	64 digital I/O channels, 3 counter/timers, 2 ESSI ports, four high-speed IRQ lines (100 ns), SRAM*
PDL-DIO-64ST	64 digital I/O channels, high-speed pattern generation and digital streaming, SRAM*
PDL-DIO-64CT	64 digital I/O channels, high-speed event counts streaming (2 Mwords/s), SRAM*

* Optional