UEI–820

UEI-820 board is designed as a drop-in replacement for ADI RTI-820 board. All registers map remains the same.

There are some jumpers change described below :

Jumpers

E1 – When installed external A/D conversion clock will be used. Positive edge of external clock will pace A/D conversion.

E2 – A/D settling time delay – when installed – 100 uS, when open – 20 uS delay will be added after A/D channel write before A/D conversion.

E4 – DAC coding. When installed – twos, when open – straight binary.

E6 – A/D coding. When installed – twos (MSB inverted and extended in upper four bits), when open – straight binary.

E8, E9 – D/A range. When installed +/-5V, when open – 0..5 V.

SW1 – address switch (same as on RTI-820)

SW2 – IRQ selection switch

J5 – debug header – do not install any jumpers

J3 – clock select header. Always install J3 in (1-2) position.

Calibration

A/D – offset only. Apply 0.0000V at A/D input and use R59 to achieve 0x800 readings.

D/A – R13 – offset, R8 – gain.

A/D Subsystem

Resolution	12 bits
Channel register	6 bits (up to 64 channels)
Write strobe	456 ns
Maximum Sampling Rate	20Ks/s
Type of A/D	Successive approximation
Input Range	±5V (fixed)
Drift	
Zero	±30 μV/°C
Gain	±30 ppm/°C
Input Impedance	100 MΩ in parallel with 22 pF
Input Bias Current	±20 nA
Input Overvoltage	+/- 20V cont., powered or unpowered
A/D Conversion Time	25 μS
A/D Settling Time	20/100 μS (jumper selectable)

DC Accuracy	
Nonlinearity	±0.5 LSB (no missing codes)
System Noise	0.5 LSB
AC Accuracy	
Effective Number of Bits	11.4
Total Harmonic Distortion+ Nonlinearity+Noise	70.2 dB
Clocking and Trigger Input	
Maximum A/D Pacer Clock	
Aggregate Throughput	20 kS/s @0.001% accuracy
External A/D Sample Clock	
Maximum Frequency	20 kS/s
Minimum Pulse Width	100 nS

Additional A/D features available on UEI–820 board:

- Software/external A/D clock (jumpers configurable)
- Interrupt on conversion complete/overrun
- Two's-compliment and straight binary coding

D/A Subsystem

Number of Channels	1
Channel list register	6 bits
Channel write strobe	608 ns
Resolution	12 bit
Update Rate	400S/s
Analog Output Range	0-5V, ±5V (jumpers selectable)
Error	
Gain	±0.5 LSB
Zero	Calibrated to 0
Current Output	±18 mA minimum
Output Impedance	0.3Ω typical
Capacitive Drive Capability	0.001 μF
Non-linearity	±1 LSB
Protection	Short circuit to analog ground
Power-on Code	0h000
Setting Time to 0.01% of FSR	10 μS, 20V step, 1 μS, 100 mV step
Slew Rate	10 V/ μS

Additional D/A features available on UEI–820 board:

- Two's-compliment and straight binary coding

Once calibrated for the particular mode (Unipolar or Bipolar) the stability and linearity over full-scale is +/- 0.5 LSB. Offset and gain errors are in a +/- 0.5 LSB range. When changing ranges, the maximum offset is 6 mV.

DIn/DOut subsystem

Input/Output Bits inverted	24, in groups of 8 (with on-board 10 K pull-up resistors),
Direction	Software selectable
Inputs	
High-level Input Voltage	2.0V minimum
Low-level Input Voltage	0.8V maximum
High-level Input Current	20 μA
Low-level Input Current	-20 μA
Outputs	
Output Driver High Voltage	2.5V minimum, 3.0V typical (I_{OH} = -32 mA)
Output Driver Low voltage:	0.55V maximum, (I_{OL} = 32 mA)
Current Sink	-64/32 mA maximum
Power-on Voltage	Logic Zero

Control register/Interrupts

The board implement the control/status register which contains the A/D interrupt enable bits and allows you to read the A/D status (conversion complete/overrun/in-progress).

The following status bits available:

- Conversion in progress (auto-cleared at the end of the conversion) (CP)
- Conversion complete (CC)
- Conversion overrun (CO)

The CP bit is set only at the time of A/D conversion, the CC bit is set at the end of the each conversion and cleared after the high byte read from the A/D data register, the CO bit is set when A/D conversion software command/external clock coming before data was read from the A/D register. In this situation old data will be stored and no new conversion will be allowed until data will be read from the A/D register.

All the status bits are cleared using the Flags Clear command asynchronously at any time.

There are two interrupt enable flags in the control register:

- Conversion complete (CCI)
- Conversion overrun (COI)

CCI —This interrupt is cleared after reading from the A/D

COI —This interrupt is cleared only after the Flags Clear command

Also board implement DAC status register which contain following information about DAC FIFO: FIFO Ready, Follow with data, FIFO full.

I/O Address Selection

Table 1: I/O Map Address Locations per DIP Switch Placement

DIP Switch Position						Base Address Extension (in Hex)
1	2	3	4	5	6	
ON	ON	NOT USED	ON	ON	ON	200H
ON	ON		ON	ON	OFF	210H
ON	ON		ON	OFF	ON	220H
ON	ON		ON	OFF	OFF	230H
ON	ON		OFF	ON	ON	240H
ON	ON		OFF	ON	OFF	250H
ON	ON		OFF	OFF	ON	260H
ON	ON		OFF	OFF	OFF	270H
ON	OFF		ON	ON	ON	280H
ON	OFF			ON	OFF	290H
ON	OFF			OFF	ON	2A0H
ON	OFF			OFF	OFF	2B0H
ON	OFF		OFF	ON	ON	2C0H
ON	OFF		OFF	ON	OFF	2D0H
ON	OFF		OFF	OFF	ON	2E0H
ON	OFF		OFF	OFF	OFF	2F0H
OFF	ON		ON	ON	ON	300H
OFF	ON			ON	OFF	310H
OFF	ON			OFF	ON	320H
OFF	ON			OFF	OFF	330H
OFF	ON		OFF	ON	ON	340H
OFF	ON		OFF	ON	OFF	350H
OFF	ON		OFF	OFF	ON	360H
OFF	ON		OFF	OFF	OFF	370H
OFF	OFF		ON	ON	ON	380H
OFF	OFF			ON	OFF	390H
OFF	OFF			OFF	ON	3A0H
OFF	OFF			OFF	OFF	3B0H
OFF	OFF		OFF	ON	ON	3C0H
OFF	OFF		OFF	ON	OFF	3D0H
OFF	OFF		OFF	OFF	ON	3E0H
OFF	OFF		OFF	OFF	OFF	3F0H

1. Factory Configuration